Accredited Standards Committee
X3, Information Processing Systems

Doc: X3T10.1/96a165r1
Date: September 22, 1996
Project: X3T10.1 / 1146D
Ref Doc.: SSA-PH2 rev 3
Reply to: John Scheible

To: X3T10.1 Membership
From: John Scheible

Subject: Changes to SSA-PH3 rev 3

## BACKGROUND

This document is intended to document the issues to SSA-PH2 rev 3 prior to the Boston meeting (rev 0) and the agreements reached at the Boston meeting (later revs). The changes will be rolled into SSA-PH2 rev 3a.

## ISSUE 1 (Connector Pinout)

INPUT: Dan Tsai wrote:

Could you change table 22 to as following ? These are input from Bill Ham.

a) pin 2: Ground.
b) Pin 4: Module fault detect
c) Pin 5: Output disable
d) Pin 7: Power +5 V d.c.

Pin not mentioned stay the same.

QUESTIONS: I have the following questions?

a) Is pin 2 Logic ground or frame ground?
b) What is the definition of Module fault detect? What error conditions cause the D/R to drive it (assuming it is a D/R output)? What is the level of assertion/deassertion?
c) What is the definition of Output disable? Is it an input from the cable/optical transducer? Is it mandatory to disable the D/R if it is asserted? What is the level of assertion/deassertion?
d) Is the Pin 7 (+5 V ± 5%) really optional?

CHANGES: The following changes are proposed for SSA-PH2 rev 3a pending answers to the questions.

### Table 22 - External HSSD device connector pinout

| Pin | Signal | Notes |
|---|---|---|
| 1 | LineOut+ | |
| 2 | Logic ground | |
| 3 | LineOut- | |
| 4 | Module Fault Detect | |
| 5 | Output Disable | |
| 6 | LineIn- | |
| 7 | +5 V ± 5% (optional) | If supplied shall be capable of supplying a minimum of 0,25 A and a maximum of 1,0 A. Direct shorts to ground shall not cause damage. |
| 8 | LineIn+ | |
| Shield | Shield | Shall conform to 8.5.2. Shield connection shall make before any other pin upon insertion. |

ISSUE 2 (Eye diagram changes)

INPUT: Phil Murfet wrote summarizing the eye diagram changes:

The minimum height of the eye should be dropped to 500mv to accommodate reflections and ringing. The rise and fall times be adjusted to reflect the minimum dV/dt of 2V/ns. The dual slope rising edge be removed so that the eye is symmetrical, and finally the jitter be increased from 140ps to 200ps to accommodate ringing, reflections, noise and AC droop.

Table 4 in PH2 be changed so that..

a) V1=V2= 500mV for both 400Mb/s and 200Mb/s (V2 can thus be removed)
b) T1=0.1ns for 400Mb/s
c) T3=0.35ns for 400Mb/s
d) T3=0.39ns for 200Mb/s
e) T5 can be removed
f) T8=2.15ns for 400Mb/s
g) T8=4.61ns for 200Mb/s
h) T10=2.4ns for 400Mb/s
i) T10=4.9ns for 200Mb/s
j) T12=2.6ns for 400Mb/s
k) T12=5.1ns for 200Mb/s

QUESTIONS: I have the following questions?

a) Figure 9 will need to be changed to show a shape with a rectangle and two equal triangles at each end. Does anyone have such a picture in .DXF format?
b) What is the purpose of V3? I could guess that no signal may even momentarily exceed the ± 1000 mV level. If this is the case, how is it tested? Where is it specified?

CHANGES:

Table 1 - Driver system operating parameters

| Speed | V1 | V3 | T1 | T3 | T8 | T10 | T11 | T12 |
|---|---|---|---|---|---|---|---|---|
| 400 Mb/s | 500 mV | 1000 mV | 0,10 ns | 0,35 ns | 2,15 ns | 2,40 ns | 2,50 ns | 2,60 ns |
| 200 Mb/s | 500 mV | 1000mV | 0,14 ns | 0,61 ns | 4.61 ns | 4,90 ns | 5,00 ns | 5,10 ns |

Table 2 - Driver test parameters

| Speed | V1 | V3 | T2 | T4 | T6 | T7 | T9 | T11 | T13 |
|---|---|---|---|---|---|---|---|---|---|
| 400 Mb/s | 500 mV | 1000 mV | 0,14 ns | 0,39 ns | 1,89 ns | 1,89 ns | 2,36 ns | 2.50 ns | 2.64 ns |
| 200 Mb/s | 500 mV | 1000 mV | 0,28 ns | 0,75 ns | 3,00 ns | 3,78 ns | 4,72 ns | 5,00 ns | 5,28 ns |

ISSUE 3 (Name change and other issues)

Dan Tsai Wrote:

The term "Line Driver" used in Phy2 Section 7.1 and its subsection are very confusing. eg. in 7.1 it is used to describe the output of CMOS driver with 18 ma. in7.1.3 it is used to describe the pin at the cable connector after resistor and ac couple capacitor. in 7.1.5 it is used to describe port output current @ 9 ma.

In Phy1, since CMOS driver pin and connector pin are of the same node and there is no confusion. But in Phy2, with resistor and cap, these two pins are two different nodes and we need to differentiate these two nodes.

Since the terms of "Line Driver" is defined as "the electrical circuitry that sets the logical state of the line atthe port connector", we need a new term to define the actual (CMOS) driver circuit.

Proposal:

Define a new term "On Chip Line Driver" which is used to define only the behavior of the chip driver circuitry. Change 7.1 title to "On Chip Line Driver, On Chip Line Driver Load and Line Driver. Also modify all sections in 7.1 accordingly to reflect this proposal.

Dave Instone responded with:

I agree there is confusion but I don't think a new term is needed to resolve this. However Figure 5 is incorrect. The Y axis is labelled 'Line current' If this is true then +9.5mA and -9.5mA needs to be changed to +4.75mA and -4.75mA. The confusion is then removed by adding 'at the port connector' to the title of figure 5. Then remove the second sentence from 7.1.3.1 and add the following to 7.1.3 ( which has no text at present) 'Line Driver measurements are referenced to the Port Connector. Finally add 'at the port connector' to the title of Table 5. These amendments should remove both the confusion and the one error.

Dan Tsai then responded with:

Dave, I was a little lazy and did not identify all the sections that have problems without new term defined at chip driver pin.

a) 7.1.1. We need to delete or modify "single current source", "N channel tansistor", can not show figure Figure 4.
b) 7.1.6 Figure 10, what is that "Triangle" in the figure.
c) 7.1.6.2 Line Driver Termination: We can not call it "Line Driver Termination or Line Driver Coupling Element because term "Line Driver" is already at external cable connector pin.

In light of these, I still think give a new term or name at chip driver pin is more straight forward solution.

QUESTIONS: I have the following questions?

a) What does the group want done?

CHANGES: ???

ISSUE 4 (AMP Connector issues)

a) Is the write-up correct (John Scheible made up a lot)?
b) There is a TBD in the connector testing write-up (Lisa investigating).
c) The testing annex references an AMP spec which may not be a standard (this could be a problem) (Lisa investigating).
d) The artwork is flawed (missing dimension references), connector shell indivisible from lines that need to be removed) (Lisa is working on it).
e) Need to verify that the pinouts match FC-AL cable wiring.

ISSUE 5 (Testing capacitance)

INPUT: Dave Instone wrote:

During the discussions on Port Connection Segment testing at Ithaca the Port Connection Segment Test Load was generated. There was some discussion between myself and Bill Ham as to where the scope should be connected. In the end Bills view prevailed and rev 3 shows the scope connected to the connector pins.

Since then I have done some measurements which show that the addition of even 0,4pF of scope probe added at the connector pins causes the impedance at the connector (as seen by a TDR at 375ps risetime) to fall from 137 ohms to 129 ohms. If however the same scope probes are connected at the point at which LC would appear then the impedance at the connector is unaffected. In addition, by connecting the scope probes across the capacitors, which represent the silicons input capacitance, then the signal displayed by the scope will be the signal that the silicon will see. In effect placing the scope across the capacitors removes the disruptive effect of the scope probes from the measurement.

Tests to determine the value of LC required to cause the dip in the TDR plot below 120 ohms for 375pS resulted in a value of around 2.5pF (0805 cap). As the scope probes which most seem to use have capacitances close to this value, placing this much capacitance at the connector would cause the test load with scope probes attached to fail the requirements of 7.3 as there would be two dips below 120 ohms, one at the connector and one at LC.

Figure 16 should therefore be amended to show the scope probes connected across LC.

The sentences which describe the PCS test load ( which starts..The Port Connection Segment test load shall conform...) should be amended to read :

The Port Connection Segment test load with scope probes attached shall conform to the characteristic impedance requirements in 7.3 at its connector. The value of each of the two capacitors LC shall be adjusted such that the total capacitance of LC and is associated probe causes the impedance beyond its time point, measured from its respective LineIn to ground, to fall below 60 ohms for 360 to 375ps. Typically the total capacitance of LC and scope probe will be in the order of 2.5pF.

The above form of words ensures that the capacitive load on each of the lines is matched to practical limits, that the objective we are trying to reach is stated and that an exact value and tolerance for the capacitor LC does not need to be stated.

Reference to LC should then be removed from the sentence which starts ...The values of LR, LC, X and Y....

The sentence referring to scope probe capacitance should not have appeared and should be deleted.

QUESTIONS: I have the following questions?

a) Is this correct?

b) This requirement implies that the implementer not put LR and LC within the silicon, or that an I/O be supplied to measure this point. Do we want to specify this?

CHANGES: Change Figure 16 and the preceding paragraph as follows:

The driver test environment shown in 7.1.3 and the associated measurement procedure shall be used when setting the input signals applied at point M2. Once the input signals have been set, the port connection segment shall be connected in place of the driver test load and measuring equipment. The Port Connection Segment test load (see Figure 1) and the measurement procedure shown in 7.1.3.1 shall be used at point M3. The Port Connection Segment test load with scope probes attached shall conform to the characteristic impedance requirements in 7.3 at its connector. The value of each of the two capacitors LC shall be adjusted such that the total capacitance of LC and its associated probe causes the impedance beyond its time point, measured from its respective LineIn to ground, to fall below 60 ohms for 360 to 375ps. Typically the total capacitance of LC and scope probe will be in the order of 2.5pF. The values of LR, X and Y in Figure 1 shall be 75 Ω ± 1%, 5 cm ± 5 mm, and 5 mm ± 1 mm respectively.

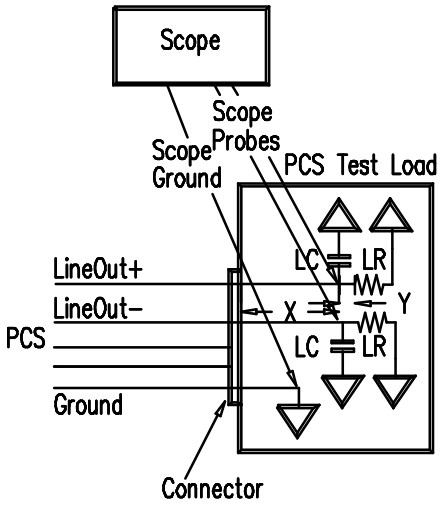


Figure 1 - Port connection segment test load

Sincerely,

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