Accredited Standards Committee
X3, Information Processing Systems

Doc: X3T10.1/96a165r0
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Project: X3T10.1 / 1146D
Ref Doc.: SSA-PH2 rev 3
Reply to: John Scheible

To: X3T10.1 Membership
From: John Scheible

Subject: Chnages to SSA-PH3 rev 3

BACKGROUND

This document is intended to document the issues to SSA-PH2 rev 3 prior to the Boston meeting (rev 0) and the agreements reached at the Boston meeting (later revs). The changes will be rolled into SSA-PH2 rev 3a.

ISSUE 1 (Connector Pinout)

Dan Tsai wrote:

Could you change table 22 to as following ? These are input from Bill Ham.

a) pin 2: Ground.
b) Pin 4: Module fault detect
c) Pin 5:Output disable
d) Pin 7:Power +5 V d.c.

Pin not mentioned stay the same.

ISSUE 2 (Eye diagram changes)

Phil Murfet wrote summarizing the eye diagram changes::

The minimum height of the eye should be dropped to 500mv to accommodate reflections and ringing. The rise and fall times be adjusted to reflect the minimum dV/dt of 2V/ns. The dual slope rising edge be removed so that the eye is symmetrical, and finally the jitter be increased from 140ps to 200ps to accommodate ringing, reflections, noise and AC droop.

Table 4 in PH2 be changed so that..

a) V1=V2= 500mV for both 400Mb/s and 200Mb/s (V2 can thus be removed)
b) T1=0.1ns for 400Mb/s
c) T3=0.35ns for 400Mb/s
d) T3=0.39ns for 200Mb/s
e) T5 can be removed
f) T8=2.15ns for 400Mb/s
g) T8=4.61ns for 200Mb/s
h) T10=2.4ns for 400Mb/s
i) T10=4.9ns for 200Mb/s
j) T12=2.6ns for 400Mb/s
k) T12=5.1ns for 200Mb/s

ISSUE 3 (Name change and other issues)

Dan Tsai Wrote: ==========

The term "Line Driver" used in Phy2 Section 7.1 and its subsection are very confusing. eg. in 7.1 it is used to describe the output of CMOS driver with 18 ma. in7.1.3 it is used to describe the pin at the cable connector after resistor and ac couple capacitor. in 7.1.5 it is used to describe port output current @ 9 ma.

In Phy1, since CMOS driver pin and connector pin are of the same node and there is no confusion. But in Phy2, with resistor and cap, these two pins are two different nodes and we need to differentiate these two nodes.

Since the terms of "Line Driver" is defined as "the electrical circuitry that sets the logical state of the line atthe port connector", we need a new term to define the actual (CMOS) driver circuit.

Proposal:

Define a new term "On Chip Line Driver" which is used to define only the behavior of the chip driver circuitry. Change 7.1 title to "On Chip Line Driver, On Chip Line Driver Load and Line Driver. Also modify all sections in 7.1 accordingly to reflect this proposal.

Dave Instone responded: ==========

I agree there is confusion but I don't think a new term is needed to resolve this. However Figure 5 is incorrect. The Y axis is labelled 'Line current' If this is true then +9.5mA and -9.5mA needs to be changed to +4.75mA and -4.75mA. The confusion is then removed by adding 'at the port connector' to the title of figure 5. Then remove the second sentence from 7.1.3.1 and add the following to 7.1.3 (which has no text at present) 'Line Driver measurements are referenced to the Port Connector. Finally add 'at the port connector' to the title of Table 5. These amendments should remove both the confusion and the one error.

Dan Tsai responded ==========

Dave, I was a little lazy and did not identify all the sections that have problems without new term defined at chip driver pin.

a) 7.1.1. We need to delete or modify "single current source", "N channel tansistor", can not show figure Figure 4.
b) 7.1.6 Figure 10, what is that "Triangle" in the figure.
c) 7.1.6.2 Line Driver Termination: We can not call it "Line Driver Termination or Line Driver Coupling Element because term "Line Driver" is already at external cable connector pin.

In light of these, I still think give a new term or name at chip driver pin is more straight forward solution.

ISSUE 4 (AMP Connector issues)

a) Is the write-up correct (John Scheible made up a lot)?
b) There is a TBD in the connector testing write-up (Lisa investigating).
c) The testing annex references an AMP spec which may not be a standard (this could be a problem) (Lisa investigating).
d) The artwork is flawed (missing dimension references), connector shell indivisible from lines that need to be removed) (Lisa is working on it).
e) Need to verify that the pinouts match FC-AL cable wiring.

Sincerely,

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