Driver Line Termination

This document includes.

1. A suggestion for a new section in PH2 on driver line termination.
2. Notes on coupling capacitor
4. Example of surface mount MLC series impedance vs freq.
3. Example of a SSA40 line driver TDR .

7.4 Line Driver termination

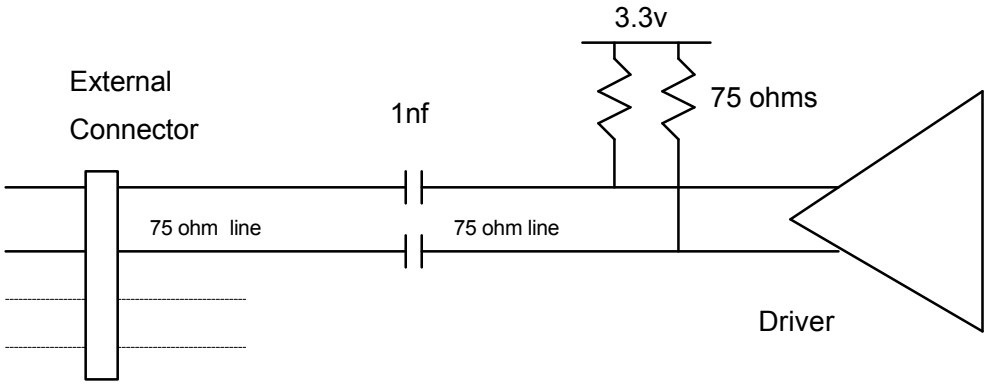
The line driver termination is defined in terms of TDR impedance in the same way as the receiver line termination, table XX gives the limits.

Table XX- Electrical requirements for line termination

Driver port test config	TDR rise time max (ps)	Zo max (ohms)	Zo min (ohms)
Lineout+ to logic gnd	375	90	60
lineout- to logic gnd	375	90	60
line+ to line-	375	180	120

A single excursion below the Zo min limit shall be allowed for a max of 0.75 ns

The diagram below illustrates the schematic of the driver termination.



The 75 ohm terminating resistor shall be +-1% and the 1nF capacitor shall be +-20%. The self resonant frequency of the capacitor shall be greater than 100Mhz and have a series impedance of less than 5 ohms at 400Mhz.

NOTES NOT FOR INCLUSION IN SPEC

AC Coupling capacitance

An AC coupling capacitor needs to have low series impedance and high shunt impedance to ground at frequencies >100Mhz. To achieve this high self resonance and low parasitic capacitance to ground is required.

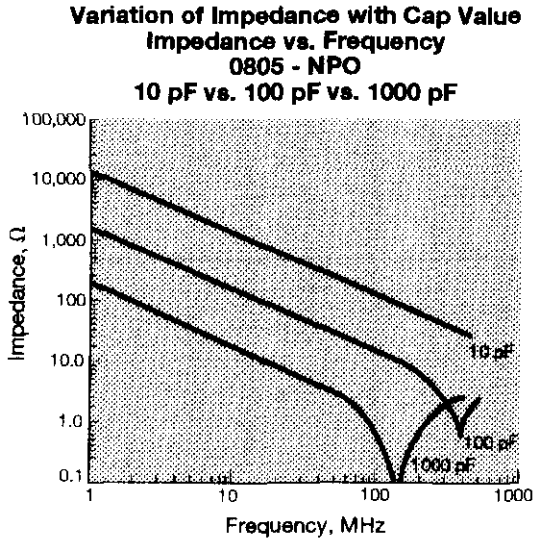
Surface mount Multi-layer Ceramic capacitors have the necessary characteristics to provide the performance, due to there construction and size they have low inductance and low parasitic capacitance to ground.

A 1nf surface mount MLC capacitor with a self resonance of greater than 100 Mhz and series impedance of less than 5 ohms above 400Mhz will give the necessary performance.

The tolerance on this component can be +-20% as the absolute value is not critical.

Capacitance series impedance

Below is a plot of a typical series impedance plot vs frequency. This illustrates the low series impedance



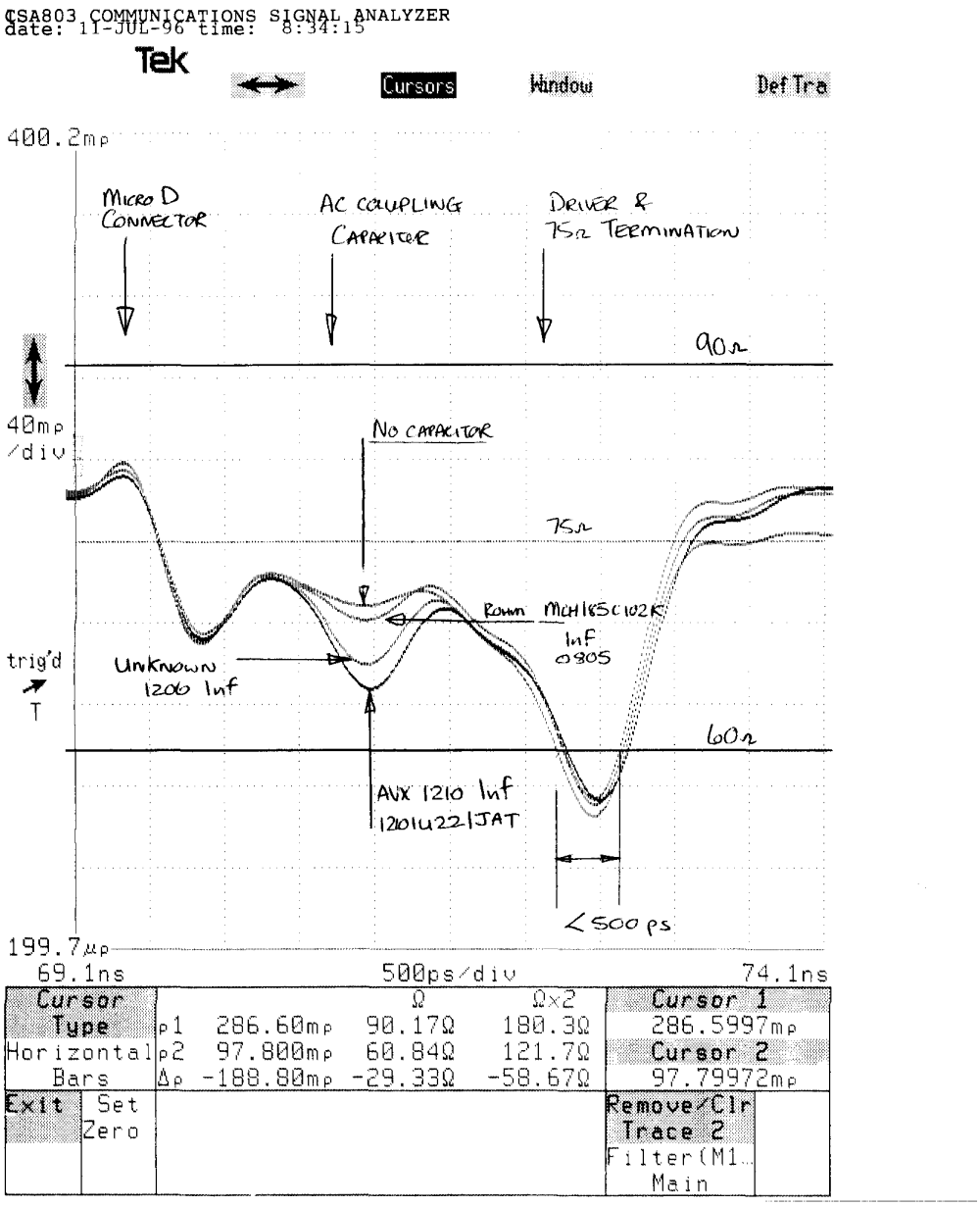
This data came from the AVX web site, a useful source of information.

Typical SSA40 TDR plot

Below is a typical TDR plot for an SSA40 device it includes a plot with no AC coupling capacitor and three other types of 1nf surface mount MLC capacitors .

1. ROHM MCH185C102K...1nf 0805
2. UNKNOWN.....1nf 1206
3. AVX 12101U221JAT 1nf 1210

It can bee seen as the physical size of the package increases from 0805 to 1210 the impedance drops this is because the parasitic capacitance to ground increases.



TYPICAL SSA40 DRIVER SEGMENT IMPEDANCE.