Accredited Standards Committee
X3, Information Processing Systems

Doc: X3T10.1/96a142r5
Date: September 4, 1996
Project: X3T10.1/1146D
Ref Doc.: SSA-PH2 rev 2
Reply to: John Scheible

To: X3T10.1 Membership
From: John Scheible

Subject: SSA-PH2 changes proposal

BACKGROUND

Following the release of SSA-PH2 rev 1, several changes have been proposed on the reflector. This proposal pulls these changes together in a single proposal. Revision 1 of this proposal includes those changes agreed to at the June 1996 X3T10.1 plenary meeting and were included in SSA-PH2 rev 2.

Since that time, additional changes and corrections have been recommended, so I created revisions 2 and 3 of this proposal and will recommend that it be included in SSA-PH2 rev 3 at the Ithica meeting. The revision marks are from revision 1 of this proposal to revision 2 (i.e., the recommenced changes for SSA-PH2 rev 3).

Revision 4 represents the agreements approved at the X3T10.1 plenary in August. Revision 5 includes hard drawn artwork in electronic form.

PROPOSAL 1 (Receiver does not have bypass capacitors) - No change from SSA-PH2 rev 2

Changes: When I created rev 1, I added bypass capacitors to both the receiver and driver. This is not correct, as the Receiver has no bypass capacitors. Make the following changes.

1) Figure 2 - Remove the bypass capacitors shown in both receivers.
2) Figure 10 - Remove the bypass capacitors shown in the receiver.

PROPOSAL 2 (Clarify Annex D requirements regarding Jitter)

Dave Instone did not like the way I changed the word can to shall (definitive writing does not like “can”) in the last sentence of paragraph 1 in Annex D (Jitter). Therefore, replace:

“This annex describes a method whereby the timings shall be applied to the K28.5 character when the predominant jitter is intersymbol jitter.”

with:

“This annex describes a method which enables these timings to be applied to the K28.5 character when the predominant jitter is intersymbol jitter.”

PROPOSAL 3 (Modify Table 6 to reflect both speeds)

Dave Instone notices that table 6 showed only a single row for “Output jitter” as 0,14 ns. This table should be changed as follows:

Replace the row with two rows for “Output jitter at 200 Mb/s (peak to peak)[1] (d)” with a maximum of “0,28 ns” and “Output jitter at 400 Mb/s (peak to peak)[1] (d)” with a maximum of “0,14 ns”.

PROPOSAL 4 (Modifications to the driver test procedure)

Dave Instone pointed out that rev 1 changes that were backed out should not have backed out the change from 2 pF to 1,5 pF which is restored in this proposal. Dave also pointed out the at line difference of 5 mm applied from the connector to the measurement point, and not connector to load resister.

Changes: Add...

a) Modify Figure 6 as shown below.

b) Change the first paragraph of 7.1.3.1 to...

Line drivers shall be tested using the test circuit shown in Figure 6. Line Driver measurements shall be made at the port connector. The distance between the port connector and the load resistance LR (labeled X in Figure 6) shall not exceed 5 cm. The distance between the measurement point (at the LR and MR junction) and the load resistance LR (labeled Z in Figure 6) shall not exceed 5 mm. The difference between the connector to measurement point distance (labeled Y in Figure 6) of the LineOut+ and LineOut- lines of the driver shall not exceed 5 mm. The resistance of the combined load resistance LR and measurement resistance MR shall be 75 $\Omega \pm 2\%$. The connecting media shall meet the requirements in 7.5 for this test. The total additional capacitive load from the scope probing scheme between Line+ and ground and between Line- and ground at the port connector shall be a maximum of 1,5 pF. This capacitance includes the sensing probes and equipment added to enable probing. Additional discrete capacitors between the scope probes and the port connector ground may be needed. The load shall conform to the characteristic impedance requirements in 7.3 at its connector.

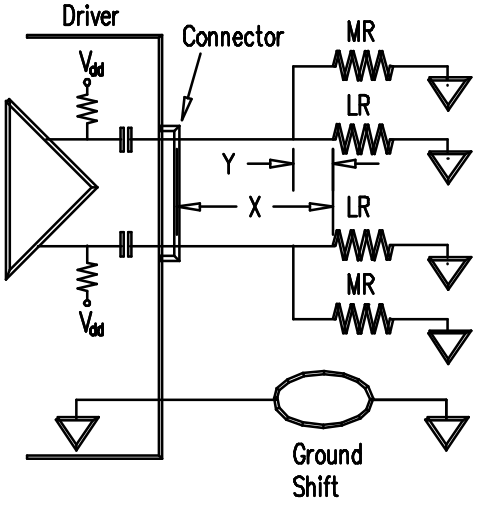

Figure 6 - Test environment for drivers

PROPOSAL 5 (Need words on Driver resister values)

This proposal incorporates the spec changes from Phil Murfet's proposal 96a153r0 entitled "Driver Line Termination". I noticed that Phil's proposal duplicated the same information for Line Receiver termination and Line Driver termination. I also noticed that we have a section 7.3 entitled "Line Segment termination", which is at the same level as the Line Driver and Line Receiver sections. In order to avoid duplicating information (and risking disagreement), I propose the following changes.

a) Replace 7.1.6 with the subclauses shown below

b) Modify "7.3 Line Segment termination" as shown below.

c) Add two new rows to Table 6 labeled "Lineout+ leakage current to ground" with a maximum of "10 μA d.c.", and "Lineout- leakage current to ground" with a maximum of "10 μA d.c.".

7.1.6 Other Line Driver requirements

Figure 9a illustrates the schematic of the Line Driver.

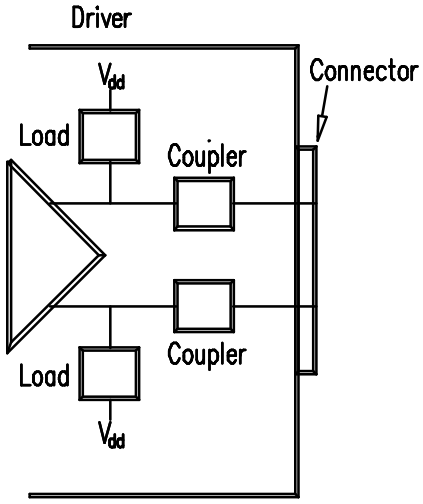

Figure 9a - Line Driver termination schematic

7.1.6.1 Line Driver termination

The Line driver termination is defined in terms of TDR impedance in the same way as Line Segment termination except it is measured at the Port connector Linout pins (see 7.3). Table xx specifies the Line Driver termination requirements.

Table xx - Electrical requirements for Line Driver termination

Receiver port test configuration	TDR rise time max (ps)	Zo max (Ωs)	Zo min (Ωs)
LineOut+ to logic ground	375	90	60 [1]
LineOut- to logic ground	375	90	60 [1]
LineOut+ to LineOut-	375	180	120 [1]
[1] A single excursion below this limit shall be allowed for a maximum of 0,75 ns			

7.1.6.2 Line Driver load

Each Line Driver load is a resistor with a d.c. impedance of 75 Ω ± 1% connected between LineOut and V_{dd}.

7.1.6.3 Line Driver coupling element

The Line Driver coupling element is an element that is capacitive at 20 MHz and has a maximum impedance of 10 Ω over a frequency range of 20 MHz to 500 MHz. Any self resonant frequency shall occur above 75 MHz. For example, this may be achieved with a 1 nF ± 20% capacitor which meets the Line Driver coupling element requirements.

7.3 Line segment termination

Line Segment termination is the electrical properties of the load on the end of the line segment opposite the end associated with the Line Driver.

Ideally a lossless, stubless transmission line that matches the media in the line exists between the port connector and a purely resistive matching terminating element. Ideally, the receiver chip connects with no

capacitance and no stub to this transmission line. It is necessary to approximate this ideal condition to avoid reflections on the line. Therefore a performance requirement requiring characteristic impedance levels at the line receiver port connector is used.

In order to accommodate the current levels and conformance voltage levels from the driver, the d.c. input characteristics for LineIn+ and LineIn- shall appear as a 75Ω ± 1% resistor connected to +3,3 V ±10% (see Figure 6). The line segment termination shall tolerate a direct short to -0,5 V for indefinite periods.

The characteristic impedance (Zo) measured into the LineIn+ and LineIn- pins of the connector with a Time Domain Reflectometer (TDR) shall meet the requirements in Table 10 including all time points affected by the connector and all associated electrical paths. The test environment shall reflect the conditions existing during operation.

Table 10 - Electrical requirements for line segment termination

Receiver port test configuration	TDR rise time max (ps)	Zo max (Ωs)	Zo min (Ωs)
LineIn+ to logic ground	375	90	60 [1]
LineIn- to logic ground	375	90	60 [1]
LineIn+ to LineIn-	375	180	120 [1]
[1] A single excursion below this limit shall be allowed for a maximum of 0,75 ns			

PROPOSAL 6 (Re-write of Dave Instone's proposal 96a158r0)

Dave Instone's proposal (96a158r0) rewrote section 7.5.1. SSA-PH is not written very definitively (SSA-TL and SSA-S2P/S3P are a little better). Definitive writing is an art, I have modified Dave's proposal to meet the definitive writing style and ask for your input, especially regarding changing "is" to "shall". I also changed the meaning of the last sentence as per my reflector note. The modified section is shown below. Revision marks indicate changes from Dave's proposal.

NEEDS DISCUSSION: Do we mark 20 MB/s only cables, 40 MB/s only cables or both? Current 20 MB/s cables are not marked. This would indicate that 40 MB/s capable cables should be marked, but this adds cost to the most commonly (hopefully) used cable. X3T10.1 decided not to mandate cable marking.

7.5.1 Test environment for port connection segments

The port connection segment test shall use point (M2) for the input signal and point (M3) for the output (see Figure 3, Figure 6 and Figure 10). The input signal at M2 shall be degraded using a signal degrader to match the minimum pulse mask for the driver (see 7.1). K28.5 characters (see SSA-TL) shall be used throughout this test. The output signal at M3 shall be measured and compared with the receiver pulse mask in 7.2 using the method defined in Annex D. Acceptable Port connection segments are those whose output signal does not intrude within the receiver pulse mask under the test conditions defined in clause 7.2.3.

If the Port connection segment is to be a restricted to a single speed connection, it need only be tested under that speed's conditions. A more general Port connection segment shall be tested using the pulse masks pertaining to both the 200 Mb/s and 400 Mb/s speeds.

The input slew rate used shall be no greater than the minimum slew rate shown in Table 6.

The driver test environment shown in 7.1.3 and the associated measurement procedure shall be used when setting the input signals applied at point M2. Once the input signals have been set, the port connection segment shall be connected in place of the driver test load and measuring equipment. The Port Connection Segment test load (see Figure 1) and the measurement procedure shown in 7.1.3.1 shall be used at point M3. The Port Connection Segment test load shall conform to the characteristic impedance requirements in

7.3 at its connector. The values of LR, LC, X and Y in Figure 1 shall be 75 Ω ± 1%, 3 pF, 5 cm ± 5 mm, and 5 mm ± 1mm respectively. The scope probe shall have capacitance of 3 ρF ±ρ 20%.

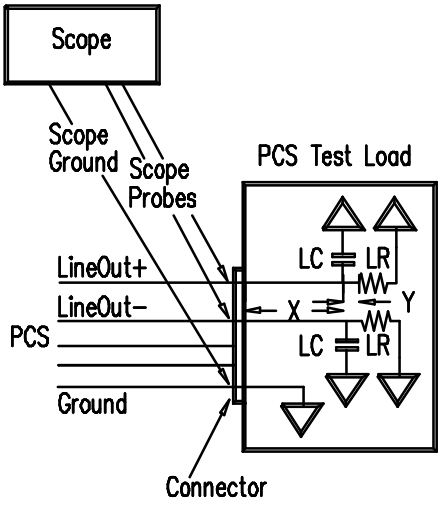

Figure 1 - Port connection segment test load

It is not required to vary the common mode or ground shift levels for the port connection segment tests.

Port connection segments shall be independently tested for each length differing by more than 2 cm or 2.5% of the longer length, whichever is larger. Independent tests shall also be performed for any change in the material, connector, or cable construction. Where the measurement of the physical length is impractical, then the length may be determined using TDR techniques and converted to a length using a conversion factor of 120 ps/cm.

7.5.2 Port connection segment marking

The hardware comprising the Port connection segment should be clearly marked to indicate the speeds for which it meets requirements. Physically inseparable Port Connection Segments (i.e. backplanes) need only be marked once.

PROPOSAL 7 (Impedance tolerance)

Two questions came up during my review regarding characteristic impedance:

a) 7.5 of SSA-PH2 states that the characteristic impedance is “150 +/- 10% ohms” (i.e. from 135 to 165). 7.5 of SSA-PH1 states the characteristic impedance is “150 +/- 10 ohms” (i.e. from 140 to 160). Which is right?
b) This impedance is “measured with a TDR with a 375 ps rise time”. Does this apply to 20 MB/s only cables? Should it also be measured with a rise time of 750 ps?

The plenary decided that the PH2 spec is correct in both these cases, and no changes are required.

PROPOSAL 8 (Move Data Rate clause to SSA-TL2)

Clause 6 (Data Rate) references ACK time-outs and frame format to come up with the data rate. The extended distance option (another SSA-TL2 concept further complicates this section. I propose:

a) Modify clause 6 as shown below and move it to SSA-TL2 prior to the existing clause 5.
b) Replace SSA-PH2’s clause 6 with the one shown below.

4 1/2 Data Rate (for SSA-TL2)

SSA links operate at a data rate of either 40 MB/s (i.e., 400 Mb/s) or 20 MB/s (i.e., 200 Mb/s) on the line.

The minimum overhead imposed by the frame format is 8 characters for a FLAG plus the control, address and CRC fields. If the link is being operated in full-duplex mode there is an additional overhead of 4 characters for the ACK and RR responses. With 128-byte data fields these overheads lead to the sustained data rates tabulated in Table 1. The equations used are as follows.

a) half duplex = 128/(128+8) * 40 MB/s (or 20 MB/s)

b) full duplex = 128/(128+8+4) * 40 MB/s * 2 directions (or 20 MB/s)

Table 1 - Sustained data rate and maximum distance

Nominal speed	Half-duplex	Full-duplex	Maximum distance at full speed	Extended distance option
40 MB/s	37,6 MB/s	2 x 36,6 MB/s	340 M	10 Km
20 MB/s	18,8 MB/s	2 x 18,3 MB/s	680 M	10 Km

These data rates assume that there are no transmission errors and that the transmitters and receivers have sufficient buffering to handle back-to-back frames.

The maximum distances allow the responses to be returned within the period of one frame, assuming a propagation velocity of 2×10^8 meters/second. Longer distances are possible at a reduced data rate. However the minimum 25μs ACK time-out imposes an upper limit of 2.5 kilometers in the standard distance mode. At this distance the maximum sustained data rate is approximately ¼ speed. The 100 us ACK time-out of the extended distance option increases the upper limit to 10 Km, while increased buffering allows 10 Km operate at full speed.

The transmit clock shall be accurate to ±250 PPM.

The receiver shall acquire bit synchronization from the transitions in the transmitted data. If an asynchronous sampling technique is used then the design shall take metastability into account.

6 Data Rate (for SSA-PH2)

SSA links operate at a data rate of either 40 MB/s (i.e., 400 Mb/s) or 20 MB/s (i.e., 200 Mb/s) on the line.

The transmit clock shall be accurate to ± 250 PPM.

The receiver shall acquire bit synchronization from the transitions in the transmitted data. If an asynchronous sampling technique is used then the design shall take metastability into account.

PROPOSAL 9 (Add a paragraph to the Jitter Nulling Annex)

Make the following changes to Annex D:

1) Change bullet a) from "... 4 to 6 bit times." to "... 4 to 12 bit times.".
2) Add the following two paragraphs prior to the list in Annex D.

   Continuous contiguous K28.5 characters contain a pattern that repeats every 20 bits. A stable display of all 20 bits is obtained by adjusting the scope trigger parameters. The trigger is then being taken from the same bit. Thickening of traces at the zero crossing point in the time dimension is caused by random jitter. Data dependent jitter and amplitude remain in the waveform for comparison against the pulse mask requirement on a bit by bit basis.

   The procedure for nulling intersymbol jitter may be performed as follows:

PROPOSAL 10 (Other changes made during the August working group)

Make the following changes:

1) 7.1.3.1 bullet a) - Remove (e. g. > 500 Mhz for 20 MB/s link)
2) 7.1.3.3 bullet a) - Remove (e. g. > 6 GHz for 4 V/ns)
3) 7.2.3, bullet a) - Remove (e. g. > 500 Mhz for 20 MB/s link)
4) 7.1.3.1 bullet b), and 7.2.3 bullet a) - Change "...25 data bit times..." to "...35 data bit times..."
5) Figures 6, 7 - Remove "Driver" and change "Node boundary" to "Driver" since the triangle is not the driver, the driver incised the terminating resistors and coupling capacitor.
6) Figure 10 - Replace V_{dd}s in receiver with V_{it}, move "Receiver" outside box, remove "Node Boundary", move "Driver" outside box.
7) 7.2.3 end of paragraph beginning "The amplitude..." - Change to "The validity of the degradation applied shall be checked by temporarily substituting..." to "The validity of the observed input conditions shall be checked by substituting..."
8) Table 9 - Change V_{dd} to V_{it}
9) Table 7 - Change four occurrences of "ms" to "ns".
10) Figure 38 - Change "28 AWG 7/34 tinned copper" to "26 AWG 7/34 tinned copper.
11) Table 6 - Change "Output voltage slew rate" to a minimum of "2.0 V/ns" (was blank) and a maximum of "5.0 V/ns" (was 4).

Sincerely,

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