Accredited Standards Committee
X3, Information Processing Systems

Doc: X3T10.1/96a142r2
Date: August 1, 1996
Project: X3T10.1/1146D
Ref Doc.: SSA-PH2 rev 1
Reply to: John Scheible

To: X3T10.1 Membership
From: John Scheible

Subject: SSA-PH2 changes proposal

BACKGROUND

Following the release of SSA-PH2 rev 1, several changes have been proposed on the reflector. This proposal pulls these changes together in a single proposal. Revision 1 of this proposal includes those changes agreed to at the June 1996 X3T10.1 plenary meeting and were included in SSA-PH2 rev 2.

Since that time, additional changes and corrections have been recommended, so I created revision 2 of this proposal and will recommend that it be included in SSA-PH2 rev 3 at the Ithica meeting. The revision marks are from revision 1 of this proposal to revision 2 (i.e., the recommenced changes for SSA-PH2 rev 3).

PROPOSAL 1 (Receiver does not have bypass capacitors) - No change from SSA-PH2 rev 2

Changes: When I created rev 1, I added bypass capacitors to both the receiver and driver. This is not correct, as the Receiver has no bypass capacitors. Make the following changes.

1) Figure 2 - Remove the bypass capacitors shown in both receivers.
2) Figure 10 - Remove the bypass capacitors shown in the receiver.

PROPOSAL 2 (Clarify Annex D requirements regarding Jitter)

Dave Instone did not like the way I changed the word can to shall (definitive writing does not like “can”) in the last sentence of paragraph 1 in Annex D (Jitter). Therefore, replace:

“This annex describes a method whereby the timings shall be applied to the K28.5 character when the predominant jitter is intersymbol jitter.”

with:

“This annex describes a method which enables these timings to be applied to the K28.5 character when the predominant jitter is intersymbol jitter.”

PROPOSAL 3 (Modify Table 6 to reflect both speeds)

Dave Instone notices that table 6 showed only a single column for “Output jitter” as 0,14 ns. This table should be changed as follows:

Replace the column with two columns for “Output jitter at 200 Mb/s (peak to peak) [1] (d)” with a maximum of “0,28 ns” and “Output jitter at 400 Mb/s (peak to peak)[1] (d)” with a maximum of “0,14 ns”.

PROPOSAL 4 (Modifications to the driver test procedure)

Dave Instone pointed out that rev 1 changes that were backed out should not have backed out the change from 2 pF to 1,5 pF which is restored in this proposal. Dave also pointed out the at line difference of 5 mm applied from the connector to the measurement point, and not connector to load resister.

Changes: Add...

a) Modify Figure 6 as shown below.

b) Change the first paragraph of 7.1.3.1 to...

Line drivers shall be tested using the test circuit shown in Figure 6. Line Driver measurements shall be made at the port connector. The distance between the port connector and the load resistance LR (labeled X in Figure 6) shall not exceed 5 cm. The distance between the measurement point (at the LR and MR junction) and the load resistance LR (labeled Z in Figure 6) shall not exceed 5 mm. The difference between the connector to measurement point distance (labeled Y in Figure 6) of the LineOut+ and LineOut- lines of the driver shall not exceed 5 mm. The resistance of the combined load resistance LR and measurement resistance MR shall be 75 Ω ± 2%. The connecting media shall meet the requirements in 7.5 for this test. The total additional capacitive load from the scope probing scheme between Line+ and ground and between Line- and ground at the port connector shall be 1,5 pF ± 20%. This capacitance includes the sensing probes and equipment added to enable probing. Additional discrete capacitors between the scope probes and the port connector ground may be needed. The load shall conform to the characteristic impedance requirements in 7.3 at its connector.

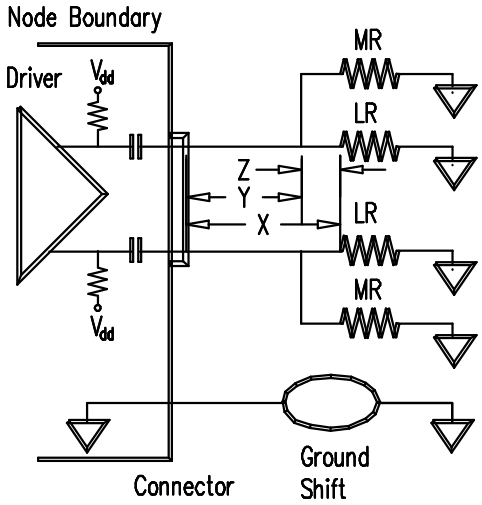

Figure 6 - Test environment for drivers

PROPOSAL 5 (Need words on Driver resister values)

This proposal incorporates the spec changes from Phil Murfet's proposal 96a153r0 entitled "Driver Line Termination". I noticed that Phil's proposal duplicated the same information for Line Receiver termination and Line Driver termination. I also noticed that we have a section 7.3 entitled "Line Segment termination", which is at the same level as the Line Driver and Line Receiver sections. In order to avoid duplicating information (and risking disagreement), I propose the following changes.

a) Modify "7.3 Line Segment termination" as shown below.

b) Remove "7.1.6 Line Driver termination",

c) Incorporate the old 7.1.6 into a new "7.3.1 Termination" as shown below,

d) Add a new section "7.3.2 AC coupling" as shown below.

We need discussion to verify this write-up is correct as it was difficult to alter a receiver write-up to be general for a receiver and driver.

The old section is shown on page 3 and the new section is shown on page 4 of this proposal.

(old section:)

7.1.6 Line driver termination

The LineOut+ and LineOut- lines of the Line Driver shall be terminated between the driver and the series capacitor with terminating resistors of 75 Ω ± 1% connected to the terminating voltage (see Figure 6). The series capacitor between the terminating resister and the connector shall have a value of TBD when measured with the measurement scheme specified in TBD.

7.3 Line segment termination

Line Segment termination is the electrical properties of the load on the end of the line segment opposite the end associated with the Line Driver.

Ideally a lossless, stubless transmission line that matches the media in the line exists between the port connector and a purely resistive matching terminating element. The receiver chip connects with no capacitance and no stub to this transmission line. It is necessary to approximate this ideal condition to avoid reflections on the line. Therefore a performance requirement requiring characteristic impedance levels at the line receiver port connector is used.

In order to accommodate the current levels and conformance voltage levels from the driver, the d.c. input characteristics for LineIn+ and LineIn- shall appear as a 75Ω ±1% resistor connected to +3,3 V ±10% (see Figure 6). The line segment termination shall tolerate a direct short to -0,5 V for indefinite periods.

The characteristic impedance (Zo) measured into the LineIn+ and LineIn- pins of the connector with a Time Domain Reflectometer (TDR) shall meet the requirements in Table 10 including all time points affected by the connector and all associated electrical paths. The test environment shall reflect the conditions existing during operation.

Table 10 - Electrical requirements for line termination

Receiver port test configuration	TDR rise time max (ps)	Zo max (Ωs)	Zo min (Ωs)
LineIn+ to logic ground	375	90	60 [1]
LineIn- to logic ground	375	90	60 [1]
LineIn+ to LineIn-	375	180	120 [1]
[1] A single excursion below this limit shall be allowed for a maximum of 0,75 ns			

(new section):

7.3 Line segment termination

Line Segment termination is the electrical properties of the load on each end of the line segment. Both the Line Receiver and the Line Driver contain terminating resisters. Only the Line Driver contains a series capacitor for AC coupling purposes.

7.3.1 Terminating resisters

Ideally a lossless, stubless transmission line that matches the media in the line exists between the port connector and a purely resistive matching terminating element of the Line Receiver and the resistive/capacitive load of the Line Driver. The receiver chip connects with no capacitance and a terminating resister stub to this transmission line. The Line Driver connects adds a series capacitor for AC coupling. It is necessary to approximate this ideal condition to avoid reflections on the line. Therefore a performance requirement requiring characteristic impedance levels at each port connector is used.

In order to accommodate the current levels and conformance voltage levels from the driver, the d.c. input characteristics for LineIn+ and LineIn- shall appear as a 75Ω ±1% resistor connected to +3,3 V ±10% on the driver (see Figure 6) and on the receiver (see Figure 10). The line segment termination shall tolerate a direct short to -0,5 V for indefinite periods.

The characteristic impedance (Zo) measured into the LineIn+ and LineIn- pins of the connector at both the Line Driver and Line Receiver with a Time Domain Reflectometer (TDR) shall meet the requirements in Table 10 including all time points affected by the connector and all associated electrical paths. The test environment shall reflect the conditions existing during operation.

Table 10 - Electrical requirements for line termination

Test configuration	TDR rise time max (ps)	Zo max (Ωs)	Zo min (Ωs)
LineIn+ to logic ground	375	90	60 [1]
LineIn- to logic ground	375	90	60 [1]
LineIn+ to LineIn-	375	180	120 [1]
NOTE[1] - A single excursion below this limit shall be allowed for a maximum of 0,75 ns			

7.3.2 AC coupling capacitors

The Line Driver shall have a series capacitor between the terminating resister and the connector. The capacitor shall have a self resonant frequency greater than 100 MHz and a series impedance of less than 5 Ω at 400 MHz.

Sincerely,

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