200/400 Mbit/s SSA PHYsical Layer Device

Functional Test Report

Revision 1.4

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REVISION HISTORY

Revision	Data	Comments
0.1	2/18/96	initial draft distributed to Adaptec BTC internal only, contained MS-WORD PRANK virus
1.2	2/19/96	fixed PRANK virus and some editorial corrections, copy sent to IMD
1.3	2/23/96	corrected slew rate section 2.0 meter cable fall time error, overhauled eye diagram section, added additional information to bit error rate section, added trace impedance plots in appendix, modified statements in scope and summary sections, removed Adaptec Confidential from footer for potential distribution outside Adaptec/IBM
1.4	2/27/96	added 20MB/s eye diagrams noted 20MB/s error rate testing

1. Scope

The purpose of this report is to illustrate the preliminary test data from the 200/400 Mbit/s SSA PHYsical Layer Device evaluation performed at the Adaptec Boulder Technology Center (BTC). Testing being done at BTC is primarily for verification of the protocol interface and general SSA functionality in anticipation of integrating PHY with the Keystone SSA Protocol Controller. The test configuration and setup is described in this document along with basic functional and parametric measurements acquired in the lab.

The data presented in this report is preliminary and based on limited testing. This report is not intended to be a definitive test summary or statement regarding SSA40 physical layer requirements. It is also not intended to represent a formal functional test report required for full qualification of the PHY design. At present, the plan is to have the primary PHY design compliance testing and qualification performed by IBM.

2. Summary

To this date all preliminary testing indicates the PHY is meeting functional requirements. The SSA 40MB/s analog signal integrity is encouraging with various cable lengths tested, from 0.3 meters to 20 meters.

3. Reference Documents

- Adaptec/IBM 200/400 Mbit/s SSA PHYsical Layer Device Specification
- X3T10.1 SSA-PH1 SSA Physical Layer 1 Specification
- Adaptec PHY Test Board schematics, file name: V1_22C.SCH, 1/22/96

4. Test Configuration

The test configuration consists of an Adaptec designed PCBA (PHY Test Board), DC linear power supplies for providing 5.0V, 3.3V and 2.0V, a Hewlett-Packard HP16500B logic analyzer with one timing/logic analysis card and one pattern generator card (16552A), and a Tektronix TDS684A digital sampling oscilloscope.

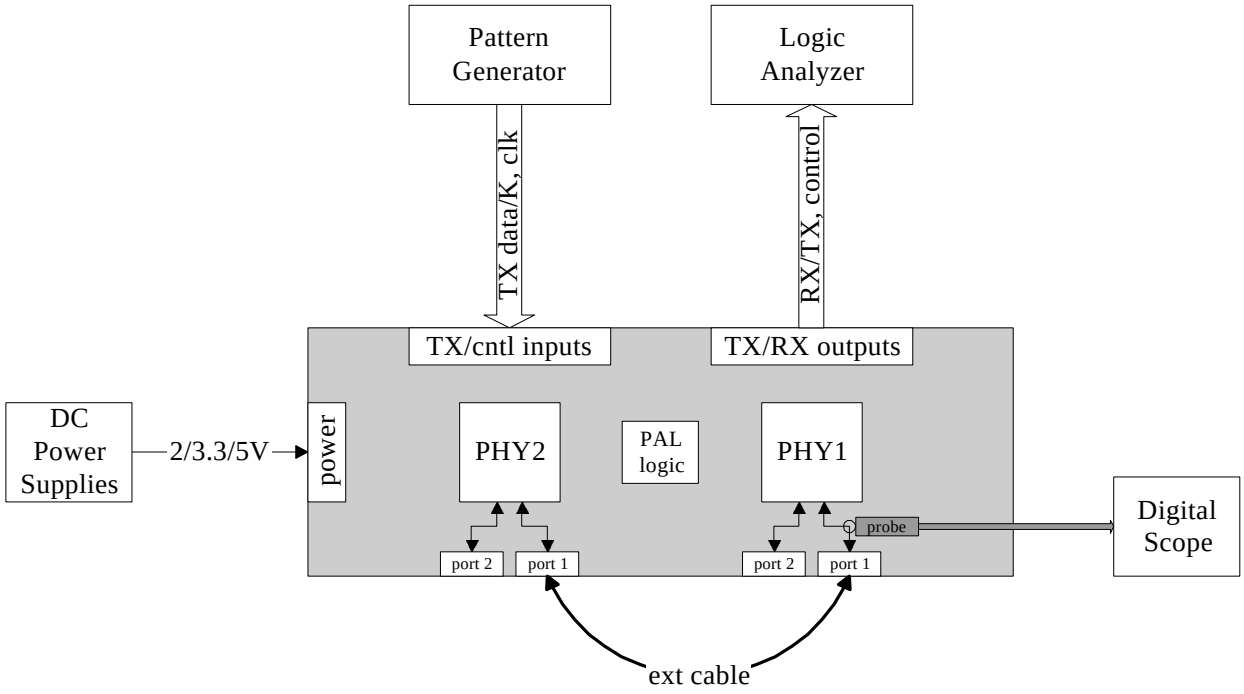

Figure 1: PHY Test Configuration

All testing to date has been done at room ambient, approximately 23 degrees C. The PHY power, 3.3V and 2.0V, was provided by independent external dc power supplies. An external 5.0V source was provided to power the PAL circuits. Preliminary current measurements were read from the power supply's display.

4.1 PHY Test Board

The PHY Test Board consists of two PHY test circuits. The two PHYs are essentially independent with the exception of sharing a common 50.0MHz clock, reset, transmit mode control signals and 3.3V/2.0V power.

The board allows for a single HP16552A pattern generator module (40 signal output channels) to drive four independent TX data ports. It is also provides the 50.0MHz clock and PHY reset. Each transmit port consists of an 8 bit data bus and a 1 bit K character. There is one set of transmit mode bits (receive speed, transmit speed, wrap mode) that are shared between the four TX ports. The mode bits are multiplexed with the lower order TX data bits on board using a 5ns PAL22V10. Multiplexing follows the PHY TX port timing protocol which is controlled by the TX type bit output from the PHY.

All PHY digital outputs (RX data and control, TX type, etc.) are routed to probe headers for logic analysis.

4.2 SSA Signal Routing

The SSA differential analog signals are routed on the outer layer which is adjacent to an inner GND plane. The nominal single-ended impedance of the SSA traces is 75 ohms. Each differential pair is signal length matched and separated from adjacent conductors by greater than 0.1 inches. Each SSA port has a set of probe sockets routed in-line with the SSA signal trace, ie. no routing stubs created. For each signal probe socket there exists an adjacent GND socket spaced 0.1 inches from the signal socket. On board external SSA connectors (one per port) allow testing of different SSA cable lengths for port to port communication.

The following figure is a section of the top component layer of the PHY Test Board. The view includes the outer layer copper, pads and silk screen for one of the PHY circuits. The center rectangle is the PQFP100 PHY pad. The outline/pads to the upper left are the external 9-pin Micro-D SSA connectors. The features that show two holes with a circle around them near the PHY pad are the scope probe points for the SSA signals. Inside each circle is an SSA signal/GND pair. The discrete pads (SMT 1206) around the PHY are for external VCO discrete components and potential SSA series/ac termination discrete components. No source or ac termination components were populated. A 0-ohm resistor was installed in the series termination pad. In this layout the bypass/de-coupling capacitors and SSA receiver termination resistors are placed on the back side directly under the respective PHY pads.

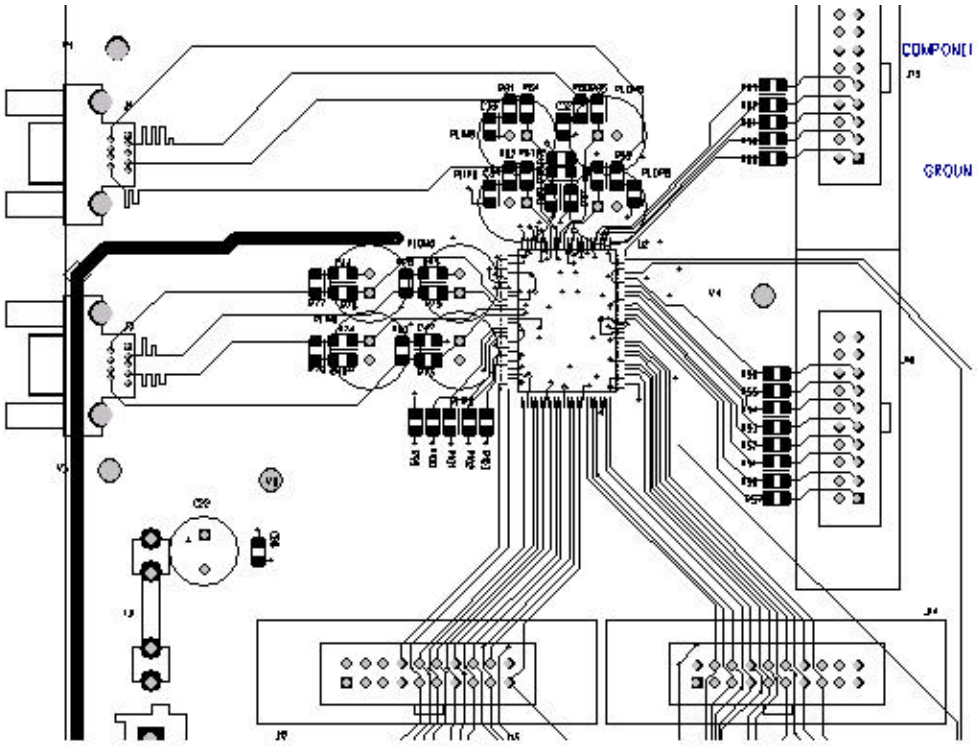

Figure 2: PHY PWB Layout: SSA routing

4.3 SSA Signal Probing

The figure below shows a dimensional diagram of the SSA signal routing and probe positioning used for the SSA signal measurements.

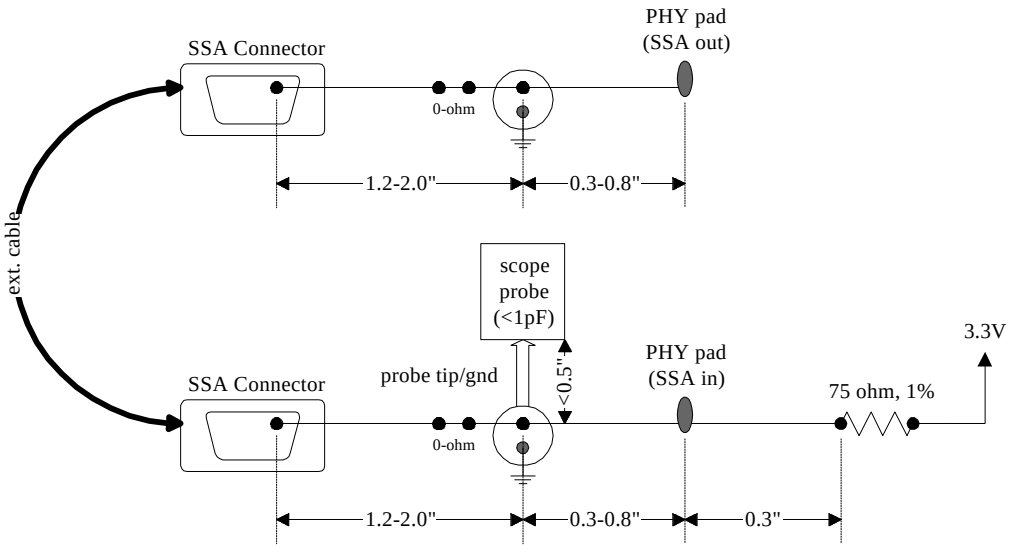

Figure 3: SSA Signal Routing/Probing

4.4 TDS 684A Scope Configuration

The analog SSA differential signals are monitored using the TDS 684A scope. The TDS 684A is a 1GHz, 5G samples per second digitizing scope which is capable of digitally processing the sampled data. This allows for channel waveforms to be displayed as mathematical functions, ex. channel 1 - channel 2. Tek P6245 TDS500/600 active probes are used for all SSA analog measurements. The probe tip connects directly to the on board signal socket and the probe ground wire is approximately 0.5 inches connecting to the adjacent GND socket.

P6245 10x active probes

- < 1pF
- 1M ohm
- 1.5GHz bandwidth
- 40V input peak max

The scope triggering and setup is important to note for qualification of the data measurements shown in this section. The scope probes were configured as channel 1 (Ch1) = receive positive input signal, and channel 2 (Ch2) = receive negative input signal.

Triggering

- Channel 1 positive edge (no means of triggering off the differential CH1-CH2 signal and 50MHz clock triggering did not provide a reference to the SSA serial link.)
- Auto trigger, 50% level which was typically the dc average of the differential signal, ie. 2.7 - 2.8V.

5. Power/Analog Data

The power consumption was measured using the supply's built-in current meter. The following preliminary current measurements were made on test board #1. Both ports were active and transmitting/receiving data. The numbers shown represent the average power of each PHY device.

TX/RX Speed	mode	TX characters	I(3.3V)	Power
all inputs fixed level	no clock input	n/a	126mA	416mW
20MB/s	wrap mode	DIS and/or FLAG	191mA	630mW
20MB/s	non-wrap mode	DIS and/or FLAG	191mA	630mW
40MB/s	wrap mode	DIS and/or FLAG	233mA	769mW
40MB/s	non-wrap mode	DIS and/or FLAG	240mA	792mW

Table 1: 3.3V Power Consumption

The PLL/VCO analog signals were measured as follows:

Signal	voltage	current
VREF input	1.95V	< 3.0mA
VCO_CNTL	1.6V with < 100mV ripple	
REXT (4.91K resistor)	1.95V	
VCO-VDD	3.3V	

Table 2: PLL/VCO V/I Measurements

6. Protocol Interface Data

The following logic analyzer waveforms where captured in timing mode (4ns/sample). For the protocol interface tests a continuous stream of K characters was transmitted. It was verified the receiver could only byte synchronize on DIS and FLAG characters as specified. For the tests shown TX data port 1 = FLAG character (0x13C), TX data port 2 = DIS character (0x13D). The PHY port 1 and port 2 were connected through a short (<1.0m) cable for the protocol test data shown.

Signal name format: PxTy_z, PxRy_z
x = PHY number (1 = U1, 2 = U2)
y = port number (1 or 2) where T is TX port, R is RX port
z = signal type where
1) D = 9 data field K, D7, …, D0
2) T = type bit
3) C = code violation bit

Transmit mode decode:
The transmit mode bits are valid 2 clocks after the sampling of the TX type bit active 'high'. The bit organization is as follows:
TX data bit 2: RX speed, 1 = 40MB/s, 0 = 20MB/s
TX data bit 1: TX speed, 1 = 40MB/s, 0 = 20MB/s
TX data bit 0: Wrap mode, 1 = wrap, 0 = normal

6.1 Protocol Interface AC Characteristics

The pattern generator / PAL logic signal outputs meet the input requirements outlined in the PHY specification. The 50.0MHz SYSCLK at the PHY input pad met all timing characteristics required. The pattern generator clock slew rate at the PHY was adjusted to the minimum 1V/ns. This equates to a 1.2ns maximum rise/fall time between the 0.8V and 2.0V input switching region.

All PHY digital outputs were within the proposed 13ns clock to output delay requirement with plenty of margin. The measured delay relative to the rising edge of SYSCLK was between 8.6ns and 9.2ns. The signal measurements were made at the load end point of the signal trace. In this test setup the TX/RX output load includes 2.5-3.0 inches of trace, the logic analyzer pod probe and the on board PAL. The total estimated capacitive load of the test setup is between 20-30pF which is more than double specified 10pF maximum.

6.2 20MB/s Wrap Mode

The following figure shows the PHY TX and RX ports in 20MB/s wrap mode synchronized. The O cursor shows the RX status cleared indicating no fault, error or re-sync conditions. The TX type bit duty cycle is 4 clocks inactive (4 data/K characters) for every 10 clocks, ie. every 200ns. This is consistent with the specified functionality of the TX/RX port in 20MB/s mode where TX/RX transfer rate is 50MB/s and the SSA link transfer rate is 20MB/s, ie. a 5:2 cycle to character ratio. The RX type bit modulation alternates 2 on : 1 off, 1 on : 1 off.

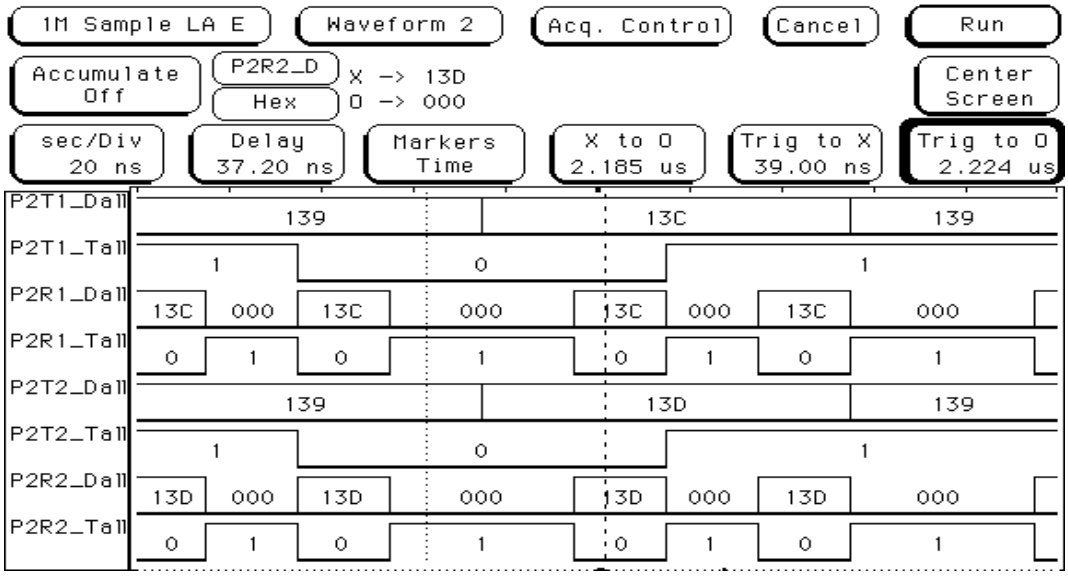

Figure 4: Protocol Waveform: 20MB/s wrap mode synchronized

6.3 20MB/s Normal Mode

The following figure shows the PHY TX and RX ports in 20MB/s normal mode coming out of a reset condition. The X cursor shows the RX status indicating a code violation and RESYNC bit set. The code violation status will persist for up to 200 characters out from reset then go away once the port is fully synchronized. The O cursor shows the receive data character = 13C, ie. FLAG.

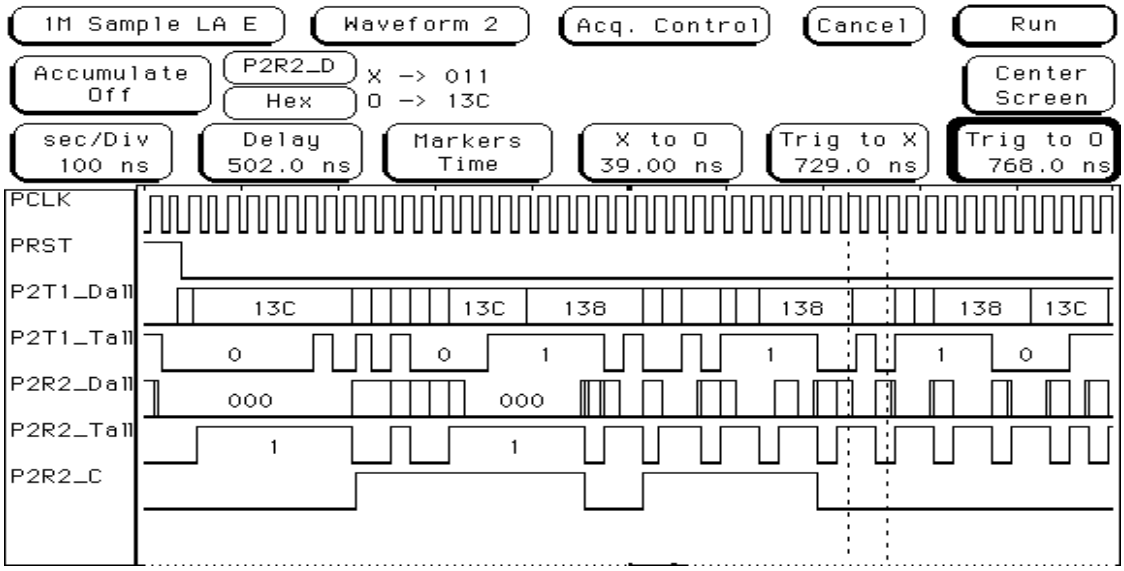

Figure 5: Protocol Waveform: 20MB/s normal mode from reset

6.4 40MB/s Wrap Mode

The following figure shows the PHY TX and RX ports in 40MB/s wrap mode synchronized. The TX and RX type bit duty cycle is 4 clocks inactive (4 data/K characters) for every 5 clocks, ie. every 100ns. This is consistent with the specified functionality of the TX/RX port in 40MB/s mode where TX/RX transfer rate is 50MB/s and the SSA link transfer rate is 40MB/s, ie. a 5:4 cycle to character ratio. Note the TX mode bits are valid 2 clock after the active TX type bit. RX status is aligned to the RX type bit active.

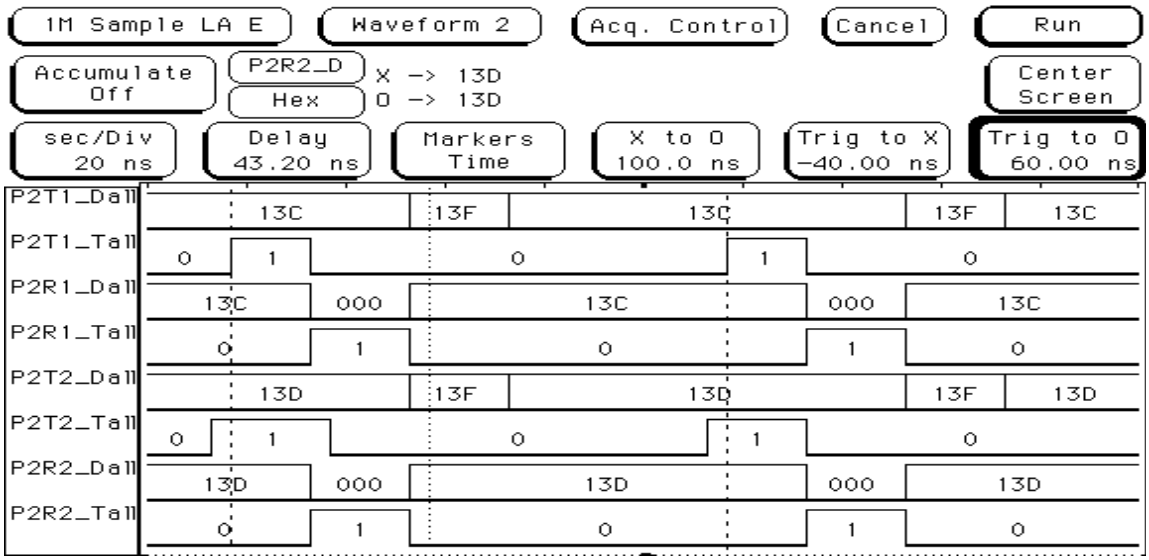

Figure 6: Protocol Waveform: 40MB/s wrap mode synchronized

6.5 40MB/s Normal Mode

The following figure shows the PHY TX and RX ports in 40MB/s normal mode coming out of a reset condition. The X and O cursors show the resync status and RX data character respectively. Note the type bit modulation is varying initially.

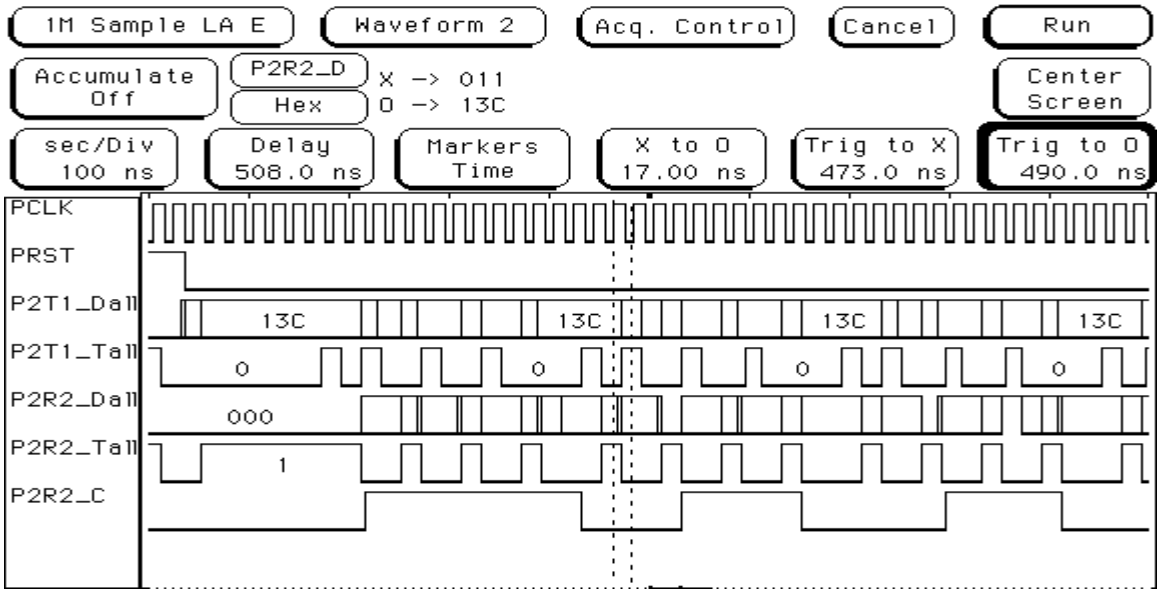

Figure 7: Protocol Waveform: 40MB/s normal mode from reset

The following figure shows the PHY TX and RX ports in 40MB/s normal mode synchronized. The type bit modulation has stabilized to a 1 on : 4 off duty cycle.

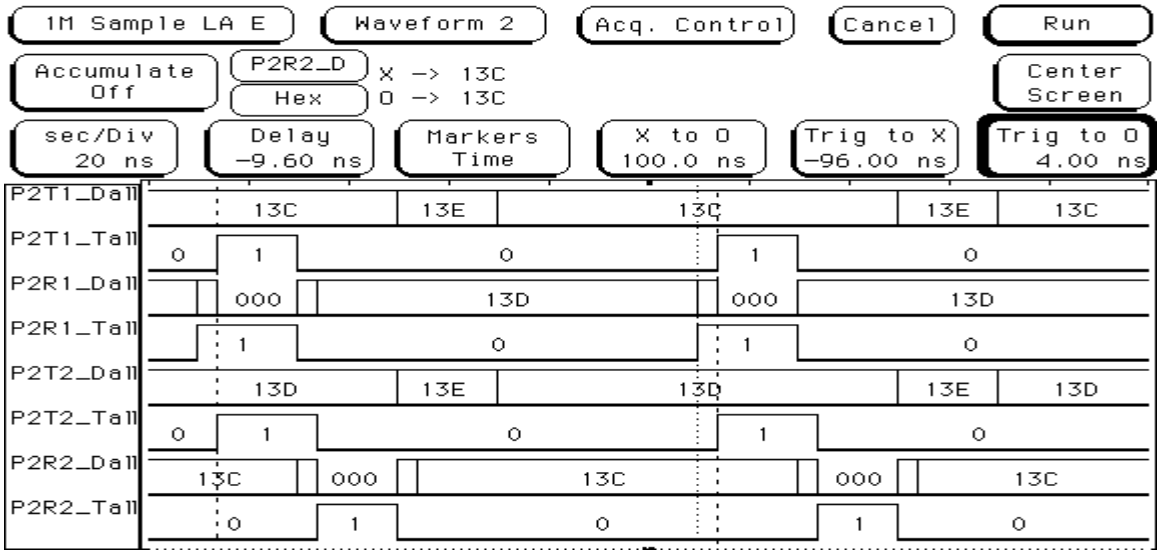

Figure 8: Protocol Waveform: 40MB/s normal mode synchronized

6.6 RX Status

1. Port receive status was verified valid on the RX data bus during the RX status phase as indicated by the RX type bit being logic high.

2. Preliminary testing was done for checking the differential driver line fault status bit. If the SSA port transmit lines are not terminated, ie. the cable is not connected the bit would be set.

3. Preliminary testing was done for checking the code violation output and status bit. If an invalid character is decoded, ie. removing the cable or by sending non-synchronizing characters after PHY reset, the bit would be set.

4. Preliminary testing was done for checking the RE_SYNC character re-synchronization status. The RE_SYNC bit was observed to be active for one status cycle after, a) a PHY reset occurred and the receiver establishes synchronization from a DIS or FLAG comma character, or b) after certain situations of code violation errors (typically multiple grouped errors) which were observed with long cables at 40MB/s. RE_SYNC doesn't occur for single random code violation errors.

7. SSA Link Interface Data

The following scope plots were primarily done on PHY test board #2. Both PHY test board #1 and #2 exhibited similar functionality and signal integrity. The plots are measured from the PHY2 port 1 receiver side connected to the PHY1 port 1 transmitter through various external shielded cable lengths as described in each figure.

The SSA waveform measurements were made with a continuous fixed DIS character (K.28.5) transmitted on all ports as described in section 7.1.3.1 of the SSA PH1 specification. The eye diagram measuremens were made with random data patterns transmitted, described in greater detail in the eye diagram section.

All data measured is at the receiver probe end, with far end 75 ohm termination only[1]

Scope cursor/measurement data

- The data shown in the upper right corner shows the signal voltage and time base data relative of the cursor positions marked as the 'X' where the cursor intersects the signal waveform.
- Where shown the signal average/mean is to the right of the plots which was selected from the measurement menu.
-

7.1 Wrap Mode

The following shows the differential pair with the port in wrap mode. In wrap mode the driver fixes the link in the logic zero state. Logic zero state is defined as line + = 10.0ma (CH1 = 2.44V) and line - = 0.0mA (Ch2 = 3.22V). The difference voltage = 0.78V which is approximately = 10.0mA * 75 ohm termination.

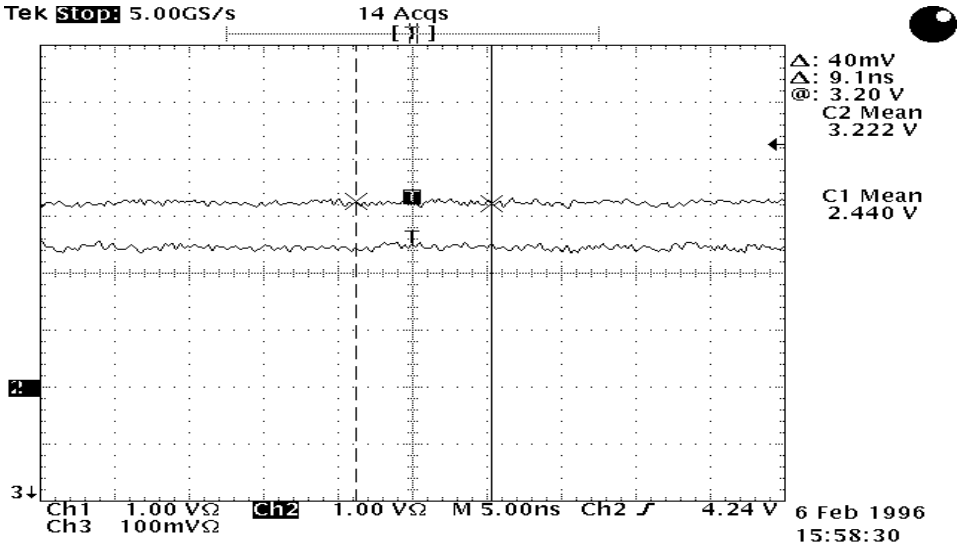

Figure 9: SSA Waveform: Link driver in wrap mode

[1] The PHY as designed does not support a 20mA driver for near end termination.

7.2 20MB/s Link

The figure below shows a single trigger 20MB/s DIS character. The CH1 and CH2 signals are shown individually with the equivalent vertical offset and positioning. The cable used was 2.0 meters.

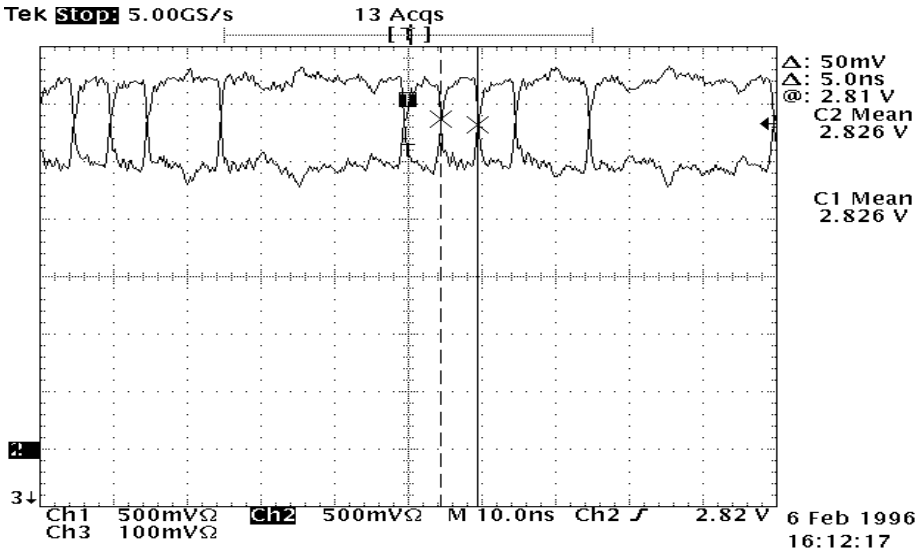

Figure 10: SSA Waveform: 20MB/s, single trigger, 2.0 meter cable

7.3 40MB/s Link

For all of the following 40MB/s measurements PHY test board #2 was used. This board is what was shipped to IBM. PHY1 TX port 1 is transmitting to PHY2 RX port 1. All measurements are made at the PHY2 RX port 1 probe sockets.

7.3.1 Single Trigger Waveforms

The following figures show the single triggered link signals for three different cable lengths, 0.6, 2.0 and 20.0 meters. The vertically centered waveform is the mathematical sum of Ch1 - Ch2. The waveforms in the upper part of the display are the individual over lapped differential signals with zero vertical offset/position.

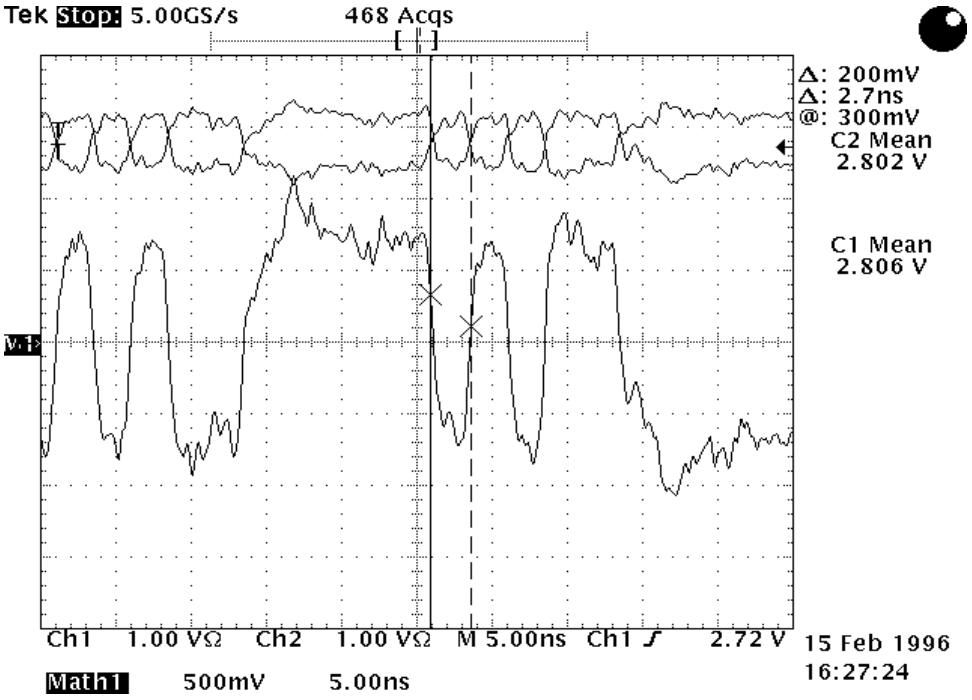

Figure 11: SSA Waveform: 40MB/s, single trigger, 0.6 meter cable

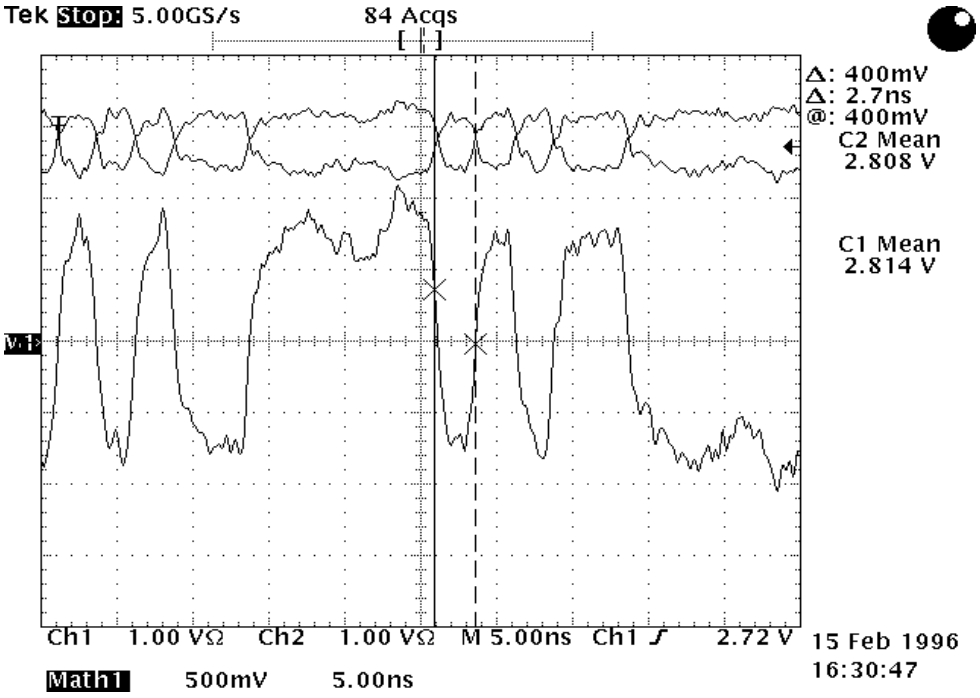

Figure 12: SSA Waveform: 40MB/s, single trigger, 2.0 meter cable

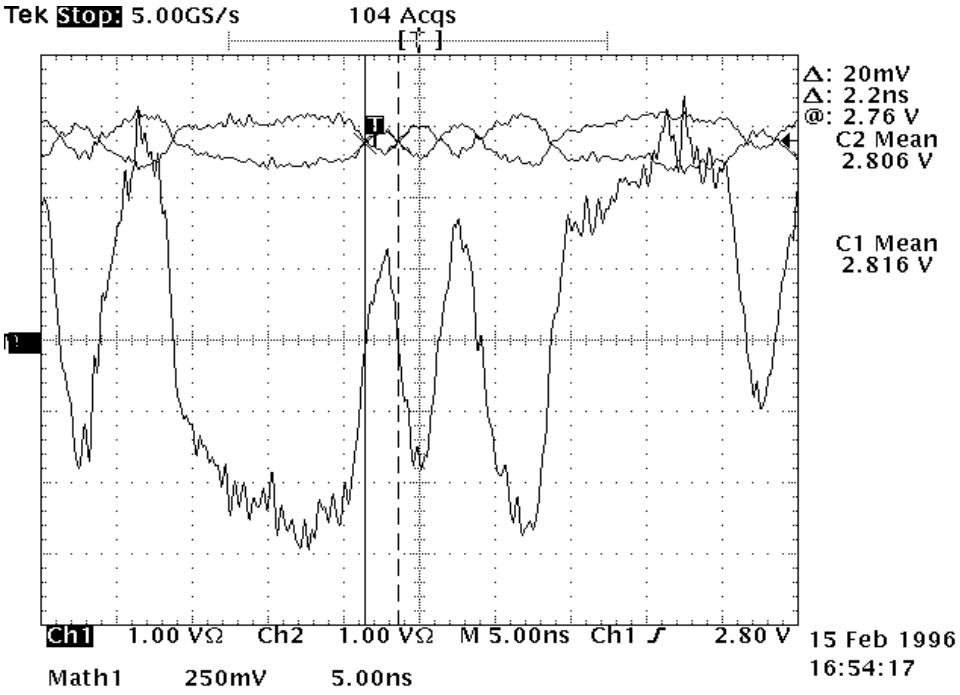

Figure 13: SSA Waveform: 40MB/s, single trigger, 20.0 meter cable

7.3.2 Signal Slew Rate

The figures in this section show the measured rise and fall times of the individual signal line crossing the mirror plane threshold, ie dc mean of the signal. These are not intended to be “true” driver slew rate measurements because the probes are at the receiver end and the measurements are not necessarily all done at +/- 200mV.

In summary the measurements show the following:

rise time, 2.0 meter	= 196mV/490ps or 0.40V/ns
fall time, 2.0 meter	= 202mV/170ps or 1.2V/ns
rise time, 20.0 meter	= 102mV/290ps or 0.35V/ns
fall time, 20.0 meter	= 100mV/330ps or 0.30V/ns

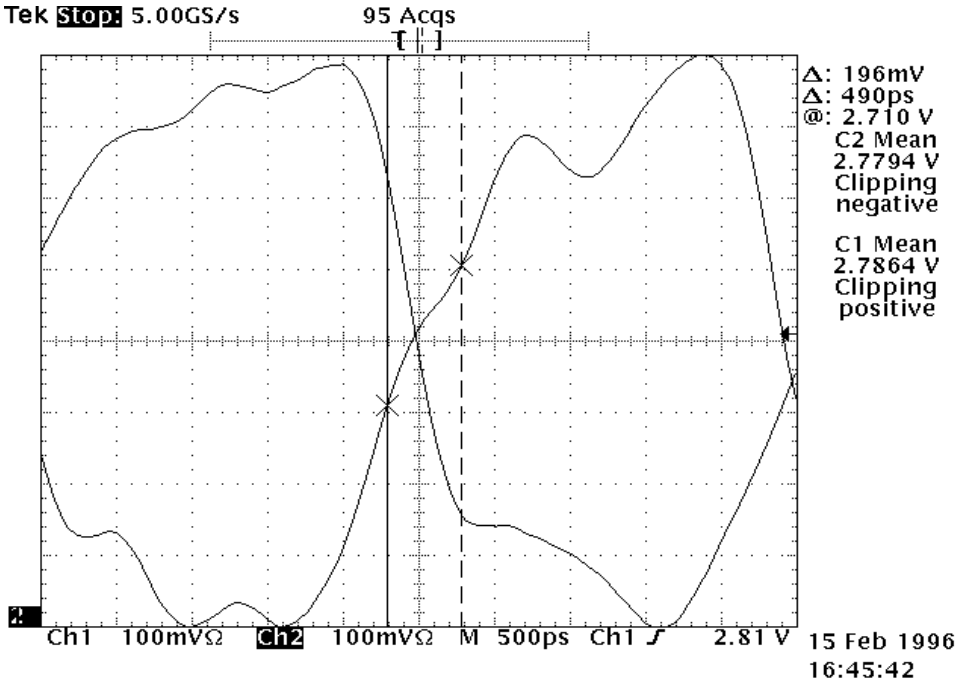

Figure 14: SSA Waveform: 40MB/s, rise time, 2.0 meter cable

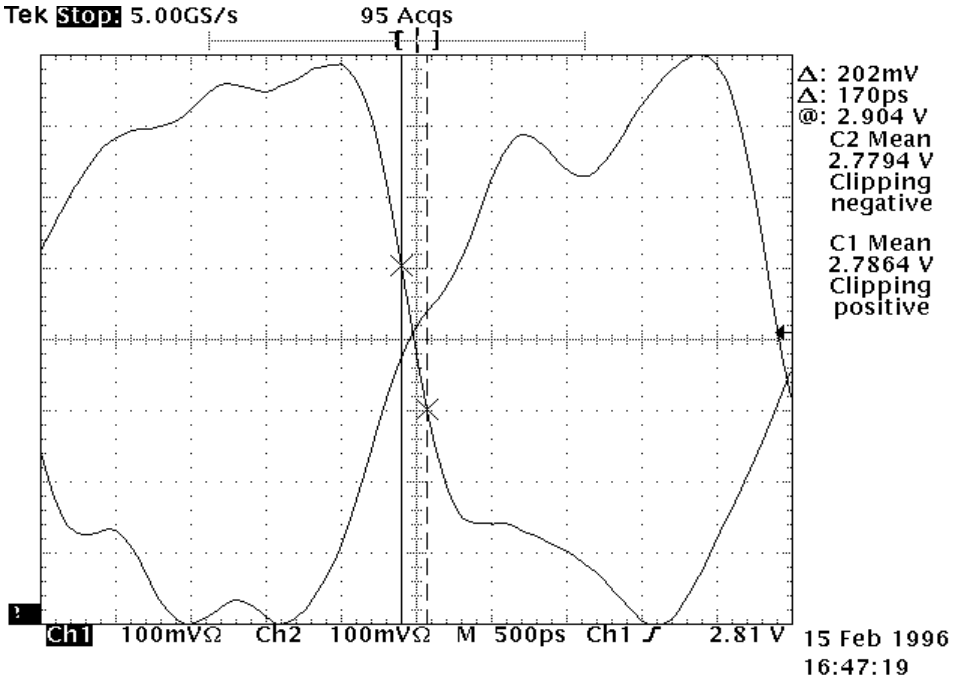

Figure 15: SSA Waveform: 40MB/s, fall time, 2.0 meter cable

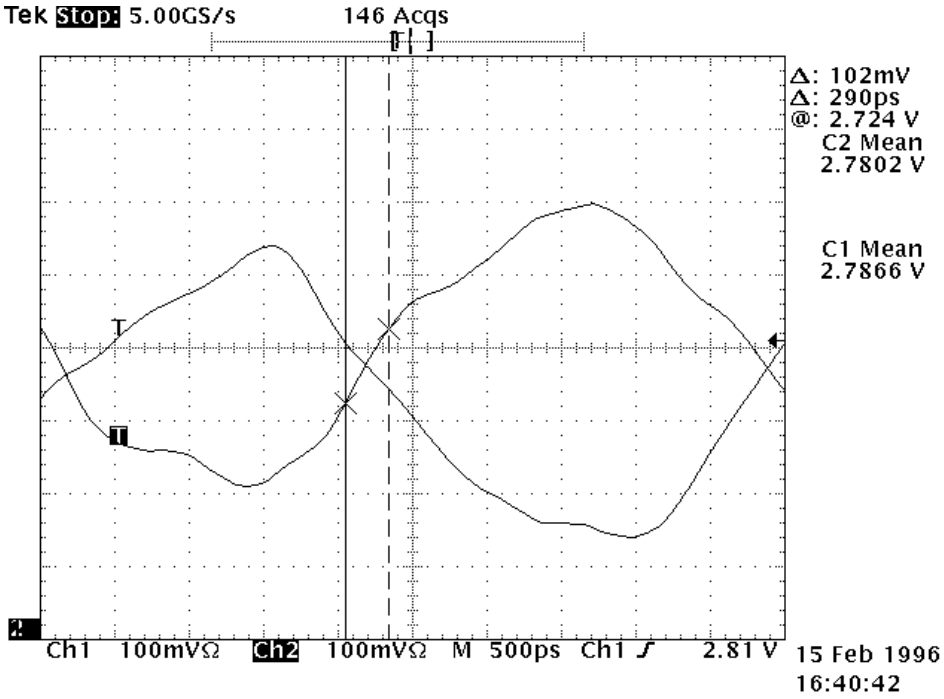

Figure 16: SSA Waveform: 40MB/s, rise time, 20.0 meter cable

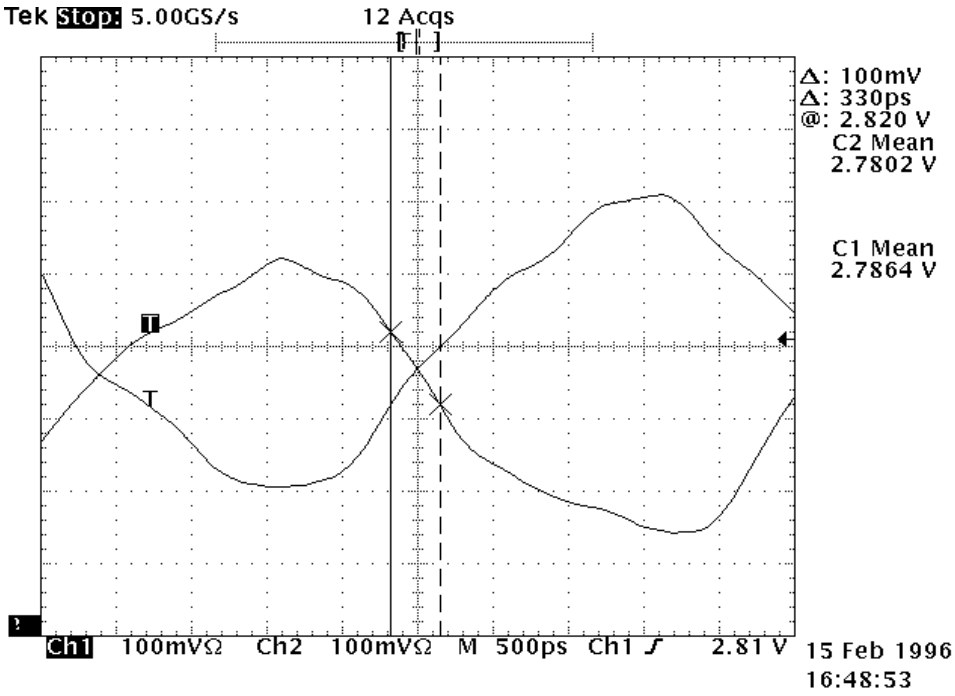

Figure 17: SSA Waveform: 40MB/s, fall time, 20.0 meter cable

7.4 Receiver Eye Diagrams

The figures in this section show a single waveform that is the mathematical sum of Ch1 (line +) minus Ch2 (line -). All eye diagram plots are displayed with a 10.0 second persistence on the scope.

The data pattern being transmitted contains valid sequences of 8B/10B characters (including comma characters) as noted in the SSA PH1 Spec rev 6b, section, 7.2.3, Test Conditions For Receivers. The eye diagrams below represent the full range of valid data and K characters, arranged in a sequence that is transmitted in a pseudo-random order. The ordering varies due to the TX type mode modulation which the HP pattern generator is unaware of.

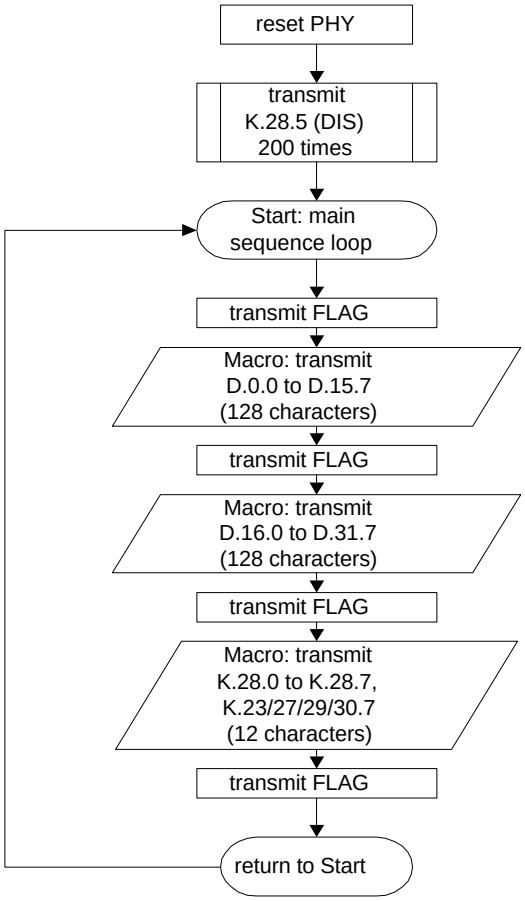

Figure 18: Transmit Pattern Sequence for Eye Diagrams

7.4.1 20MB/s

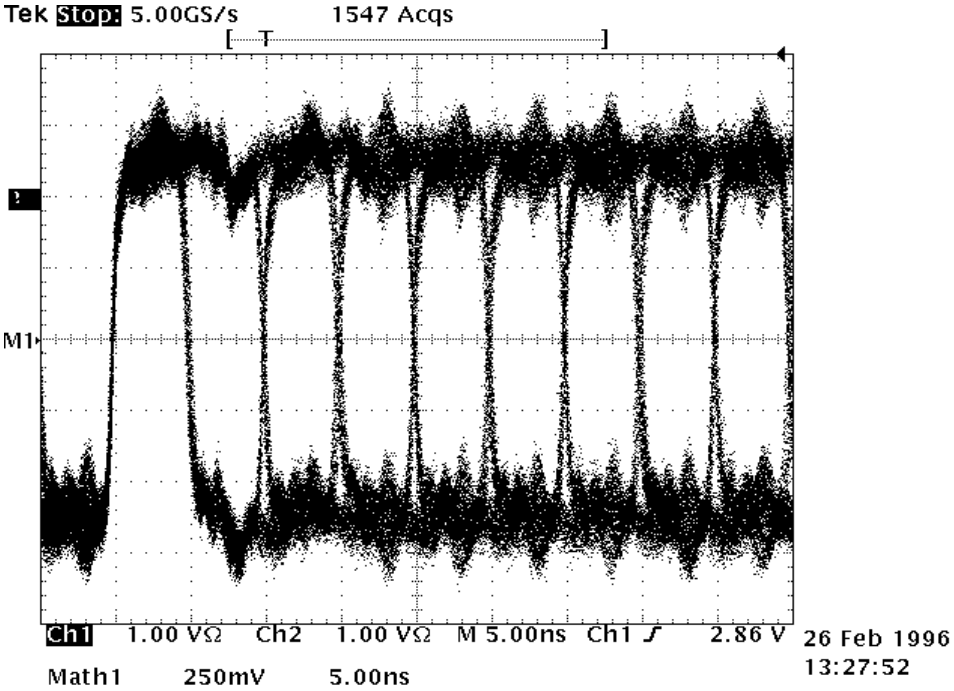

Figure 19: SSA RX Eye Diagram: 20MB/s, 0.6 meter cable

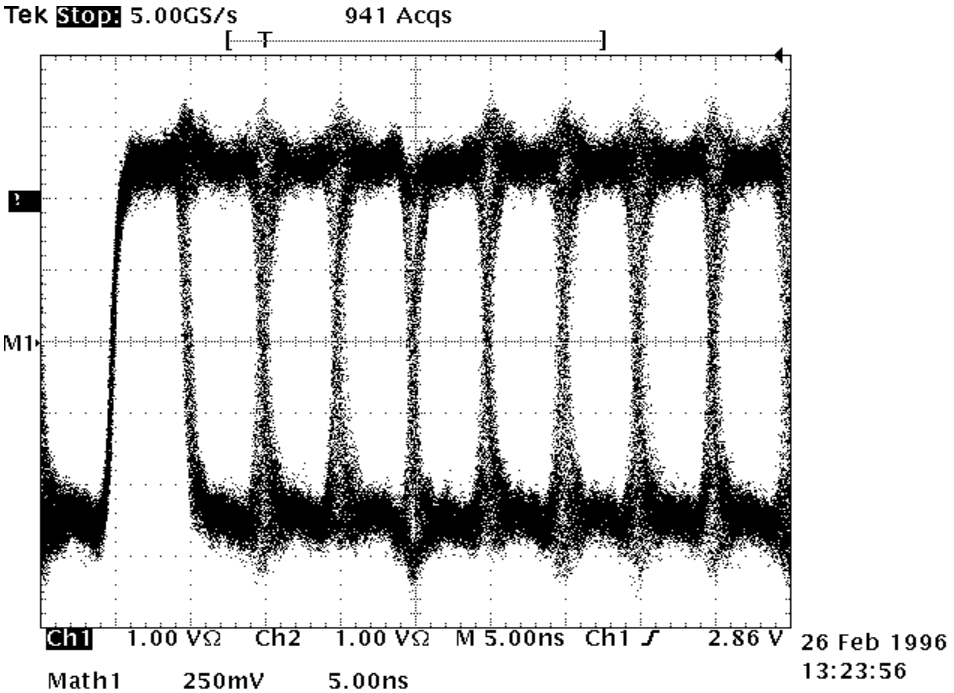

Figure 20: SSA RX Eye Diagram: 20MB/s, 2.0 meter cable

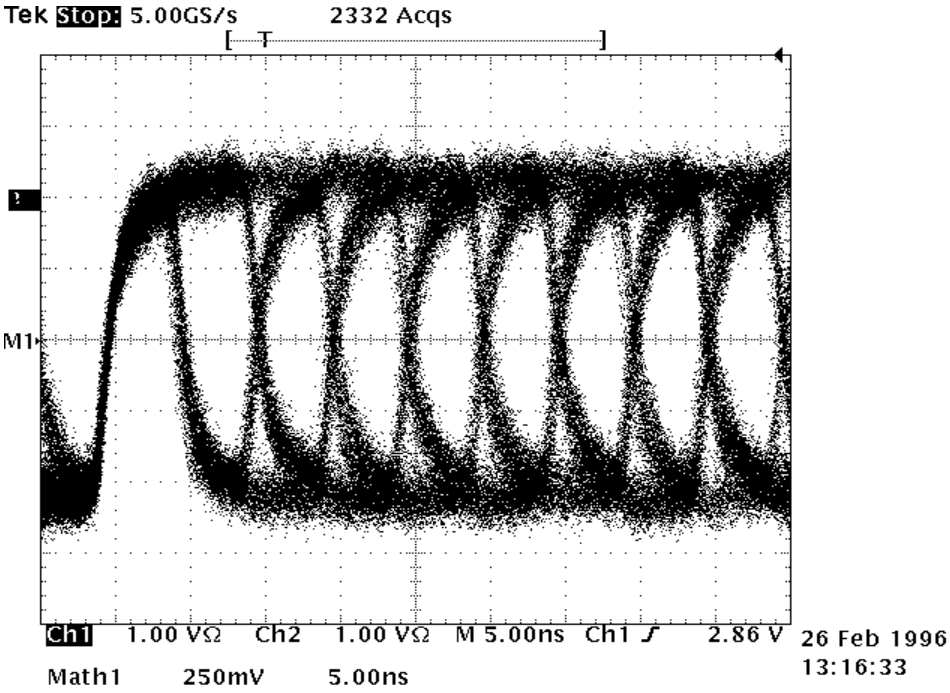

Figure 21: SSA RX Eye Diagram: 20MB/s, 20.0 meter cable

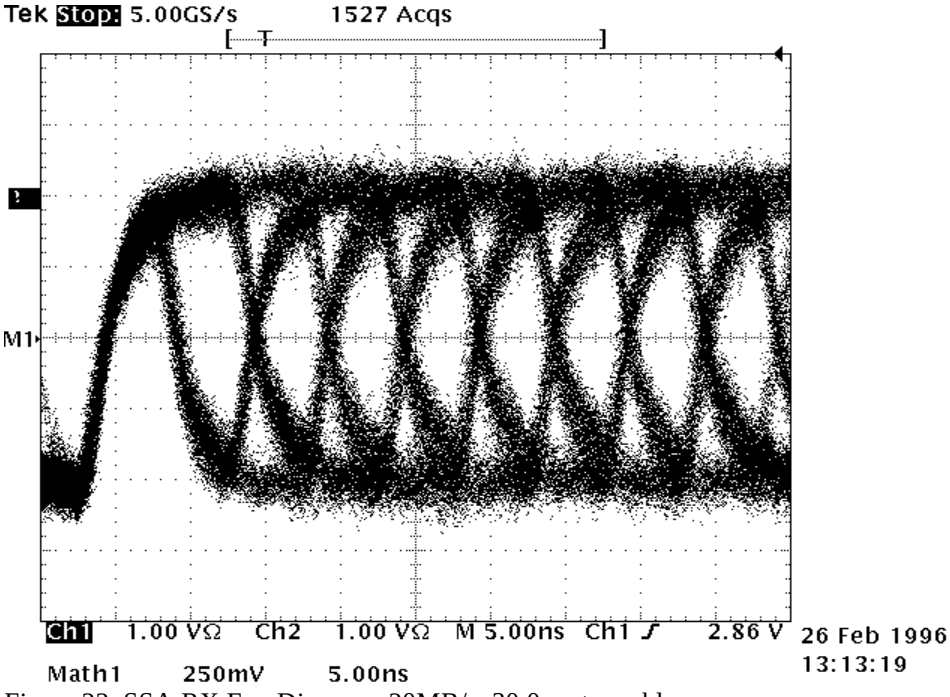

Figure 22: SSA RX Eye Diagram: 20MB/s, 30.0 meter cable

7.4.2 40MB/s

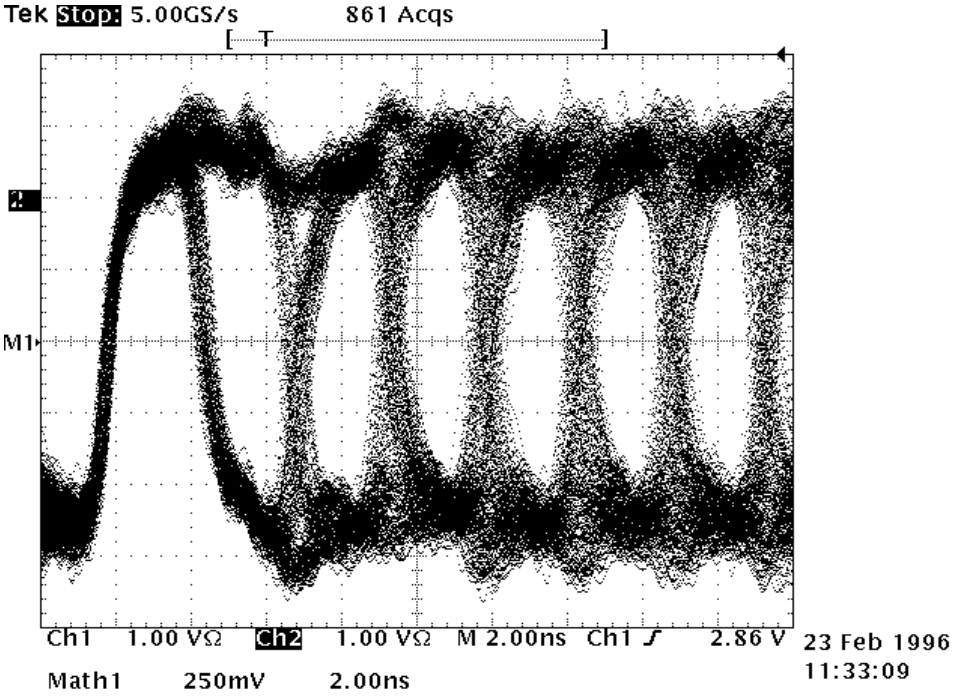

Figure 23: SSA RX Eye Diagram: 40MB/s, 0.3 meter cable

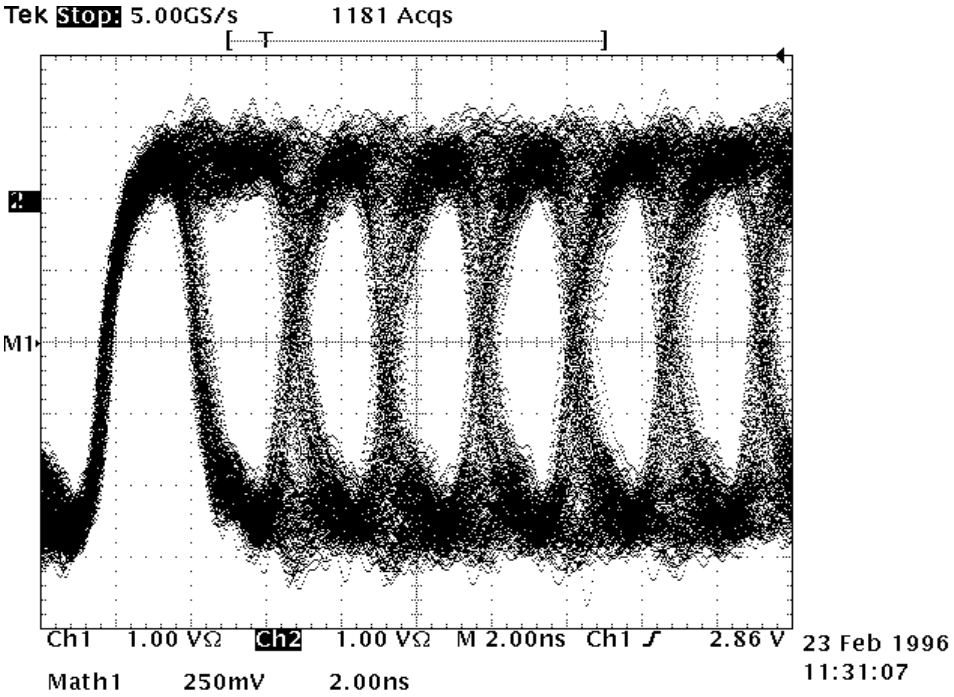

Figure 24: SSA RX Eye Diagram: 40MB/s, 2.0 meter cable

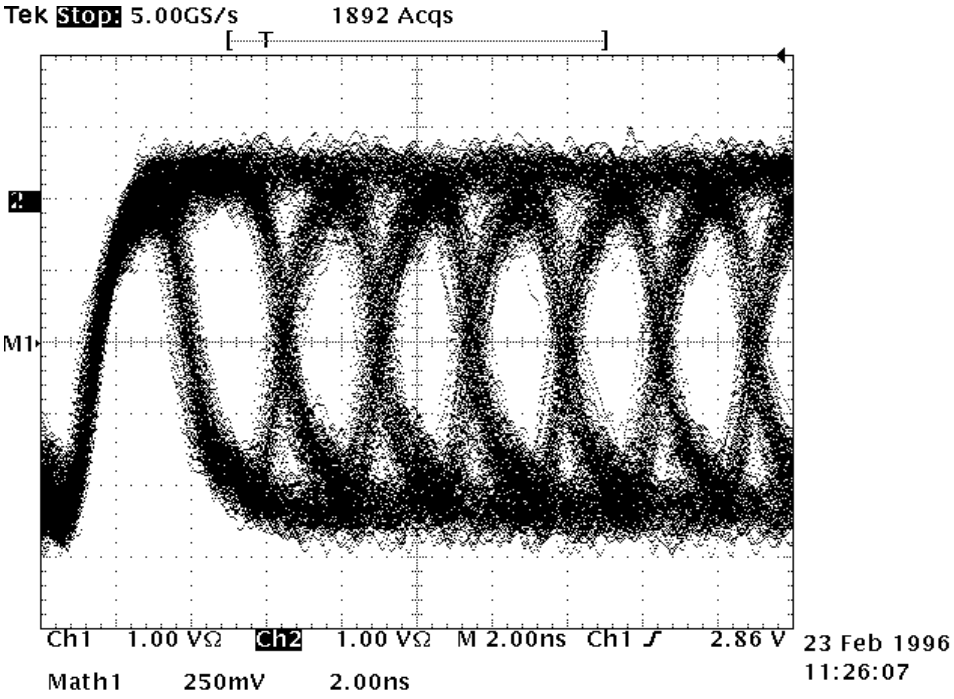

Figure 25: SSA RX Eye Diagram: 40MB/s, 10.0 meter cable

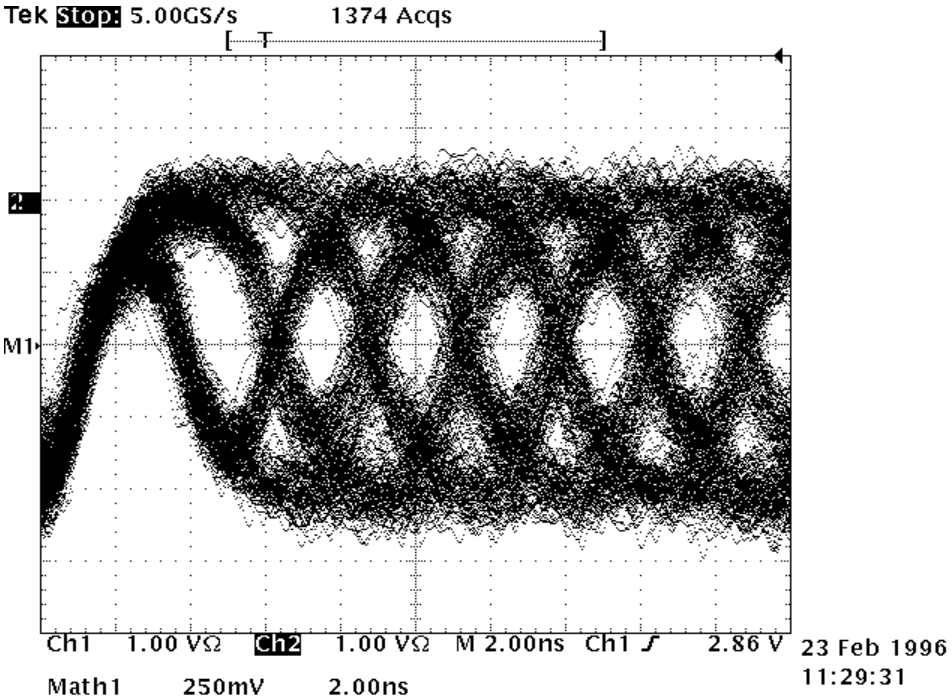

Figure 26: SSA RX Eye Diagram: 40MB/s, 20.0 meter cable

8. Bit Error Rates

At present the ability to trigger bit error rates is limited, due to limitations of the HP pattern generator and logic analyzer trigger programmability. The bit error rate information described in this section is very primarily.

8.1 40MB/s Single Character (DIS)

Initial bit error rates were tested with a continuous fixed DIS character (K.28.5) transmitted on one PHY and received by the other PHY. Multiple configurations of PHY1/2 and port1/2 were tested with various cable lengths up to 20 meters. The logic analyzer was configured to trigger on any character received that was not a DIS character.

Bit error rate testing was done with the PHY power supply set to the 3.0V and 3.6V limits. No character errors were triggered with the above conditions. The over/under voltage tests were run over a 3 day period. Cable voltage drop was considered in tuning the supply outputs for voltage corner testing.

Using one of the 30 meter cables from the lab stock we were able to trigger random character errors at an indeterminate rate. The differential single bit pattern was clearly attenuated and measured below 100mV differential.

8.2 40MB/s Random Characters

Using a random pattern sequence transmitted, as described in the eye diagram section, more additional bit error rate testing was done. Again various cable lengths were tested between two PHY devices sharing a common 50MHz clock input and common power supplies. The logic analyzer was configured to trigger on any receive code violation, ie. RX port CODEV output = logic high. This method of triggering for bit errors is not 100% valid because each character received was not verified to the relative character sent. A serial bit error that resulted in the decoding of a “valid” 10 bit 8B/10B pattern would not be detected.

For all cables tested between 0.3 and 10.0 meters no character code violations were triggered. A 10.0 meter cable was tested over a period greater than 3 days without triggering a code violation. Minimum and maximum voltage conditions were tested.

Using a 20.0 meter cable code violations were consistently triggered. Different 20.0 meter cables were tested and the results were similar. The code violation error rate was observed to be as high as $3x10^{3}$ errors/sec. At present no cables that are between the length of 10.0 and 20.0 meters were available for testing. Further evaluation of code violation error rate is being done and will be described in a future revision of this report.

8.3 20MB/s Fixed/Random Characters

No code violation errors were triggered with cable lengths up to 30.0 meters at 20MB/s data rates. Both fixed and random character patterns were tested over minimum and maximum voltage conditions.

9. Appendix

The following plots are TDR impedance measurements of the SSA signal traces on PHY Test Board #2. Measurements were made by Chris Parker of IBM Microelectronics Division, 2/22/96. A Tektronix 11801A Digital Sampling Oscilloscope was used for making these measurements.