To: Bill Ham, DEC From: Dave Instone Subject: SSA TDR Measurements

I have done some TDR measurements on some of our Eclipse SSA products. The capacitive load of the module pulls the impedance down below 60 ohms for up to 1.5 nanosecs. Rather alarmed I did some tests on some printed circuit stripline and found that as little as 3 picofarads between the traces caused an identical effet. This equates to 1.5pf to ground on each line.

I also tried the effect of a software filter to limit the effective rise time to 1v/ns. This had virtually no effect on the error caused by the capacitor.

I think you would agree that it is unreasonable to expect the 'silicon' to present a capacitive load less than this. In addition our Eclipses perform correctly with respect to the error rate requirments.

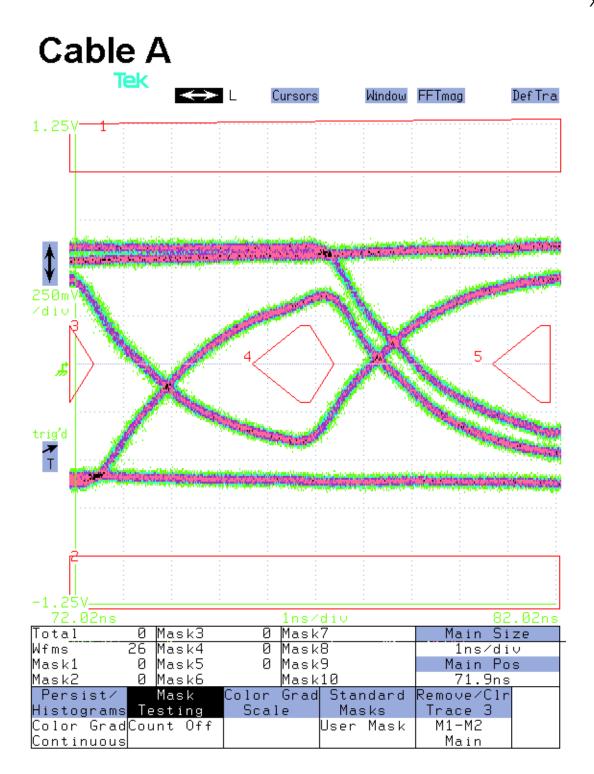
I suggest the following note be added to 7.3:-

The impedances measured may fall below 60 ohm (line to gnd) and 120 ohm (line to line) provided that no single excursion below these limits last for more than 1.5nS and that the lowest point is not less than 20 ohms (line to gnd) and 40 ohms(line to line).

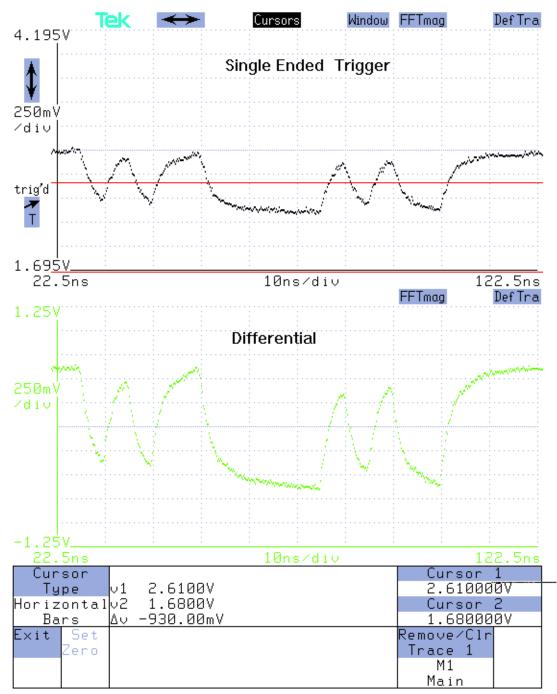
Regards

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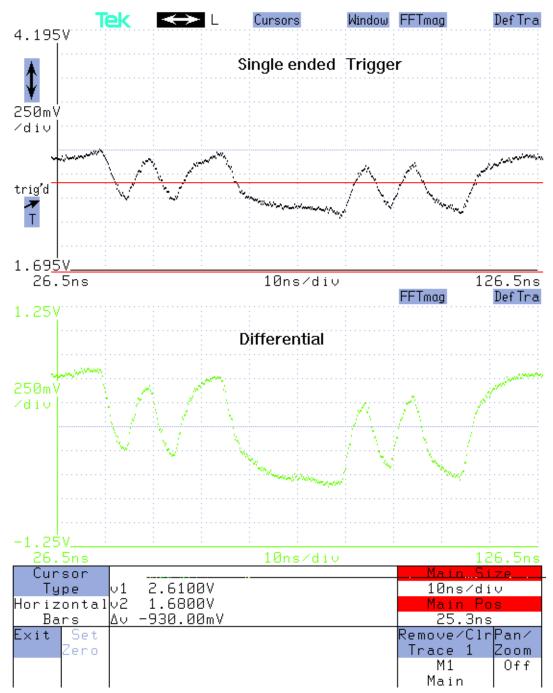
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Cable A



Cable B



Cable B

