

48-bit LBA proposal

To: Technical Committee T13
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Introduction

Today's 28-bit sector addressing provides for up to 268,435,456 sectors or approximately 268 mega sectors. At 512 bytes per sector, this allows device capacity up to 137,438,953,472 bytes or approximately 137 giga bytes. At the rate that disk drive capacities are increasing today, that limit will soon be reached.

This proposal provides for 48-bit sector addressing that provides for up to 281,474,976,710,656 sectors or approximately 281 tera sectors. At 512 bytes per sector, this allows device capacity up to 144,115,188,075,855,872 bytes or approximately 144 peta bytes.

New devices implementing this 48-bit addressing are totally backward compatible with existing hosts and host software. The usable capacity of the device will be limited to that addressable by the host but the device will operate normally at that capacity.

In addition, the number of sectors that may be transferred by a single command are increased by increasing the allowable sector number to 16 bits.

Proposed changes

The following additions/modifications are proposed for the ATA/ATAPI-6 standard based on the ATA/ATAPI-6 rev 0 draft standard:

6.x 48-bit Address feature set

The 48-bit Address feature set allows devices of capacities up to 281,474,976,710,656 sectors or approximately 281 tera sectors. At 512 bytes per sector, this allows device capacity up to 144,115,188,075,855,872 bytes or approximately 144 peta bytes. In addition, the number of sectors that may be transferred by a single command are increased by increasing the allowable sector number to 16 bits.

Commands unique to the 48-bit Address feature set are:

FLUSH CACHE EXT
 READ DMA EXT
 READ DMA QUEUED EXT
 READ MULTIPLE EXT
 READ NATIVE MAX ADDRESS EXT
 READ SECTOR(S) EXT
READ VERIFY SECTOR(S)
 SET MAX ADDRESS EXT
 WRITE DMA EXT
 WRITE DMA QUEUED EXT
 WRITE MULTIPLE EXT

WRITE SECTOR(S) EXT

The 48-bit Address feature set operates in LBA addressing only. Devices implementing the 48-bit Address feature set shall also implement commands that use 28-bit addressing and 28-bit and 48-bit commands may be intermixed. Support of the 48-bit Address feature set is indicated in the IDENTIFY DEVICE response.

In a device implementing the 48-bit Address feature set, the Features register, the Sector Count register, the Sector Number register, the Cylinder Low register, and the Cylinder High register are each in fact a two byte deep FIFO. Each time one of these registers is written, the new content written is placed into the “most recently written” location and the previous content of the register is moved to “previous content” location. For example, when a 48-bit Address feature set READ SECTOR(S) EXT command is written to the device Command register, the address utilized by the command is as described in the table below.

Register	“most recently written”	“previous content”
Features	Reserved	Reserved
Sector Count	Sector count (7:0)	Sector count (15:8)
Sector Number	LBA (7:0)	LBA (31:24)
Cylinder Low	LBA (15:8)	LBA (39:32)
Cylinder High	LBA (23:16)	LBA (47:40)
Device/Head register	LBA bit shall be set, Bits (3:0) are reserved	Reserved

When a READ SECTOR(S) command utilizing 28-bit addressing is written to the device Command register, the address utilized by the command is as described in the table below. Thus commands utilizing 28-bit addressing still function as described in the command descriptions.

Register	“most recently written”	“previous content”
Features	na	na
Sector Count	Sector count (7:0)	na
Sector Number	Sector number or LBA (7:0)	na
Cylinder Low	Cylinder low or LBA (15:8)	na
Cylinder High	Cylinder High or LBA (23:16)	na
Device/Head register	Head or LBA (27:24)	na

The host may read the “previous content” of the Features, Sector Count, Sector Number, Cylinder Low, and Cylinder High registers by first setting HOB (bit 7) of the Device Control register to one and then reading the desired register. Setting HOB (bit 7) in the Device Control register to zero allows the host to read the “most recently written” content. A host shall always clear HOB (bit 7) to zero after reading the “previous content” of registers. A write to any Command Block register shall cause the device to clear the HOB bit to zero in the Device Control register. The “most recently written” content always gets written by a register write regardless of the state of HOB (bit 7) in the Device Control register.

Registers are written and read as described in 7.1.

The fact that the 48-bit Address feature set is supported is indicated in the IDENTIFY DEVICE response. In addition, the maximum user LBA address accessible by 48-bit addressable commands is contained in IDENTIFY DEVICE response words 100 through 103.

If the value contained IDENTIFY DEVICE response words 100 through 103 is equal to or less than 268,435,456, then the content of words 1, 3, 6, 54, 55, 56, 57, 58, 60, and 61 shall be as described in 6.2.1. If the value contained IDENTIFY DEVICE response words 100 through 103 is greater than 268,435,456, then the content of words 1, 3, 6, 54, 55, 56, 57, 58, 60, and 61 shall

be as described in 6.2.1 when the value in words 61:60 is 268,435,456. That is, if the device contains greater than the capacity addressable with 28-bit commands, words 1, 3, 6, 54, 55, 56, 57, 58, 60, and 61 shall describe the maximum capacity device that can be addressed by 28-bit commands.

When the 48-bit Address feature set is implemented, the native maximum address is the highest address accepted by the device in the factory default condition using a 48-bit Address feature set command. The native maximum address is the value returned by a READ NATIVE MAX ADDRESS EXT command. If the native maximum address of a device is equal to or less than 268,435,455, a READ NATIVE MAX ADDRESS shall return the native maximum address. If the native maximum address is greater than 268,435,455, a READ NATIVE MAX ADDRESS command shall return a value of 268,435,455.

When the 48-bit Address feature set is implemented, the SET MAX ADDRESS command shall execute as described in 8.38.1. However, in addition to modifying the content of words 61:60, the new content of 61:60 shall also be placed in words 103:100. When a SET MAX ADDRESS EXT command is issued and the address requested is greater than 268,435,455, words 103:100 shall be modified to reflect the requested value but words 1, 3, 6, 54, 55, 56, 57, 58, 60, and 61 shall not be modified. When a SET MAX ADDRESS EXT command is issued and the address requested is equal to or less than 268,435,455, words 103:100 shall be modified to reflect the requested value and words 1, 3, 6, 54, 55, 56, 57, 58, 60, and 61 shall be modified as described in 8.38.1.8.

If a Host Protected Area has been created using the SET MAX ADDRESS command, all SET MAX ADDRESS EXT commands shall return command abort until the Host protected area is eliminated by use of the SET MAX ADDRESS command with the address value returned by the READ NATIVE MAX ADDRESS command. If a Host Protected Area has been created using the SET MAX ADDRESS EXT command, all SET MAX ADDRESS commands shall return command abort until the Host Protected Area is eliminated by use of the SET MAX ADDRESS EXT command with the address value returned by the READ NATIVE MAX ADDRESS EXT command.

In clause 7.9.6.

Add the HOB bit as shown below:

7	6	5	4	3	2	1	0
HOB	r	r	r	r	SRST	nIEN	0

- HOB (high order byte) is utilized by devices that implement the 48-bit Address feature set (see 6.x). A write to any Command Block register shall clear the HOB bit to zero.
- Bits 6 through 3 are reserved.
- SRST is the host software reset bit (see 9.2).
- nIEN is the enable bit for the device Assertion of INTRQ to the host. When the nIEN bit is cleared to zero, and the device is selected, INTRQ shall be enabled through a tri-state buffer and shall be asserted or negated by the device as appropriate. When the nIEN bit is set to one, or the device is not selected, the INTRQ signal shall be in a high impedance state.
- Bit 0 shall be cleared to zero.

In clause 8

A command description is added for each of the new 48-bit Address features set commands and the IDENTIFY DEVICE, READ NATIVE MAX ADDRESS, and SET MAX ADDRESS commands are modified as shown below.

8.10 FLUSH CACHE

8.10.6 Error outputs

Sector Number, Cylinder Low, Cylinder High, Device/Head –

Add sentence “If the device supports the 48-bit Address feature set and the error occurred in an address greater than FFFFFFFh, the value set in the Sector number, Cylinder Low, and Cylinder High registers shall be FFh and the value set in the bits 3 through 0 of the Device/Head register shall be Fh.”

8.a FLUSH CACHE EXT

8.a.1 Command code

EAh

8.a.2 Feature set

48-bit Address feature set

- Mandatory for all devices implementing the 48-bit Address feature set and not implementing the PACKET Command feature set.

8.a.3 Protocol

Non-data command (see 9.4).

8.a.4 Inputs

Register		7	6	5	4	3	2	1	0
Features	Current	Reserved							
	Previous (see note)	Reserved							
Sector Count	Current	Reserved							
	Previous (see note)	Reserved							
Sector Number	Current	Reserved							
	Previous (see note)	Reserved							
Cylinder Low	Current	Reserved							
	Previous (see note)	Reserved							
Cylinder High	Current	Reserved							
	Previous (see note)	Reserved							
Device/Head		obs	na	obs	DEV	na			
Command		EAh							
NOTE – The value indicated as Current is the value most recently written to the register. The value indicated as Previous is the value that was in the register before the most recent write to the register.									

Device/Head register –
DEV shall indicate the selected device.

8.a.5 Normal outputs

Register		7	6	5	4	3	2	1	0
Error		na							
Sector Count	HOB=0	Reserved							
	HOB =1 (see note)	Reserved							
Sector Number	HOB =0	Reserved							
	HOB =1 (see note)	Reserved							
Cylinder Low	HOB =0	Reserved							
	HOB =1 (see note)	Reserved							
Cylinder High	HOB =0	Reserved							
	HOB =1 (see note)	Reserved							
Device/Head		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE – The value indicated by HOB = 0 is the value read when the HOB of the Device Control register is cleared to zero. The value indicated by HOB = 1 is the value read when the HOB of the Device Control register is set to one.									

Device/Head register –
DEV shall indicate the selected device.

Status register –
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.
 DRQ shall be cleared to zero.
 ERR shall be cleared to zero.

8.a.6 Error outputs

An unrecoverable error encountered during execution of writing data results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred. The sector is removed from the cache. Subsequent FLUSH CACHE commands continue the process of flushing the cache.

Register		7	6	5	4	3	2	1	0
Error		na	na	na	na	na	ABRT	na	na
Sector Count	HOB =0	Reserved							
	HOB =1 (see note)	Reserved							
Sector Number	HOB =0	LBA (7:0)							
	HOB =1 (see note)	LBA (31:24)							
Cylinder Low	HOB =0	LBA (15:8)							
	HOB =1 (see note)	LBA (39:32)							
Cylinder High	HOB =0	LBA (23:16)							
	HOB =1 (see note)	LBA (47:40)							
Device/Head		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE – The value indicated by HOB = 0 is the value read when the HOB of the Device Control register is cleared to zero. The value indicated by HOB = 1 is the value read when the HOB of the Device Control register is set to one.									

Error register -

ABRT shall be set to one if the device is not able to complete the action requested by the command.

Sector Number -

LBA (7:0) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (31:24) of the address of the first unrecoverable error when read with Device Control register HOB set to one.

Cylinder Low -

LBA (15:8) of the address of the first unrecoverable error when read with Device Control register HOB cleared to zero.

LBA (39:32) of the address of the first unrecoverable error when read with Device Control register HOB set to one.

Cylinder High -

LBA (23:16) of the address of the first unrecoverable error when read with Device Control register HOB cleared to zero.

LBA (47:40) of the address of the first unrecoverable error when read with Device Control register HOB is set to one.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.
 DF (Device Fault) shall be set to one if a device fault has occurred.
 DRQ shall be cleared to zero.
 ERR shall be set to one if an Error register bit is set to one.

8.a.7 Prerequisites

DRDY set to one.

8.a.8 Description

This command is used by the host to request the device to flush the write cache. If the write cache is to be flushed, all data cached shall be written to the media. The BSY bit shall remain set to one until all data has been successfully written or an error occurs. The device should use all error recovery methods available to ensure the data is written successfully. The flushing of write cache may take several seconds to complete depending upon the amount of data to be flushed and the success of the operation.

NOTE – This command may take longer than 30 s to complete.

8.12 IDENTIFY DEVICE

Table 20

Word	F/V		
84	F	n	1 = 48-bit Address feature set supported.
87	F	n	1 = 48-bit Address feature set supported.
100-103	V		Maximum user LBA address for 48-bit Address feature set.

8.12.45 Words 82-84: Features/command sets supported

If bit n of word 84 is set to one, the 48-bit Address feature set is supported.

8.12.46 Words 85-87: Features/command sets enabled

If bit n of word 87 is set to one, the 48-bit Address feature set is supported.

8.12.x words 100-103 Maximum user LBA address

Words 100 through 103 contains the maximum user LBA address when the 48-bit Address feature set is supported.

8.b READ DMA EXT

8.b.1 Command code

25h

8.b.2 Feature set

48-bit Address feature set

- Mandatory for devices implementing the 48-bit Address feature set.
- Use prohibited for devices implementing the PACKET Command feature set.

8.b.3 Protocol

DMA (see 9.7).

8.b.4 Inputs

0000h in the sector Count register indicates that 65,536 sectors are to be transferred.

Register		7	6	5	4	3	2	1	0
Features	Current Previous (see note)	Reserved Reserved							
Sector Count	Current Previous (see note)	Sector count (7:0) Sector count (15:8)							
Sector Number	Current Previous (see note)	LBA (7:0) LBA (31:24)							
Cylinder Low	Current Previous (see note)	LBA (15:8) LBA (39:32)							
Cylinder High	Current Previous (see note)	LBA (23:16) LBA (47:40)							
Device/Head		obs	LBA	obs	DEV	Reserved			
Command		25h							
NOTE – The value indicated as Current is the value most recently written to the register. The value indicated as Previous is the value that was in the register before the most recent write to the register.									

Sector Count Current -

number of sectors to be transferred low order, bits (7:0).

Sector Count Previous -

number of sectors to be transferred high order, bits (15:8).

Sector Number Current -

LBA (7:0).

Sector Number Previous -

LBA (31:24).

Cylinder Low Current -

LBA (15:8).

Cylinder Low Previous -

LBA (39:32).

Cylinder High Current -

LBA (23:16).

Cylinder High Previous -

LBA (47:40).

Device/Head -

LBA (bit 6) shall be set to one.

DEV shall indicate the selected device.

8.b.5 Normal outputs

Register		7	6	5	4	3	2	1	0
Error		na							
Sector Count	HOB =0				Reserved				
	HOB =1 (see note)				Reserved				
Sector Number	HOB =0				Reserved				
	HOB =1 (see note)				Reserved				
Cylinder Low	HOB =0				Reserved				
	HOB =1 (see note)				Reserved				
Cylinder High	HOB =0				Reserved				
	HOB =1 (see note)				Reserved				
Device/Head		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE – The value indicated by HOB = 0 is the value read when the HOB bit of the Device Control register is cleared to zero. The value indicated by HOB = 1 is the value read when the HOB bit of the Device Control register is set to one.									

Device/Head register –

DEV shall indicate the selected device.

Status register –

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

8.b.6 Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Register		7	6	5	4	3	2	1	0
Error		ICRC	UNC	MC	IDNF	MCR	ABRT	MN	obs
Sector Count	HOB =0 HOB =1 (see note)	Reserved Reserved							
Sector Number	HOB =0 HOB =1 (see note)	LBA (7:0) LBA (31:24)							
Cylinder Low	HOB =0 HOB =1 (see note)	LBA (15:8) LBA (39:32)							
Cylinder High	HOB =0 HOB =1 (see note)	LBA (23:16) LBA (47:40)							
Device/Head		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE – The value indicated by HOB = 0 is the value read when the HOB bit of the Device Control register is cleared to zero. The value indicated by HOB = 1 is the value read when the HOB of the Device Control register is set to one.									

Error register -

ICRC shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer. The content of this bit is not applicable for Multiword DMA transfers.

UNC shall be set to one if data is uncorrectable

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found and after an unsuccessful INITIALIZE DEVICE PARAMETERS command until a valid CHS translation is established (see 8.16.8). IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not supported or if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

Sector Number -

LBA (7:0) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (31:24) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Cylinder Low -

LBA (15:8) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (39:32) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Cylinder High -

LBA (23:16) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (47:40) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Device/Head register -
 DEV shall indicate the selected device.

Status register -
 BSY shall be cleared to zero indicating command completion.
 DRDY shall be set to one.
 DF (Device Fault) shall be set to one if a device fault has occurred.
 DRQ shall be cleared to zero.
 ERR shall be set to one if an Error register bit is set to one.

8.b.7 Prerequisites

DRDY set to one. The host shall initialize the DMA channel.

8.b.8 Description

The READ DMA command allows the host to read data using the DMA data transfer protocol.

8.c READ DMA QUEUED EXT

8.c.1 Command code

26h

8.c.2 Feature set

48-bit Address feature set

- Mandatory for devices implementing the Overlapped feature set and the 48-bit Address feature set but not implementing the PACKET command feature set.
- Use prohibited for devices implementing the PACKET command feature set.

8.c.3 Protocol

DMA QUEUED (see 9.9).

8.c.4 Inputs

0000h in the Features register indicates that 65,536 sectors are to be transferred.

Register		7	6	5	4	3	2	1	0
Features	Current Previous (see note)	Sector count (7:0) Sector count (15:8)							
Sector Count	Current Previous (see note)	Tag				Reserved			
		Reserved							
Sector Number	Current Previous (see note)	LBA (7:0) LBA (31:24)							
		LBA (15:8) LBA (39:32)							
Cylinder Low	Current Previous (see note)	LBA (23:16) LBA (47:40)							
		LBA (23:16) LBA (47:40)							
Device/Head		obs	LBA	obs	DEV	Reserved			
Command		26h							
NOTE – The value indicated as Current is the value most recently written to the register. The value indicated as Previous is the value that was in the register before the most recent write to the register.									

Features Current -

number of sectors to be transferred low order, bits (7:0).

Features Previous -

number of sectors to be transferred high order, bits (15:8).

Sector Count Current -

if the device supports command queuing, bits (7:3) contain the Tag for the command being delivered. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If queuing is not supported, this field is not applicable.

Sector Count Previous -

Reserved

Sector Number Current -

LBA (7:0).

Sector Number Previous -

LBA (31:24).

Cylinder Low Current -

LBA (15:8).

Cylinder Low Previous -

LBA (39:32).

Cylinder High Current -

LBA (23:16).

Cylinder High Previous -

LBA (47:40).

Device/Head -

LBA (bit 6) shall be set to one.

DEV shall indicate the selected device.

8c.5 Normal outputs

8.c.5.1 Data transmission

Data transfer may occur after receipt of the command or may occur after the receipt of a SERVICE command. When the device is ready to transfer data requested by a data transfer command, the device sets the following register content to initiate the data transfer.

Register		7	6	5	4	3	2	1	0
Error		na							
Sector Count	HOB =0	Tag				REL	I/O	C/D	
	HOB =1 (see note)	Reserved							
Sector Number	HOB =0	Reserved							
	HOB =1 (see note)	Reserved							
Cylinder Low	HOB =0	Reserved							
	HOB =1 (see note)	Reserved							
Cylinder High	HOB =0	Reserved							
	HOB =1 (see note)	Reserved							
Device/Head		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE – The value indicated by HOB = 0 is the value read when the HOB bit of the Device Control register is cleared to zero. The value indicated by HOB = 1 is the value read when the HOB bit of the Device Control register is set to one.									

Sector Count (when bit 7 of the Device Control register is cleared to zero) -

Tag -This field contains the command Tag for the command. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If the device does not support command queuing or overlap is disabled, this field is not applicable.

REL - Shall be cleared to zero.

I/O - Shall be set to one indicating the transfer is to the host.

C/D - Shall be cleared to zero indicating the transfer of data.

Device/Head register –

DEV shall indicate the selected device.

Status register –

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

8.c.5.2 Release

If the device performs a bus release before transferring data for this command, the register content upon performing a bus release shall be as shown below.

Register		7	6	5	4	3	2	1	0
Error		na							
Sector Count	HOB =0	Tag				REL	I/O	C/D	
	HOB =1 (see note)	Reserved							
Sector Number	HOB =0	Reserved				Reserved			
	HOB =1 (see note)	Reserved							
Cylinder Low	HOB =0	Reserved				Reserved			
	HOB =1 (see note)	Reserved							
Cylinder High	HOB =0	Reserved				Reserved			
	HOB =1 (see note)	Reserved							
Device/Head		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	SERV	DRQ	na	na	ERR
NOTE – The value indicated by HOB = 0 is the value read when the HOB bit of the Device Control register is cleared to zero. The value indicated by HOB = 1 is the value read when the HOB bit of the Device Control register is set to one.									

Sector Count (when the HOB bit of the Device Control register is cleared to zero) -

Tag -This field contains the command Tag for the command. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If the device does not support command queuing or overlap is disabled, this field is not applicable.

REL - Shall be set to one.

I/O - Shall be set to one indicating the transfer is to the host.

C/D - Shall be cleared to zero indicating the transfer of data.

Device/Head register –

DEV shall indicate the selected device.

Status register –

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

SERV (Service) shall be cleared to zero when no other queued command is ready for service. SERV shall be set to one when another queued command is ready for service. SERV shall be set to one when the device has prepared this command for service.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

8.c.5.3 Service request

When the device is ready to transfer data or complete a command after the command has performed a bus release, the device shall set the SERV bit and not change the state of any other register bit (see 6.9). When the SERVICE command is received, the device shall set outputs as described in data transfer, command completion, or error outputs depending on the service the device requires.

8.c.5.4 Command completion

When the transfer of all requested data has occurred without error, the register content shall be as shown below.

Register		7	6	5	4	3	2	1	0
Error		na							
Sector Count	HOB =0	Tag				REL	I/O	C/D	
	HOB =1 (see note)	Reserved							
Sector Number	HOB =0	Reserved				Reserved			
	HOB =1 (see note)	Reserved							
Cylinder Low	HOB =0	Reserved				Reserved			
	HOB =1 (see note)	Reserved							
Cylinder High	HOB =0	Reserved				Reserved			
	HOB =1 (see note)	Reserved							
Device/Head		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	SERV	DRQ	na	na	ERR
NOTE – The value indicated by HOB = 0 is the value read when the HOB bit of the Device Control register is cleared to zero. The value indicated by HOB = 1 is the value read when the HOB bit of the Device Control register is set to one.									

Sector Count (when the HOB bit of the Device Control register is cleared to zero) -

Tag -This field contains the command Tag for the command. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If the device does not support command queuing or overlap is disabled, this field is not applicable.

REL - Shall be cleared to zero.

I/O - Shall be set to one.

C/D - Shall be set to one.

Device/Head register –

DEV shall indicate the selected device.

Status register –

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

SERV (Service) shall be cleared to zero when no other queued command is ready for service. SERV shall be set to one when another queued command is ready for service.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

8.c.6 Error outputs

The Sector Count register contains the Tag for this command if the device supports command queuing. The device shall return command aborted if the command is not supported or if the device has not had overlapped interrupt enabled. The device shall return command aborted if the device supports command queuing and the Tag is invalid. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector where the first unrecoverable error occurred. If a queue existed, the unrecoverable error shall cause the queue to abort.

Register		7	6	5	4	3	2	1	0
Error		ICRC	UNC	MC	IDNF	MCR	ABRT	MN	obs
Sector Count	HOB =0	Tag					REL	I/O	C/D
	HOB =1 (see note)	Reserved							
Sector Number	HOB =0				LBA (7:0)				
	HOB =1 (see note)				LBA (31:24)				
Cylinder Low	HOB =0				LBA (15:8)				
	HOB =1 (see note)				LBA (39:32)				
Cylinder High	HOB =0				LBA (23:16)				
	HOB =1 (see note)				LBA (47:40)				
Device/Head		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	SERV	DRQ	na	na	ERR
NOTE – The value indicated by HOB = 0 is the value read when the HOB bit of the Device Control register is cleared to zero. The value indicated by HOB = 1 is the value read when the HOB bit of the Device Control register is set to one.									

Error register -

ICRC shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer. The content of this bit is not applicable for Multiword DMA transfers.

UNC shall be set to one if data is uncorrectable

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found and after an unsuccessful INITIALIZE DEVICE PARAMETERS command until a valid CHS translation is established (see 8.16.8). IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not supported or if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

Sector Count (when the HOB bit of the Device Control register is cleared to zero) -

Tag -This field contains the command Tag for the command. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If the device does not support command queuing or overlap is disabled, this field is not applicable.

REL - Shall be cleared to zero.

I/O - Shall be set to one.

C/D - Shall be set to one.

Sector Number -

LBA (7:0) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (31:24) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Cylinder Low -

LBA (15:8) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (39:32) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Cylinder High -

LBA (23:16) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (47:40) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

8.c.7 Prerequisites

DRDY set to one. The host shall initialize the DMA channel.

8.c.8 Description

This command executes in a similar manner to a READ DMA command. The device may perform a bus release or may execute the data transfer without performing a bus release if the data is ready to transfer.

8.j READ MULTIPLE EXT

8.j.1 Command code

29h

8.j.2 Feature set

48-bit Address feature set

- Mandatory for all devices implementing the 48-bit Address feature set.
- Use prohibited when the PACKET feature set is implemented

8.j.3 Protocol

PIO data-in (see 9.5).

8.j.4 Inputs

0000h in the sector Count register indicates that 65,536 sectors are to be transferred.

Register		7	6	5	4	3	2	1	0
Features	Current Previous (see note)	Reserved Reserved							
Sector Count	Current Previous (see note)	Sector count (7:0) Sector count (15:8)							
Sector Number	Current Previous (see note)	LBA (7:0) LBA (31:24)							
Cylinder Low	Current Previous (see note)	LBA (15:8) LBA (39:32)							
Cylinder High	Current Previous (see note)	LBA (23:16) LBA (47:40)							
Device/Head		obs	LBA	obs	DEV	Reserved			
Command		29h							
NOTE – The value indicated as Current is the value most recently written to the register. The value indicated as Previous is the value that was in the register before the most recent write to the register.									

- Sector Count Current -
number of sectors to be transferred low order, bits (7:0).
- Sector Count Previous -
number of sectors to be transferred high order, bits (15:8).
- Sector Number Current -
LBA (7:0).
- Sector Number Previous -
LBA (31:24).
- Cylinder Low Current -
LBA (15:8).
- Cylinder Low Previous -
LBA (39:32).
- Cylinder High Current -
LBA (23:16).
- Cylinder High Previous -
LBA (47:40).
- Device/Head -
LBA (bit 6) shall be set to one.
DEV shall indicate the selected device.

8.j.5 Normal outputs

Register		7	6	5	4	3	2	1	0
Error		na							
Sector Count	HOB=0				Reserved				
	HOB =1 (see note)				Reserved				
Sector Number	HOB =0				Reserved				
	HOB =1 (see note)				Reserved				
Cylinder Low	HOB =0				Reserved				
	HOB =1 (see note)				Reserved				
Cylinder High	HOB =0				Reserved				
	HOB =1 (see note)				Reserved				
Device/Head		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE – The value indicated by HOB = 0 is the value read when the HOB bit of the Device Control register is cleared to zero. The value indicated by HOB = 1 is the value read when the HOB bit of the Device Control register is set to one.									

Device/Head register –

DEV shall indicate the selected device.

Status register –

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

8.j.6 Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Register		7	6	5	4	3	2	1	0
Error		na	UNC	MC	IDNF	MCR	ABRT	NM	obs
Sector Count	HOB =0 HOB =1 (see note)	Reserved Reserved							
Sector Number	HOB =0 HOB =1 (see note)	LBA (7:0) LBA (31:24)							
Cylinder Low	HOB =0 HOB =1 (see note)	LBA (15:8) LBA (39:32)							
Cylinder High	HOB =0 HOB =1 (see note)	LBA (23:16) LBA (47:40)							
Device/Head		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE – The value indicated by HOB = 0 is the value read when the HOB bit of the Device Control register is cleared to zero. The value indicated by HOB = 1 is the value read when the HOB bit of the Device Control register is set to one.									

Error register -

UNC shall be set to one if data is uncorrectable

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

Sector Number -

LBA (7:0) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (31:24) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Cylinder Low -

LBA (15:8) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (39:32) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Cylinder High -

LBA (23:16) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (47:40) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.
 DF (Device Fault) shall be set to one if a device fault has occurred.
 DRQ shall be cleared to zero.
 ERR shall be set to one if an Error register bit is set to one.

8.j.7 Prerequisites

DRDY set to one. If bit of IDENTIFY DEVICE word 59 is cleared to zero, a successful SET MULTIPLE MODE command shall precede a READ MULTIPLE EXT command.

8.j.8 Description

The READ MULTIPLE EXT command performs the same as the READ SECTOR(S) command except that when the device is ready to transfer data for a block of sectors, the device clears BSY, sets DRDY and DRQ (and sets DF, ERR, and the bits in the Error register, as required), and enters the interrupt pending state only before the data transfer for the first sector of the block sectors. The remaining sectors for the block are transferred without the device asserting INTRQ. In addition, the DRQ qualification of the transfer is required only before the first sector of a block, not before each sector of the block.

The number of sectors per block is defined by a successful SET MULTIPLE command. If no successful SET MULTIPLE command has been issued, the block is defined by the device's default value for number of sectors per block as defined in bits 0-7 in word 47 in the IDENTIFY DEVICE information.

If bit 8 equals 1 and bits 0-7 are cleared to zero in word 59 in the IDENTIFY DEVICE information, then the block count of sectors to be transferred without intervening interrupts shall be programmed by the SET MULTIPLE MODE command before issuing the first READ MULTIPLE EXT command after a power-on or hardware reset. If bit 8 in word 1 is set to one and bits 0-7 are not cleared to zero in word 59 in the IDENTIFY DEVICE information, then the block count of sectors to be transferred without intervening interrupts may be reprogrammed by the SET MULTIPLE MODE command before issuing the next READ MULTIPLE EXT command.

When the READ MULTIPLE EXT command is issued, the Sector Count register contains the number of sectors (not the number of blocks) requested.

If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer shall be for n sectors, where $n = \text{remainder}(\text{sector count} / \text{block count})$.

If the READ MULTIPLE EXT command is received when READ MULTIPLE commands are disabled, the READ MULTIPLE operation shall be rejected with command aborted.

Device errors encountered during READ MULTIPLE EXT commands are posted at the beginning of the block or partial block transfer, but the DRQ bit is still set to one and the data transfer shall take place, including transfer of corrupted data, if any. The contents of the Command Block Registers following the transfer of a data block that had a sector in error are undefined. The host should retry the transfer as individual requests to obtain valid error information.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block that contained the error.

8.26 READ NATIVE MAX ADDRESS

Add to 8.26.8 –

If the 48-bit Address feature set is supported and the 48-bit native max address is greater than 268,435,455, the READ NATIVE MAX ADDRESS command shall return a value of 268,435,455.

8.d READ NATIVE MAX ADDRESS EXT

8.d.1 Command code

27h

8.d.2 Feature set

Host Protected Area feature set/48-bit Address feature set.

- Mandatory when the Host Protected Area feature set and the 48-bit Address feature set are implemented.
- Use prohibited when Removable feature set is implemented.

8.d.3 Protocol

Non-data command (see 9.4).

8.d.4 Inputs

Register		7	6	5	4	3	2	1	0
Features	Current Previous (see note)	Reserved Reserved							
Sector Count	Current Previous (see note)	Reserved Reserved							
Sector Number	Current Previous (see note)	Reserved Reserved							
Cylinder Low	Current Previous (see note)	Reserved Reserved							
Cylinder High	Current Previous (see note)	Reserved Reserved							
Device/Head		obs	LBA	obs	DEV	na			
Command		27h							
NOTE – The value indicated as Current is the value most recently written to the register. The value indicated as Previous is the value that was in the register before the most recent write to the register.									

Device/Head register –
LBA shall be set to one.
DEV shall indicate the selected device.

8.d.5 Normal outputs

Register		7	6	5	4	3	2	1	0
Error		na							
Sector Count	HOB =0	Reserved							
	HOB =1 (see note)	Reserved							
Sector Number	HOB =0	Native max address LBA (7:0)							
	HOB =1 (see note)	Native max address LBA (31:24)							
Cylinder Low	HOB =0	Native max address LBA (15:8)							
	HOB =1 (see note)	Native max address LBA (39:32)							
Cylinder High	HOB =0	Native max address LBA (23:16)							
	HOB =1 (see note)	Native max address LBA (47:40)							
Device/Head		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE – The value indicated by HOB = 0 is the value read when the HOB bit of the Device Control register is cleared to zero. The value indicated by HOB = 1 is the value read when the HOB bit of the Device Control register is set to one.									

Sector Number -

LBA (7:0) of the address of the Native max address when read with Device Control register HOB bit cleared to zero.

LBA (31:24) of the address of the Native max address when read with Device Control register HOB bit set to one.

Cylinder Low -

LBA (15:8) of the address of the Native max address when read with Device Control register HOB bit cleared to zero.

LBA (39:32) of the address of the Native max address when read with Device Control register HOB bit set to one.

Cylinder High -

LBA (23:16) of the address of the Native max address when read with Device Control register HOB bit cleared to zero.

LBA (47:40) of the address of the Native max address when read with Device Control register HOB bit set to one.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

8.d.6 Error outputs

If this command is not supported the device shall return command aborted.

Register		7	6	5	4	3	2	1	0
Error		na	na	na	na	na	ABRT	na	obs
Sector Count	HOB =0 HOB =1 (see note)	Reserved				Reserved			
Sector Number	HOB =0 HOB =1 (see note)	Reserved				Reserved			
Cylinder Low	HOB =0 HOB =1 (see note)	Reserved				Reserved			
Cylinder High	HOB =0 HOB =1 (see note)	Reserved				Reserved			
Device/Head		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE – The value indicated by HOB = 0 is the value read when HOB bit of the Device Control register is cleared to zero. The value indicated by HOB = 1 is the value read when HOB bit of the Device Control register is set to one.									

Error register -

ABRT shall be set to one if this command is not supported.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

8.d.7 Prerequisites

DRDY set to one.

8.d.8 Description

This command returns the native maximum address. The native maximum address is the highest address accepted by the device in the factory default condition. The native maximum address is the maximum address that is valid when using the SET MAX ADDRESS EXT command.

8.e READ SECTOR(S) EXT

8.e.1 Command code

24h

8.e.2 Feature set

48-bit Address feature set

- Mandatory for all devices implementing the 48-bit Address feature set.
- Use prohibited when the PACKET feature set is implemented

8.e.3 Protocol

PIO data-in (see 9.5).

8.e.4 Inputs

0000h in the sector Count register indicates that 65,536 sectors are to be transferred.

Register		7	6	5	4	3	2	1	0
Features	Current Previous (see note)	Reserved Reserved							
Sector Count	Current Previous (see note)	Sector count (7:0) Sector count (15:8)							
Sector Number	Current Previous (see note)	LBA (7:0) LBA (31:24)							
Cylinder Low	Current Previous (see note)	LBA (15:8) LBA (39:32)							
Cylinder High	Current Previous (see note)	LBA (23:16) LBA (47:40)							
Device/Head		obs	LBA	obs	DEV	Reserved			
Command		24h							
NOTE – The value indicated as Current is the value most recently written to the register. The value indicated as Previous is the value that was in the register before the most recent write to the register.									

Sector Count Current -

number of sectors to be transferred low order, bits (7:0).

Sector Count Previous -

number of sectors to be transferred high order, bits (15:8).

Sector Number Current -

LBA (7:0).

Sector Number Previous -

LBA (31:24).

Cylinder Low Current -

LBA (15:8).

Cylinder Low Previous -

LBA (39:32).

Cylinder High Current -

LBA (23:16).

Cylinder High Previous -

LBA (47:40).

Device/Head -

LBA (bit 6) shall be set to one.

DEV shall indicate the selected device.

8.e.5 Normal outputs

Register		7	6	5	4	3	2	1	0
Error		na							
Sector Count	HOB=0				Reserved				
	HOB =1 (see note)				Reserved				
Sector Number	HOB =0				Reserved				
	HOB =1 (see note)				Reserved				
Cylinder Low	HOB =0				Reserved				
	HOB =1 (see note)				Reserved				
Cylinder High	HOB =0				Reserved				
	HOB =1 (see note)				Reserved				
Device/Head		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE – The value indicated by HOB = 0 is the value read when the HOB bit of the Device Control register is cleared to zero. The value indicated by HOB = 1 is the value read when the HOB bit of the Device Control register is set to one.									

Device/Head register –

DEV shall indicate the selected device.

Status register –

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

8.e.6 Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Register		7	6	5	4	3	2	1	0
Error		na	UNC	MC	IDNF	MCR	ABRT	NM	obs
Sector Count	HOB =0 HOB =1 (see note)	Reserved Reserved							
Sector Number	HOB =0 HOB =1 (see note)	LBA (7:0) LBA (31:24)							
Cylinder Low	HOB =0 HOB =1 (see note)	LBA (15:8) LBA (39:32)							
Cylinder High	HOB =0 HOB =1 (see note)	LBA (23:16) LBA (47:40)							
Device/Head		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE – The value indicated by HOB = 0 is the value read when the HOB bit of the Device Control register is cleared to zero. The value indicated by HOB = 1 is the value read when the HOB bit of the Device Control register is set to one.									

Error register -

UNC shall be set to one if data is uncorrectable

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

Sector Number -

LBA (7:0) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (31:24) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Cylinder Low -

LBA (15:8) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (39:32) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Cylinder High -

LBA (23:16) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (47:40) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

8.e.7 Prerequisites

DRDY set to one.

8.e.8 Description

This command reads from 1 to 65,536 sectors as specified in the Sector Count register. A sector count of 0 requests 65,536 sectors. The transfer shall begin at the sector specified in the Sector Number register.

The DRQ bit is always set to one prior to data transfer regardless of the presence or absence of an error condition.

8.x READ VERIFY SECTOR(S) EXT

8.x.1 Command code

42h

8.x.2 Feature set

48-bit Address feature set

- Mandatory for all devices implementing the 48-bit Address feature set.
- Use prohibited when the PACKET feature set is implemented

8.x.3 Protocol

Non-data (see 9.4).

8.x.4 Inputs

Register		7	6	5	4	3	2	1	0
<u>Features</u>	<u>Current</u> <u>Previous</u> <u>(see note)</u>	<u>Reserved</u> <u>Reserved</u>							
<u>Sector Count</u>	<u>Current</u> <u>Previous</u> <u>(see note)</u>	<u>Sector count (7:0)</u> <u>Sector count (15:8)</u>							
<u>Sector Number</u>	<u>Current</u> <u>Previous</u> <u>(see note)</u>	<u>LBA (7:0)</u> <u>LBA (31:24)</u>							
<u>Cylinder Low</u>	<u>Current</u> <u>Previous</u> <u>(see note)</u>	<u>LBA (15:8)</u> <u>LBA (39:32)</u>							
<u>Cylinder High</u>	<u>Current</u> <u>Previous</u> <u>(see note)</u>	<u>LBA (23:16)</u> <u>LBA (47:40)</u>							
<u>Device/Head</u>		<u>obs</u>	<u>LBA</u>	<u>obs</u>	<u>DEV</u>	<u>Reserved</u>			
<u>Command</u>		<u>24h</u>							
<u>NOTE – The value indicated as Current is the value most recently written to the register. The value indicated as Previous is the value that was in the register before the most recent write to the register.</u>									

Sector Count Current -number of sectors to be transferred low order, bits (7:0).Sector Count Previous -number of sectors to be transferred high order, bits (15:8).Sector Number Current -LBA (7:0).Sector Number Previous -LBA (31:24).Cylinder Low Current -LBA (15:8).Cylinder Low Previous -LBA (39:32).Cylinder High Current -LBA (23:16).Cylinder High Previous -LBA (47:40).Device/Head -LBA (bit 6) shall be set to one.DEV shall indicate the selected device.

8.x.5 Normal outputs

Register		7	6	5	4	3	2	1	0
<u>Error</u>		<u>na</u>							
<u>Sector Count</u>	<u>HOB=0</u> <u>HOB =1</u> <u>(see note)</u>				<u>Reserved</u> <u>Reserved</u>				
<u>Sector Number</u>	<u>HOB =0</u> <u>HOB =1</u> <u>(see note)</u>				<u>Reserved</u> <u>Reserved</u>				
<u>Cylinder Low</u>	<u>HOB =0</u> <u>HOB =1</u> <u>(see note)</u>				<u>Reserved</u> <u>Reserved</u>				
<u>Cylinder High</u>	<u>HOB =0</u> <u>HOB =1</u> <u>(see note)</u>				<u>Reserved</u> <u>Reserved</u>				
<u>Device/Head</u>		<u>obs</u>	<u>na</u>	<u>obs</u>	<u>DEV</u>	<u>Reserved</u>			
<u>Status</u>		<u>BSY</u>	<u>DRDY</u>	<u>DF</u>	<u>na</u>	<u>DRQ</u>	<u>na</u>	<u>na</u>	<u>ERR</u>
<p><u>NOTE – The value indicated by HOB = 0 is the value read when the HOB bit of the Device Control register is cleared to zero. The value indicated by HOB = 1 is the value read when the HOB bit of the Device Control register is set to one.</u></p>									

Device/Head register –DEV shall indicate the selected device.Status register –BSY shall be cleared to zero indicating command completion.DRDY shall be set to one.DF (Device Fault) shall be cleared to zero.DRQ shall be cleared to zero.ERR shall be cleared to zero.**8.x.6 Error outputs**

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred.

Register		7	6	5	4	3	2	1	0
Error		na	UNC	MC	IDNF	MCR	ABRT	NM	obs
Sector Count	HOB =0 HOB =1 (see note)				Reserved Reserved				
Sector Number	HOB =0 HOB =1 (see note)				LBA (7:0) LBA (31:24)				
Cylinder Low	HOB =0 HOB =1 (see note)				LBA (15:8) LBA (39:32)				
Cylinder High	HOB =0 HOB =1 (see note)				LBA (23:16) LBA (47:40)				
Device/Head		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE – The value indicated by HOB = 0 is the value read when the HOB bit of the Device Control register is cleared to zero. The value indicated by HOB = 1 is the value read when the HOB bit of the Device Control register is set to one.									

Error register -

UNC shall be set to one if data is uncorrectable

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

Sector Number -

LBA (7:0) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (31:24) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Cylinder Low -

LBA (15:8) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (39:32) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Cylinder High -

LBA (23:16) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (47:40) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

8.x.7 Prerequisites

DRDY set to one.

8.x.8 Description

This command is identical to the READ SECTOR(S) EXT command, except that the device shall have read the data from the media, the DRQ bit is never set to one, and no data is transferred to the host.

8.38.1 SET MAX ADDRESS

Add the following as paragraph two to 8.38.1.8 –

If the 48-bit Address feature set is supported, the value placed in IDENTIFY DEVICE response words 103:100 shall be the same as the value placed in words 61:60.

8.f SET MAX ADDRESS EXT

8.f.1 Command code

37h.

8.f.2 Feature set

Host Protected Area feature set/48-bit Address feature set.

- Mandatory when the Host Protected Area feature set and the 48-bit Address feature set is implemented.
- Use prohibited when the Removable feature set is implemented.

8.f.3 Protocol

Non-data command (see 9.4).

8.f.4 Inputs

Register		7	6	5	4	3	2	1	0	
Features	Current Previous (see note)	Reserved Reserved								
Sector Count	Current Previous (see note)	Reserved Reserved							V	V
Sector Number	Current Previous (see note)	SET MAX LBA (7:0) SET MAX LBA (31:24)								
Cylinder Low	Current Previous (see note)	SET MAX LBA (15:8) SET MAX LBA (39:32)								
Cylinder High	Current Previous (see note)	SET MAX LBA (23:16) SET MAX LBA (47:40)								
Device/Head		obs	LBA	obs	DEV	Reserved				
Command		37h								
NOTE – The value indicated as Current is the value most recently written to the register. The value indicated as Previous is the value that was in the register before the most recent write to the register.										

Sector Count Current -

V V (Value volatile). If bit 0 is set to one, the device shall preserve the maximum values over power-up or hardware reset. If bit 0 is cleared to zero, the device shall revert to the most recent non-volatile maximum address value setting over power-up or hardware reset.

Sector Number Current -

SET MAX LBA (7:0).

Sector Number Previous -

SET MAX LBA (31:24).

Cylinder Low Current -

SET MAX LBA (15:8).

Cylinder Low Previous -

SET MAX LBA (39:32).

Cylinder High Current -

SET MAX LBA (23:16).

Cylinder High Previous -

SET MAX LBA (47:40).

Device/Head -

LBA (bit 6) shall be set to one.

DEV shall indicate the selected device.

8.f.5 Normal outputs

Register		7	6	5	4	3	2	1	0
Error		na							
Sector Count	HOB =0 HOB =1 (see note)	Reserved Reserved							
Sector Number	HOB =0 HOB =1 (see note)	SET MAX LBA (7:0) SET MAX LBA (31:24)							
Cylinder Low	HOB =0 HOB =1 (see note)	SET MAX LBA (15:8) SET MAX LBA (39:32)							
Cylinder High	HOB =0 HOB =1 (see note)	SET MAX LBA (23:16) SET MAX LBA (47:40)							
Device/Head		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE – The value indicated by HOB = 0 is the value read when the HOB bit of the Device Control register is cleared to zero. The value indicated by HOB = 1 is the value read when the HOB bit of the Device Control register is set to one.									

Sector Number -

LBA (7:0) of the address of the SET MAX ADDRESS when read with Device Control register HOB bit cleared to zero.

LBA (31:24) of the address of the SET MAX ADDRESS when read with Device Control register HOB bit set to one.

Cylinder Low -

LBA (15:8) of the address of the SET MAX ADDRESS when read with Device Control register HOB bit cleared to zero.

LBA (39:32) of the address of the SET MAX ADDRESS when read with Device Control register HOB bit set to one.

Cylinder High -

LBA (23:16) of the address of the SET MAX ADDRESS when read with Device Control register HOB bit cleared to zero.

LBA (47:40) of the address of the SET MAX ADDRESS when read with Device Control register HOB bit set to one.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

8.f.6 Error outputs

If this command is not supported, the maximum value to be set exceeds the capacity of the device, or the device is in the Set_Max_Locked or Set_Max_Frozen state, then the device shall return command aborted.

Register		7	6	5	4	3	2	1	0
Error		na	na	na	IDNF	na	ABRT	na	obs
Sector Count	HOB =0 HOB =1 (see note)				Reserved Reserved				
Sector Number	HOB =0 HOB =1 (see note)				Reserved Reserved				
Cylinder Low	HOB =0 HOB =1 (see note)				Reserved Reserved				
Cylinder High	HOB =0 HOB =1 (see note)				Reserved Reserved				
Device/Head		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	na	na	na	na	na	ERR
NOTE – The value indicated by HOB = 0 is the value read when the HOB bit of the Device Control register is cleared to zero. The value indicated by HOB = 1 is the value read when the HOB bit of the Device Control register is set to one.									

Error register -

ABRT shall be set to one if this command is not supported, maximum value requested exceeds the device capacity or the command is not immediately preceded by a READ NATIVE MAX ADDRESS EXT command. ABRT may be set to one if the device is not able to complete the action requested by the command.

IDNF shall be set to one if the command was the second non-volatile SET MAX ADDRESS command after power-on or hardware reset.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

8.f.7 Prerequisites

DRDY set to one. A successful READ NATIVE MAX ADDRESS EXT command shall immediately precede a SET MAX ADDRESS EXT command.

8.f.8 Description

After successful command completion, all read and write access attempts to addresses greater than specified by the successful SET MAX ADDRESS EXT command shall be rejected with an IDNF error. IDENTIFY DEVICE response words 100, 101, 102, and 103 shall reflect the maximum address set with this command.

Hosts should not issue more than one non-volatile SET MAX ADDRESS EXT command after a power-on or hardware reset. Devices should report an IDNF error upon receiving a second non-volatile SET MAX ADDRESS command after a power-on or hardware reset.

The contents of IDENTIFY DEVICE words and the max address shall not be changed if a SET MAX ADDRESS EXT command fails.

After a successful SET MAX ADDRESS command using a new maximum cylinder number value the content of all IDENTIFY DEVICE words shall comply with 6.2.1 in addition to the following:

- 1) The content of words 3, 6, 55, and 56 are unchanged
- 2) The content of word 1 shall equal (the new SET MAX cylinder number + 1) or 16,383, whichever is less
- 3) The content of words (61:60) shall equal [(the new content of word 1 as determined by the successful SET MAX ADDRESS command) * (the content of word 3) * (the content of word 6)]
- 4) If the content of words (61:60) as determined by a successful SET MAX ADDRESS command is less than 16,514,064, then the content of word 54 shall be equal to [(the content of words (61:60)) ÷ ((the content of IDENTIFY DEVICE word 55) * (the content of word 56))] or 65,535, whichever is less
- 5) If the content of word (61:60) as determined by a successful SET MAX ADDRESS command is greater than 16,514,064, then word 54 shall equal the whole number result of [((16,514,064) ÷ [(the content of word 55) * (the content of word 56)])] or 65,535 whichever is less) The content of words (58:57) shall be equal to [(the new content of word 54 as determined by the successful SET MAX ADDRESS command) * (the content of word 55) * (the content of word 56)]

After a successful SET MAX ADDRESS command using a new maximum LBA address the content of all IDENTIFY DEVICE words shall comply with 6.2.1 in addition to the following:

- The content of words (61:60) shall be equal to the new Maximum LBA address + 1.
- If the content of words (61:60) is greater than 16,514,064 and if the device does not support CHS addressing, then the content of words 1, 3, 6, 54, 55, 56, and (58:57) shall equal zero.

If the device supports CHS addressing:

- The content of words 3, 6, 55, and 56 are unchanged.
- If the new content of words (61:60) is less than 16,514,064, then the content of word 1 shall be equal to [(the new content of words (61:60)) ÷ [(the content of word 3) * (the content of word 6)]] or 65,535, whichever is less.
- If the new content of words (61:60) is greater than or equal to 16,514,064, then the content of word 1 shall be equal to 16,383.
- If the new content of words (61:60) is less than 16,514,064, then the content of word 54 shall be equal to [(the new content of words (61:60)) ÷ [(the content of word 55) * (the content of word 56)]].
- If the new content of words (61:60) is greater than or equal to 16,514,064, then the content of word 54 shall be equal to 16,383.
- Words (58:57) shall be equal to [(the content of word 54) * (the content of word 55) * (the content of word 56)].

8.g WRITE DMA EXT

8.g.1 Command code

35h

8.g.2 Feature set

48-bit Address feature set

Mandatory for devices implementing the 48-bit Address feature set and not implementing the PACKET Command feature set.

Use prohibited for devices implementing the PACKET Command feature set.

8.g.3 Protocol

DMA (see 9.7).

8.g.4 Inputs

0000h in the sector Count register indicates that 65,536 sectors are to be transferred.

Register		7	6	5	4	3	2	1	0
Features	Current Previous (see note)	Reserved Reserved							
Sector Count	Current Previous (see note)	Sector count (7:0) Sector count (15:8)							
Sector Number	Current Previous (see note)	LBA (7:0) LBA (31:24)							
Cylinder Low	Current Previous (see note)	LBA (15:8) LBA (39:32)							
Cylinder High	Current Previous (see note)	LBA (23:16) LBA (47:40)							
Device/Head		obs	LBA	obs	DEV	Reserved			
Command		35h							
NOTE – The value indicated as Current is the value most recently written to the register. The value indicated as Previous is the value that was in the register before the most recent write to the register.									

Sector Count Current -

number of sectors to be transferred low order, bits (7:0).

Sector Count Previous -

number of sectors to be transferred high order, bits (15:8).

Sector Number Current -

LBA (7:0).

Sector Number Previous -

LBA (31:24).

Cylinder Low Current -

LBA (15:8).

Cylinder Low Previous -

LBA (39:32).

Cylinder High Current -

LBA (23:16).

Cylinder High Previous -

LBA (47:40).

Device/Head -

LBA (bit 6) shall be set to one.
DEV shall indicate the selected device.

8.g.5 Normal outputs

Register		7	6	5	4	3	2	1	0
Error		na							
Sector Count	HOB =0				Reserved				
	HOB =1 (see note)				Reserved				
Sector Number	HOB =0				Reserved				
	HOB =1 (see note)				Reserved				
Cylinder Low	HOB =0				Reserved				
	HOB =1 (see note)				Reserved				
Cylinder High	HOB =0				Reserved				
	HOB =1 (see note)				Reserved				
Device/Head		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE – The value indicated by HOB = 0 is the value read when the HOB bit of the Device Control register is cleared to zero. The value indicated by HOB = 1 is the value read when the HOB bit of the Device Control register is set to one.									

Device/Head register –

DEV shall indicate the selected device.

Status register –

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

8.g.6 Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Register		7	6	5	4	3	2	1	0
Error		ICRC	WP	MC	IDNF	MCR	ABRT	MN	obs
Sector Count	HOB =0 HOB =1 (see note)	Reserved Reserved							
Sector Number	HOB =0 HOB =1 (see note)	LBA (7:0) LBA (31:24)							
Cylinder Low	HOB =0 HOB =1 (see note)	LBA (15:8) LBA (39:32)							
Cylinder High	HOB =0 HOB =1 (see note)	LBA (23:16) LBA (47:40)							
Device/Head		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE – The value indicated by = 0 is the value read when the HOB bit of the Device Control register is cleared to zero. The value indicated by HOB = 1 is the value read when the HOB bit of the Device Control register is set to one.									

Error register -

ICRC shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer. The content of this bit is not applicable for Multiword DMA transfers.

WP shall be set to one if the media in a removable media device is write protected.

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not supported or if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

Sector Number -

LBA (7:0) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (31:24) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Cylinder Low -

LBA (15:8) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (39:32) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Cylinder High -

LBA (23:16) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (47:40) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

8.g.7 Prerequisites

DRDY set to one. The host shall initialize the DMA channel.

8.g.8 Description

The WRITE DMA EXT command allows the host to write data using the DMA data transfer protocol.

8.h WRITE DMA QUEUED EXT

8.h.1 Command code

36h

8.h.2 Feature set

Overlapped feature set/48-bit Address feature set

- Mandatory for devices implementing the Overlapped feature set and the 48-bit Address feature set but not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET Command feature set.

8.h.3 Protocol

DMA QUEUED (see 9.9).

8.h.4 Inputs

0000h in the Features register indicates that 65,536 sectors are to be transferred.

Register		7	6	5	4	3	2	1	0
Features	Current Previous (see note)	Sector count (7:0) Sector count (15:8)							
Sector Count	Current Previous (see note)	Tag				Reserved			
		Reserved							
Sector Number	Current Previous (see note)	LBA (7:0) LBA (31:24)							
		LBA (15:8) LBA (39:32)							
Cylinder Low	Current Previous (see note)	LBA (23:16) LBA (47:40)							
		LBA (23:16) LBA (47:40)							
Device/Head		obs	LBA	obs	DEV	Reserved			
Command		36h							
NOTE – The value indicated as Current is the value most recently written to the register. The value indicated as Previous is the value that was in the register before the most recent write to the register.									

Features Current -

number of sectors to be transferred low order, bits (7:0).

Features Previous -

number of sectors to be transferred high order, bits (15:8).

Sector Count Current -

if the device supports command queuing, bits (7:3) contain the Tag for the command being delivered. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If queuing is not supported, this field is not applicable.

Sector Count Previous -

Reserved

Sector Number Current -

LBA (7:0).

Sector Number Previous -

LBA (31:24).

Cylinder Low Current -

LBA (15:8).

Cylinder Low Previous -

LBA (39:32).

Cylinder High Current -

LBA (23:16).

Cylinder High Previous -

LBA (47:40).

Device/Head -

LBA (bit 6) shall be set to one.

DEV shall indicate the selected device.

8.h.5 Normal outputs

8.h.5.1 Data transmission

Data transfer may occur after receipt of the command or may occur after the receipt of a SERVICE command. When the device is ready to transfer data requested by a data transfer command, the device sets the following register content to initiate the data transfer.

Register		7	6	5	4	3	2	1	0
Error		na							
Sector Count	HOB =0	Tag				REL	I/O	C/D	
	HOB =1 (see note)	Reserved							
Sector Number	HOB =0	Reserved							
	HOB =1 (see note)	Reserved							
Cylinder Low	HOB =0	Reserved							
	HOB =1 (see note)	Reserved							
Cylinder High	HOB =0	Reserved							
	HOB =1 (see note)	Reserved							
Device/Head		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE – The value indicated by HOB = 0 is the value read when the HOB bit of the Device Control register is cleared to zero. The value indicated by HOB = 1 is the value read when the HOB bit of the Device Control register is set to one.									

Sector Count (when bit 7 of the Device Control register is cleared to zero) -

Tag -This field contains the command Tag for the command. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If the device does not support command queuing or overlap is disabled, this field is not applicable.

REL - Shall be cleared to zero.

I/O - Shall be cleared to zero indicating the transfer is from the host.

C/D - Shall be cleared to zero indicating the transfer of data.

Device/Head register –

DEV shall indicate the selected device.

Status register –

BSY shall be cleared to zero.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

8.h.5.2 Release

If the device performs a bus release before transferring data for this command, the register content upon performing a bus release shall be as shown below.

Register		7	6	5	4	3	2	1	0
Error		na							
Sector Count	HOB =0	Tag				REL	I/O	C/D	
	HOB =1 (see note)	Reserved							
Sector Number	HOB =0	Reserved				Reserved			
	HOB =1 (see note)	Reserved							
Cylinder Low	HOB =0	Reserved				Reserved			
	HOB =1 (see note)	Reserved							
Cylinder High	HOB =0	Reserved				Reserved			
	HOB =1 (see note)	Reserved							
Device/Head		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	SERV	DRQ	na	na	ERR
NOTE – The value indicated by HOB = 0 is the value read when the HOB bit of the Device Control register is cleared to zero. The value indicated by HOB = 1 is the value read when the HOB bit of the Device Control register is set to one.									

Sector Count (when bit 7 of the Device Control register is cleared to zero) -

Tag -This field contains the command Tag for the command. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If the device does not support command queuing or overlap is disabled, this field is not applicable.

REL - Shall be set to one.

I/O - Shall be cleared to zero.

C/D - Shall be cleared to zero indicating the transfer of data.

Device/Head register –

DEV shall indicate the selected device.

Status register –

BSY shall be cleared to zero.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

SERV (Service) shall be cleared to zero when no other queued command is ready for service. SERV shall be set to one when another queued command is ready for service. SERV shall be set to one when the device has prepared this command for service.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

8.h.5.3 Service request

When the device is ready to transfer data or complete a command after the command has performed a bus release, the device shall set the SERV bit and not change the state of any other register bit (see 6.9). When the SERVICE command is received, the device shall set outputs as described in data transfer, command completion, or error outputs depending on the service the device requires.

8.h.5.4 Command completion

When the transfer of all requested data has occurred without error, the register content shall be as shown below.

Register		7	6	5	4	3	2	1	0
Error		na							
Sector Count	HOB =0	Tag				REL	I/O	C/D	
	HOB =1 (see note)	Reserved							
Sector Number	HOB =0	Reserved				Reserved			
	HOB =1 (see note)	Reserved							
Cylinder Low	HOB =0	Reserved				Reserved			
	HOB =1 (see note)	Reserved							
Cylinder High	HOB =0	Reserved				Reserved			
	HOB =1 (see note)	Reserved							
Device/Head		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	SERV	DRQ	na	na	ERR
NOTE – The value indicated by HOB = 0 is the value read when the HOB bit of the Device Control register is cleared to zero. The value indicated by HOB = 1 is the value read when the HOB bit of the Device Control register is set to one.									

Sector Count (when bit 7 of the Device Control register is cleared to zero) -

Tag -This field contains the command Tag for the command. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If the device does not support command queuing or overlap is disabled, this field is not applicable.

REL - Shall be cleared to zero.

I/O - Shall be set to one.

C/D - Shall be set to one.

Device/Head register –

DEV shall indicate the selected device.

Status register –

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

SERV (Service) shall be cleared to zero when no other queued command is ready for service. SERV shall be set to one when another queued command is ready for service.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

8.h.6 Error outputs

The Sector Count register contains the Tag for this command if the device supports command queuing. The device shall return command aborted if the command is not supported or if the device has not had overlapped interrupt enabled. The device shall return command aborted if the device supports command queuing and the Tag is invalid. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector where the first unrecoverable error occurred. If a queue existed, the unrecoverable error shall cause the queue to abort.

Register		7	6	5	4	3	2	1	0
Error		ICRC	WP	MC	IDNF	MCR	ABRT	MN	obs
Sector Count	HOB =0	Tag					REL	I/O	C/D
	HOB =1 (see note)	Reserved							
Sector Number	HOB =0				LBA (7:0)				
	HOB =1 (see note)				LBA (31:24)				
Cylinder Low	HOB =0				LBA (15:8)				
	HOB =1 (see note)				LBA (39:32)				
Cylinder High	HOB =0				LBA (23:16)				
	=1 (see note)				LBA (47:40)				
Device/Head		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	SERV	DRQ	na	na	ERR
NOTE – The value indicated by = 0 is the value read when the HOB bit of the Device Control register is cleared to zero. The value indicated by HOB = 1 is the value read when the HOB bit of the Device Control register is set to one.									

Error register -

ICRC shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer. The content of this bit is not applicable for Multiword DMA transfers.

WP shall be set to one if the media in a removable media device is write protected.

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not supported or if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

Sector Count (when bit 7 of the Device Control register is cleared to zero) -

Tag -This field contains the command Tag for the command. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If the device does not support command queuing or overlap is disabled, this field is not applicable.

REL - Shall be cleared to zero.

I/O - Shall be set to one.

C/D - Shall be set to one.

Sector Number -

LBA (7:0) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (31:24) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Cylinder Low -

LBA (15:8) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (39:32) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Cylinder High -

LBA (23:16) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (47:40) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

8.h.7 Prerequisites

DRDY set to one. The host shall initialize the DMA channel.

8.h.8 Description

This command executes in a similar manner to a WRITE DMA EXT command. The device may perform a bus release the bus or may execute the data transfer without performing a bus release if the data is ready to transfer.

If the device performs a bus release, the host shall reselect the device using the SERVICE command.

Once the data transfer is begun, the device shall not perform a bus release until the entire data transfer has been completed.

8.k WRITE MULTIPLE EXT

8.k.1 Command code

39h

8.k.2 Feature set

48-bit Address feature set

- Mandatory for devices implementing the 48-bit Address feature set and not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET Command feature set.

8.k.3 Protocol

PIO data-out (see 9.6).

8.k.4 Inputs

0000h in the sector Count register indicates that 65,536 sectors are to be transferred.

Register		7	6	5	4	3	2	1	0
Features	Current Previous (see note)	Reserved Reserved							
Sector Count	Current Previous (see note)	Sector count (7:0) Sector count (15:8)							
Sector Number	Current Previous (see note)	LBA (7:0) LBA (31:24)							
Cylinder Low	Current Previous (see note)	LBA (15:8) LBA (39:32)							
Cylinder High	Current Previous (see note)	LBA (23:16) LBA (47:40)							
Device/Head		obs	LBA	obs	DEV	Reserved			
Command		39h							
NOTE – The value indicated as Current is the value most recently written to the register. The value indicated as Previous is the value that was in the register before the most recent write to the register.									

- Sector Count Current -
number of sectors to be transferred low order, bits (7:0).
- Sector Count Previous -
number of sectors to be transferred high order, bits (15:8).
- Sector Number Current -
LBA (7:0).
- Sector Number Previous -
LBA (31:24).
- Cylinder Low Current -
LBA (15:8).
- Cylinder Low Previous -
LBA (39:32).
- Cylinder High Current -
LBA (23:16).
- Cylinder High Previous -
LBA (47:40).
- Device/Head -
LBA (bit 6) shall be set to one.
DEV shall indicate the selected device.

8.k.5 Normal outputs

Register		7	6	5	4	3	2	1	0
Error		na							
Sector Count	HOB=0				Reserved				
	HOB =1 (see note)				Reserved				
Sector Number	HOB =0				Reserved				
	HOB =1 (see note)				Reserved				
Cylinder Low	HOB =0				Reserved				
	HOB =1 (see note)				Reserved				
Cylinder High	HOB =0				Reserved				
	HOB =1 (see note)				Reserved				
Device/Head		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE – The value indicated by HOB = 0 is the value read when the HOB bit of the Device Control register is cleared to zero. The value indicated by HOB = 1 is the value read when the HOB bit of the Device Control register is set to one.									

Device/Head register –

DEV shall indicate the selected device.

Status register –

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

8.i.6 Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Register		7	6	5	4	3	2	1	0
Error		na	WP	MC	IDNF	MCR	ABRT	NM	obs
Sector Count	HOB =0 HOB =1 (see note)	Reserved Reserved							
Sector Number	HOB =0 HOB =1 (see note)	LBA (7:0) LBA (31:24)							
Cylinder Low	HOB =0 HOB =1 (see note)	LBA (15:8) LBA (39:32)							
Cylinder High	HOB =0 HOB =1 (see note)	LBA (23:16) LBA (47:40)							
Device/Head		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE – The value indicated by HOB = 0 is the value read when the HOB bit of the Device Control register is cleared to zero. The value indicated by HOB = 1 is the value read when the HOB bit of the Device Control register is set to one.									

Error register -

WP shall be set to one if the media in a removable media device is write protected.

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

Sector Number -

LBA (7:0) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (31:24) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Cylinder Low -

LBA (15:8) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (39:32) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Cylinder High -

LBA (23:16) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (47:40) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.
 DF (Device Fault) shall be set to one if a device fault has occurred.
 DRQ shall be cleared to zero.
 ERR shall be set to one if an Error register bit is set to one.

8.k.7 Prerequisites

DRDY set to one. If bit 8 of IDENTIFY DEVICE word 59 is cleared to zero, a successful SET MULTIPLE MODE command shall proceed a WRITE MULTIPLE EXT command.

8.k.8 Description

The WRITE MULTIPLE EXT command performs the same as the WRITE SECTOR(S) command except that the device does not a) set DF, as required, b) set ERR and the bits in the Error register, as required, c) clear DRQ and BSY, and d) assert INTRQ until data is transferred for all sectors in the block. Data for all of the other sectors in the block are transferred without the device asserting INTRQ. In addition, the DRQ qualification of the transfer is required only before the first sector of a block, not before each sector of the block.

The number of sectors per block is defined by a successful SET MULTIPLE command. If no successful SET MULTIPLE command has been issued, the block is defined by the device's default value for number of sectors per block as defined in bits 0-7 in word 47 in the IDENTIFY DEVICE information.

If bit 8 is set to one and bits 0-7 are cleared to zero in word 59 in the IDENTIFY DEVICE information, then the block count of sectors to be transferred without intervening interrupts shall be programmed by the SET MULTIPLE MODE command before issuing the first WRITE MULTIPLE EXT command after a power-on or hardware reset. If bit 8 in word 1 is set to one and bits 0-7 are not cleared to zero in word 59 in the IDENTIFY DEVICE information, then the block count of sectors to be transferred without intervening interrupts may be reprogrammed by the SET MULTIPLE MODE command before issuing the next WRITE MULTIPLE EXT command.

When the WRITE MULTIPLE EXT command is issued, the Sector Count register contains the number of sectors (not the number of blocks) requested.

If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

$$n = \text{Remainder (sector count/ block count)}.$$

If the WRITE MULTIPLE EXT command is received when WRITE MULTIPLE EXT commands are disabled, the Write Multiple operation shall be rejected with command aborted.

Device errors encountered during WRITE MULTIPLE EXT commands are posted after the attempted device write of the block or partial block transferred. The command ends with the sector in error, even if the error was in the middle of a block. Subsequent blocks are not transferred in the event of an error.

The contents of the Command Block Registers following the transfer of a data block that had a sector in error are undefined. The host should retry the transfer as individual requests to obtain valid error information. Interrupt pending is set when the DRQ bit is set to one at the beginning of each block or partial block.

8.i WRITE SECTOR(S) EXT

8.i.1 Command code

34h

8.i.2 Feature set

48-bit Address feature set

- Mandatory for devices implementing the 48-bit Address feature set and not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET Command feature set.

8.i.3 Protocol

PIO data-out (see 9.6).

8.i.4 Inputs

0000h in the sector Count register indicates that 65,536 sectors are to be transferred.

Register		7	6	5	4	3	2	1	0
Features	Current Previous (see note)	Reserved Reserved							
Sector Count	Current Previous (see note)	Sector count (7:0) Sector count (15:8)							
Sector Number	Current Previous (see note)	LBA (7:0) LBA (31:24)							
Cylinder Low	Current Previous (see note)	LBA (15:8) LBA (39:32)							
Cylinder High	Current Previous (see note)	LBA (23:16) LBA (47:40)							
Device/Head		obs	LBA	obs	DEV	Reserved			
Command		34h							
NOTE – The value indicated as Current is the value most recently written to the register. The value indicated as Previous is the value that was in the register before the most recent write to the register.									

Sector Count Current -

number of sectors to be transferred low order, bits (7:0).

Sector Count Previous -

number of sectors to be transferred high order, bits (15:8).

Sector Number Current -

LBA (7:0).

Sector Number Previous -

LBA (31:24).

Cylinder Low Current -

LBA (15:8).

Cylinder Low Previous -
LBA (39:32).
Cylinder High Current -
LBA (23:16).
Cylinder High Previous -
LBA (47:40).
Device/Head -
LBA (bit 6) shall be set to one.
DEV shall indicate the selected device.

8.i.5 Normal outputs

Register		7	6	5	4	3	2	1	0
Error		na							
Sector Count	HOB=0	Reserved				Reserved			
	HOB =1 (see note)	Reserved				Reserved			
Sector Number	HOB =0	Reserved				Reserved			
	HOB =1 (see note)	Reserved				Reserved			
Cylinder Low	HOB =0	Reserved				Reserved			
	HOB =1 (see note)	Reserved				Reserved			
Cylinder High	HOB =0	Reserved				Reserved			
	HOB =1 (see note)	Reserved				Reserved			
Device/Head		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE – The value indicated by HOB = 0 is the value read when the HOB bit of the Device Control register is cleared to zero. The value indicated by HOB = 1 is the value read when the HOB bit of the Device Control register is set to one.									

Device/Head register –
DEV shall indicate the selected device.

Status register –
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

8.i.6 Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Register		7	6	5	4	3	2	1	0
Error		na	WP	MC	IDNF	MCR	ABRT	NM	obs
Sector Count	HOB =0 HOB =1 (see note)	Reserved Reserved							
Sector Number	HOB =0 HOB =1 (see note)	LBA (7:0) LBA (31:24)							
Cylinder Low	HOB =0 HOB =1 (see note)	LBA (15:8) LBA (39:32)							
Cylinder High	HOB =0 HOB =1 (see note)	LBA (23:16) LBA (47:40)							
Device/Head		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE – The value indicated by HOB = 0 is the value read when the HOB bit of the Device Control register is cleared to zero. The value indicated by HOB = 1 is the value read when the HOB bit of the Device Control register is set to one.									

Error register -

WP shall be set to one if the media in a removable media device is write protected.

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

Sector Number -

LBA (7:0) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (31:24) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Cylinder Low -

LBA (15:8) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (39:32) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Cylinder High -

LBA (23:16) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (47:40) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Device/Head register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.
 DF (Device Fault) shall be set to one if a device fault has occurred.
 DRQ shall be cleared to zero.
 ERR shall be set to one if an Error register bit is set to one.

8.i.7 Prerequisites

DRDY set to one.

8.i.8 Description

This command writes from 1 to 65,536 sectors as specified in the Sector Count register. A sector count of 0 requests 65,536 sectors.

In Annex F

Add the following to tables F.1, F.2., and F.3.

Table F.1 .

	x0	x1	x2	x3	x4	x5	x6	x7	x8	x9	xA	xB	xC	xD	xE	xF
2x	C	O	O	O	C	C	C	C	R	C	R	R	R	R	R	R
3x	C	O	O	O	C	C	C	C	C	C	R	R	O	R	R	R
4x	C	O	C	R	R	R	R	R	R	R	R	R	R	R	R	R

Table F.2 .

Command name	Command code
READ SECTOR(S) EXT	24h
READ DMA EXT	25h
READ DMA QUEUED EXT	26h
READ MULTIPLE EXT	29h
READ NATIVE MAX ADDRESS EXT	27h
WRITE SECTOR(S) EXT	34h
<u>READ VERIFY SECTOR(S) EXT</u>	<u>42h</u>
WRITE DMA EXT	35h
WRITE DMA QUEUED EXT	36h
WRITE MULTIPLE EXT	39h
SET MAX ADDRESS EXT	37h
FLUSH CACHE EXT	EAh

Table F.3

proto	Command	typ	PKT fea	Command code	Parameters used				
					FR	SC	SN	CY	DH
ND	FLUSH CACHE EXT	O	N	EAh		y	y	y	y
DM	READ DMA EXT	O	N	25h		y	y	y	y
DMO	READ DMA QUEUED EXT	O	N	26h	y	y	y	y	y
PI	READ MULTIPLE EXT	O	N	29h		y	y	y	y
ND	READ NATIVE MAX ADDRESS EXT	O	N	27h					D
PI	READ SECTOR(S) EXT	O	N	24h		y	y	y	y
<u>ND</u>	<u>READ VERIFY SECTOR(S) EXT</u>	<u>O</u>	<u>N</u>	<u>42h</u>		<u>y</u>	<u>y</u>	<u>y</u>	<u>y</u>
ND	SET MAX ADDRESS EXT	O	N	37h		y	y	y	y
DM	WRITE DMA EXT	O	N	35h		y	y	y	y

DMO	WRITE DMA QUEUED EXT	O	N	36h	y	y	y	y	y
PO	WRITE MULTIPLE EXT	O	N	39h		y	y	y	y
PO	WRITE SECTOR(S) EXT	O	N	34h		y	y	y	y