

Multiword DMA Timing Diagram Proposal

D99132R0

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31 September 1999

As requested at the August plenary meeting, I have created a set of timing diagrams for Multiword DMA that are similar to the Ultra DMA timing diagrams in that a separate diagram is presented to show initiation, continuation, and termination of a Multiword DMA data burst.

It is proposed that clause 10.2.3 be replaced with the following:

10.2.3 Multiword DMA data transfer

Figure aa through figure xx define the timings associated with Multiword DMA transfers.

Table zz contains the values for the timings for each of the Multiword DMA modes.

For Multiword DMA modes 1 and above, the minimum value of t_0 is specified by word 65 in the IDENTIFY DEVICE parameter list. Table zz defines the minimum value that shall be placed in word 65.

Devices shall power up with mode 0 as the default Multiword DMA mode.

Table zz– Multiword DMA data transfer

Multiword DMA timing parameters		Mode 0 ns	Mode 1 ns	Mode 2 ns	Note
t_0	Cycle time (min)	480	150	120	see note
t_D	DIOR-/DIOW- asserted pulse width (min)	215	80	70	see note
t_E	DIOR- data access (max)	150	60	50	
t_F	DIOR- data hold (min)	5	5	5	
t_G	DIOR-/DIOW- data setup (min)	100	30	20	
t_H	DIOW- data hold (min)	20	15	10	
t_I	DMACK to DIOR-/DIOW- setup (min)	0	0	0	
t_J	DIOR-/DIOW- to DMACK hold (min)	20	5	5	
t_{KR}	DIOR- negated pulse width (min)	50	50	25	see note
t_{KW}	DIOW- negated pulse width (min)	215	50	25	see note
t_{LR}	DIOR- to DMARQ delay (max)	120	40	35	
t_{LW}	DIOW- to DMARQ delay (max)	40	40	35	
t_M	CS(1:0) valid to DIOR-/DIOW- (min)	50	30	25	
t_N	CS(1:0) hold (min)	15	10	10	
t_Z	DMACK- to read data released (max)	20	25	25	

NOTE – t_0 is the minimum total cycle time, t_D is the minimum DIOR-/DIOW- assertion time, and t_k (t_{KR} or t_{KW} , as appropriate) is the minimum DIOR-/DIOW- negation time. A host shall lengthen t_D and/or t_k to ensure that t_0 is equal to the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any legal host implementation.

10.2.3.1 Initiating a Multiword DMA burst

The values for the timings for each of the Multiword DMA modes are contained in 10.2.3.

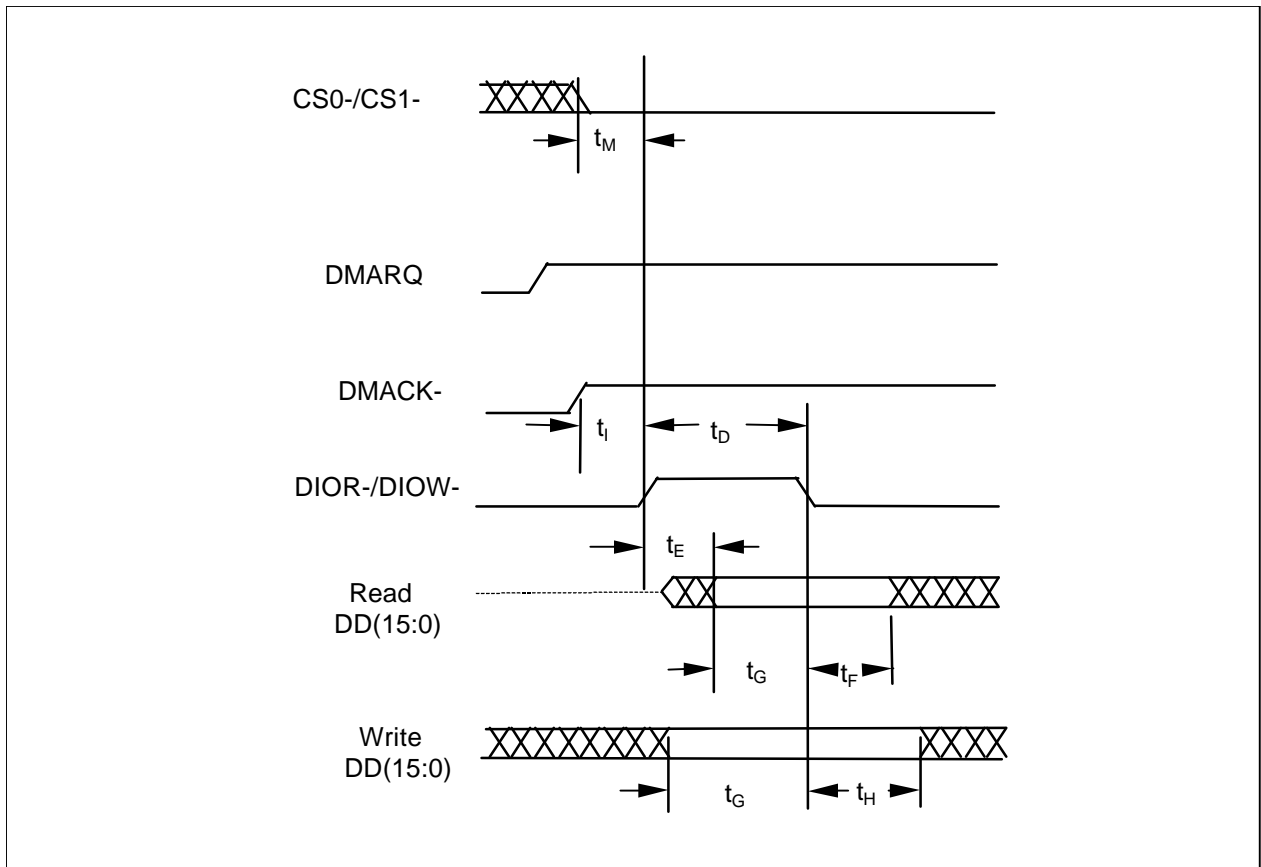


Figure aa – Initiating a Multiword DMA data transfer

10.2.3.2 Sustained Multiword DMA burst

The values for the timings for each of the Multiword DMA modes are contained in 10.2.3.

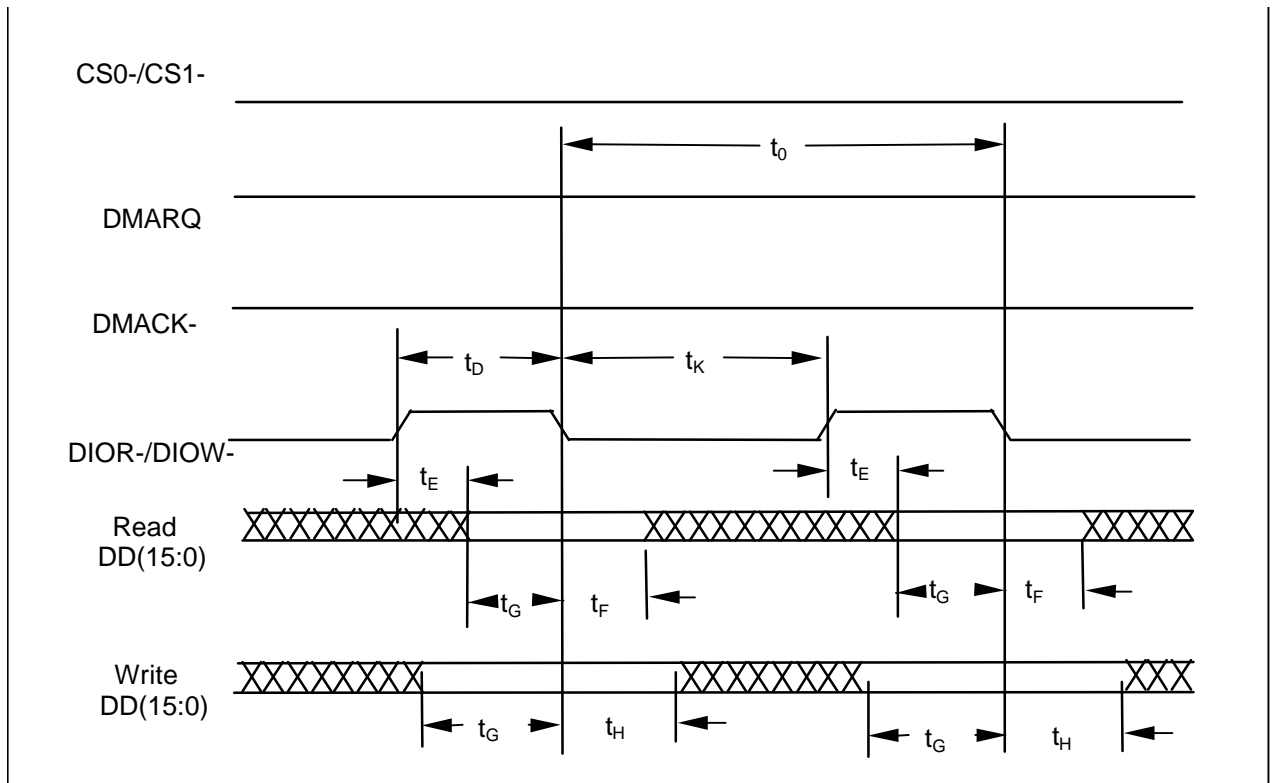


Figure bb – Sustained Multiword DMA data transfer

10.2.3.3 Device terminating a Multiword DMA burst

The values for the timings for each of the Multiword DMA modes are contained in 10.2.3.

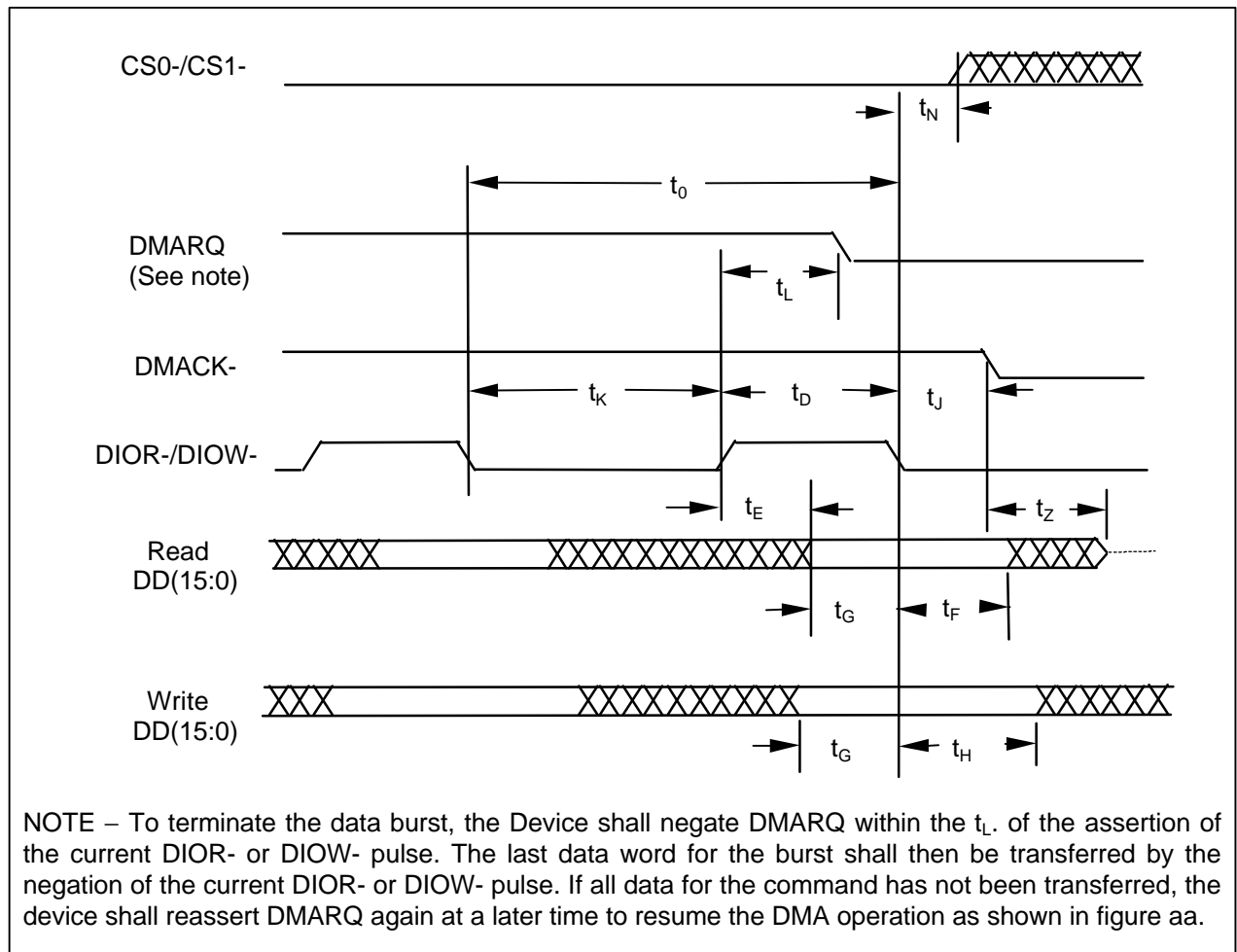


Figure cc – Device terminating a Multiword DMA data transfer

10.2.3.4 Host terminating a Multiword DMA burst

The values for the timings for each of the Multiword DMA modes are contained in 10.2.3.

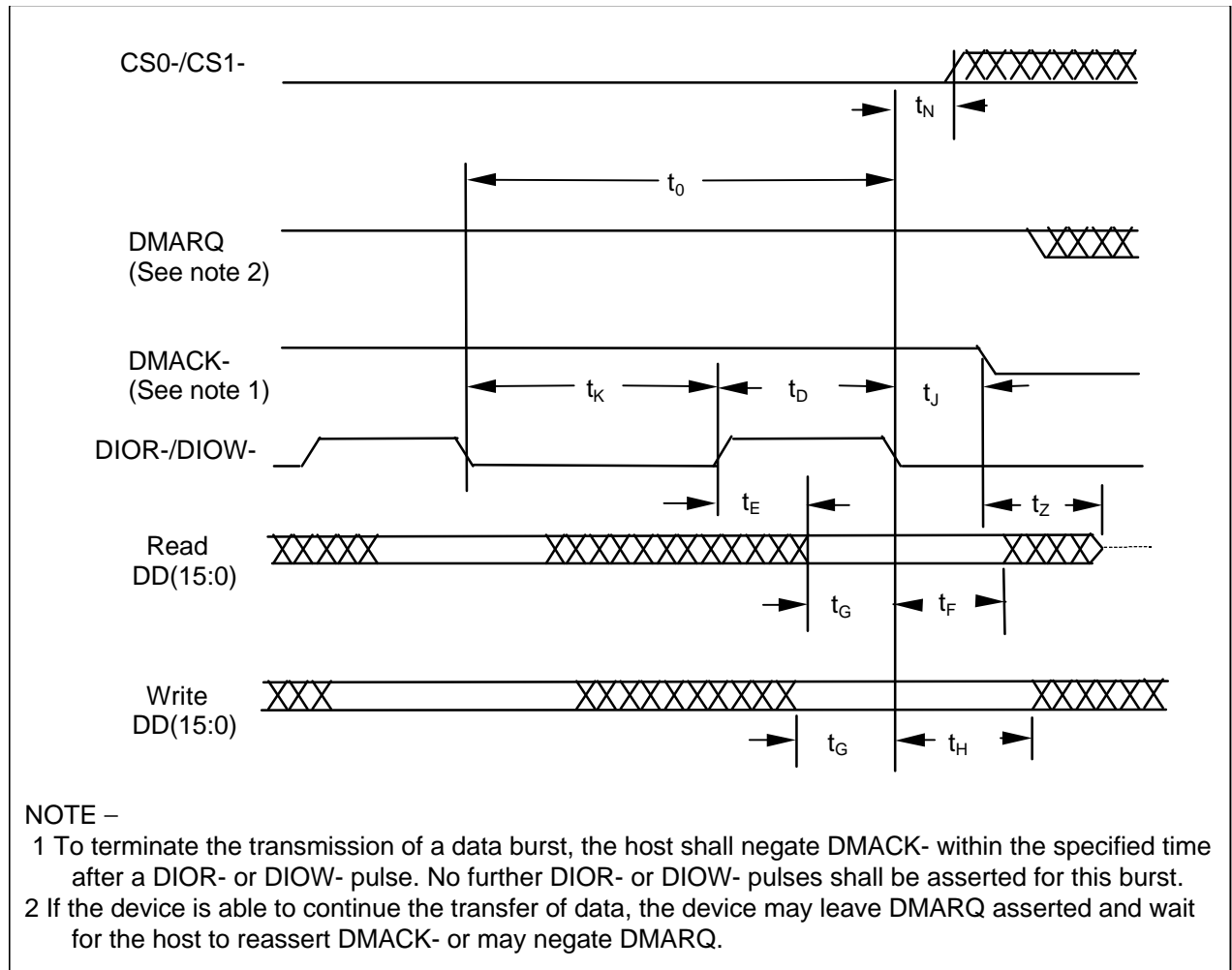


Figure dd – Host terminating a Multiword DMA data transfer