

93-165KX

LOCAL BUS PHYSICAL INTERFACE SIMULATION RESULTS

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The circuit used for the simulations is shown in figure one. This is the circuit as agreed upon in the last meeting. The termination on the host side is a 51 ohm series resistor while the termination on the hard drive side is 2.6k/4k ($V_{th}=3V$, $R_{th}=1575\text{ ohm}$). The capacitors C1, C2, and C3 were varied in the simulations (15pF, 20pF, 25pF) to help determine what a maximum node capacitance could be. The cable length used was 4 inches so that t_d was 0.5nS for T1 and T2 ($Z_o=75\text{ ohms}$). With the cable that short the transmission lines had no effect in the simulations. The simulations were run with a wired or driver and with a negation driver with an output current of 10mA. The frequencies used were 11MHz (90nS period 50% duty cycle) and 22MHz (45nS period 50% duty). The following table summarizes the results;

PERIOD(50% DUTY)	CAP(C1,C2,C3)	Vda(NEGATION 10mA)	Vda(WIRED OR)
90nS	15pF	3.6V	1.7V
90nS	20pF	3.2V	1.55V
90nS	25pF	2.75V	1.4V
45nS	15pF	2.5V	1.15V
45nS	20pF	2.25V	1V
45nS	25pF	2.2V	0.9V

The graphical outputs on pages 1 thru 12 correlate to the above numbers and show the voltage at node 6 (corresponding to node 6 figure 1) and the driver current (including negation current where appropriate). Simulation results show that with the setup in figure one that a wired or driver can't be used if a 2V step is needed. The negation driver was adequate in all cases (depending on V_{ih} of the receiver).

In this meeting I think the following questions need to be answered (and agreed on):

- 1) receiver characteristics
- 2) maximum allowed node capacitance (what is reasonable in practice)
- 3) maximum cable length (is 4 inches acceptable)
- 4) will wired or drivers be used
- 5) what should the driver current be

When the receiver characteristics, maximum node capacitance, and the maximum cable length are defined then the driver characteristics and termination can be defined.

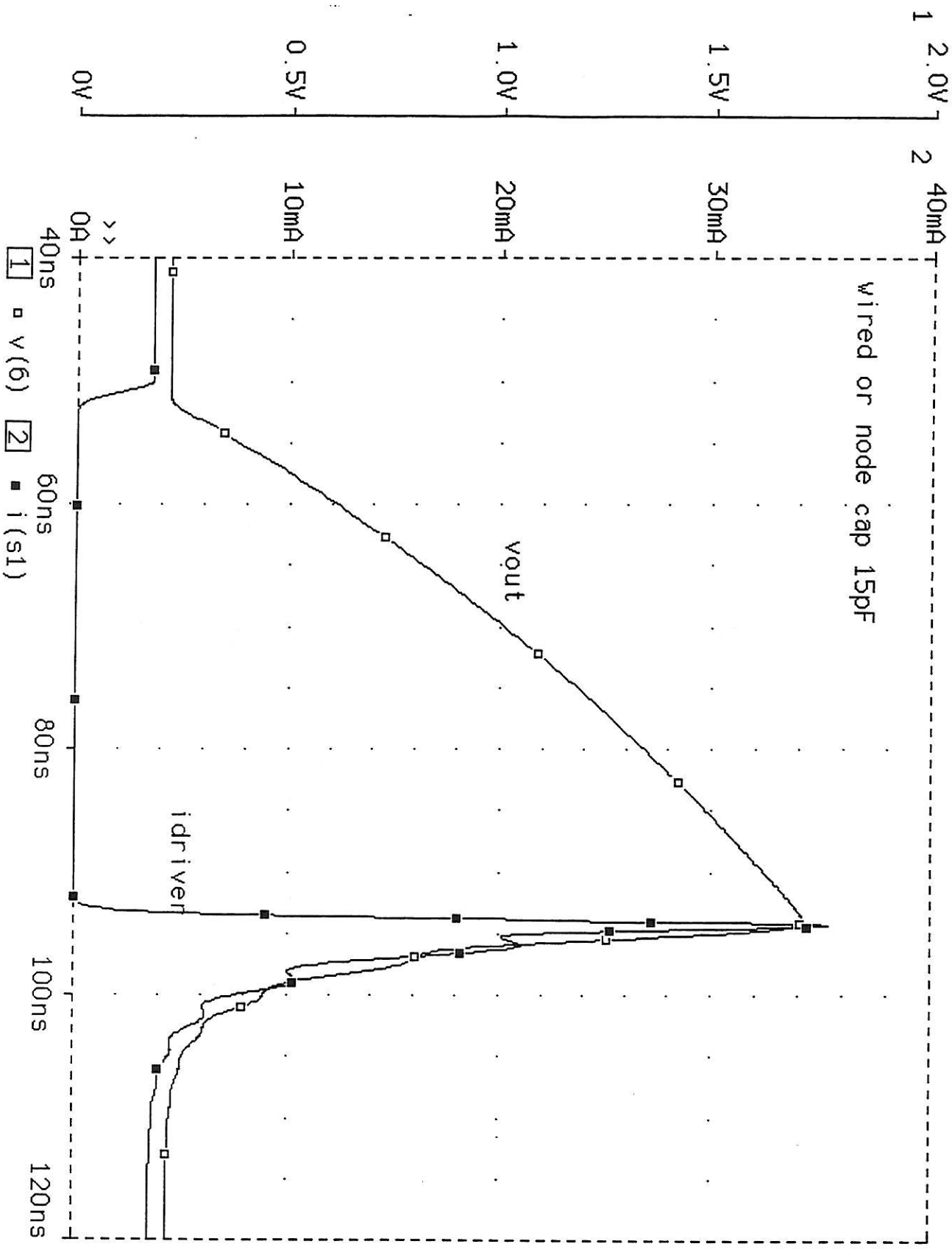


fig 1

Date/Time run: 10/13/93

ide physical interface circuit

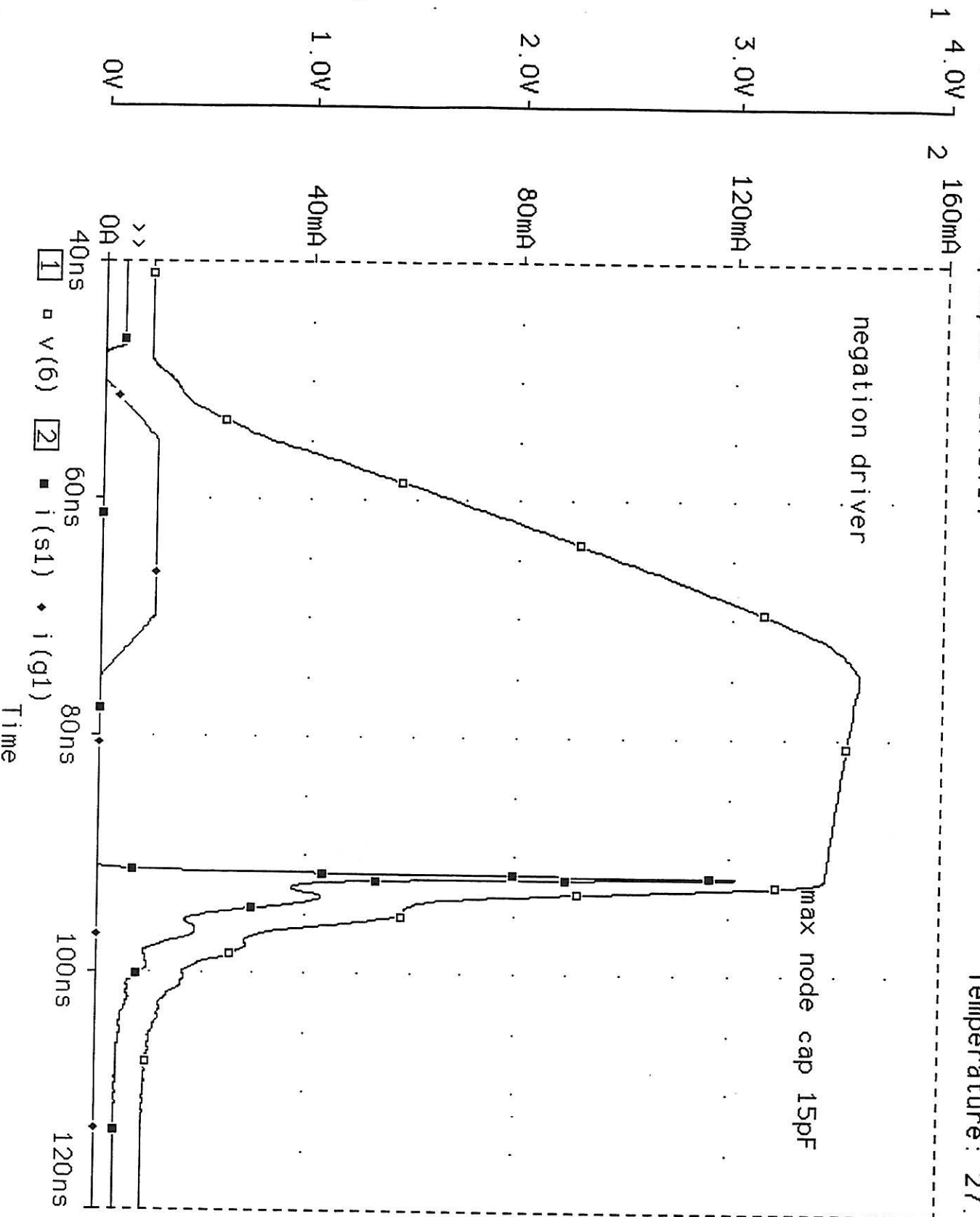
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Date/Time run: 10/12/93 10:43:14

ide physical interface circuit

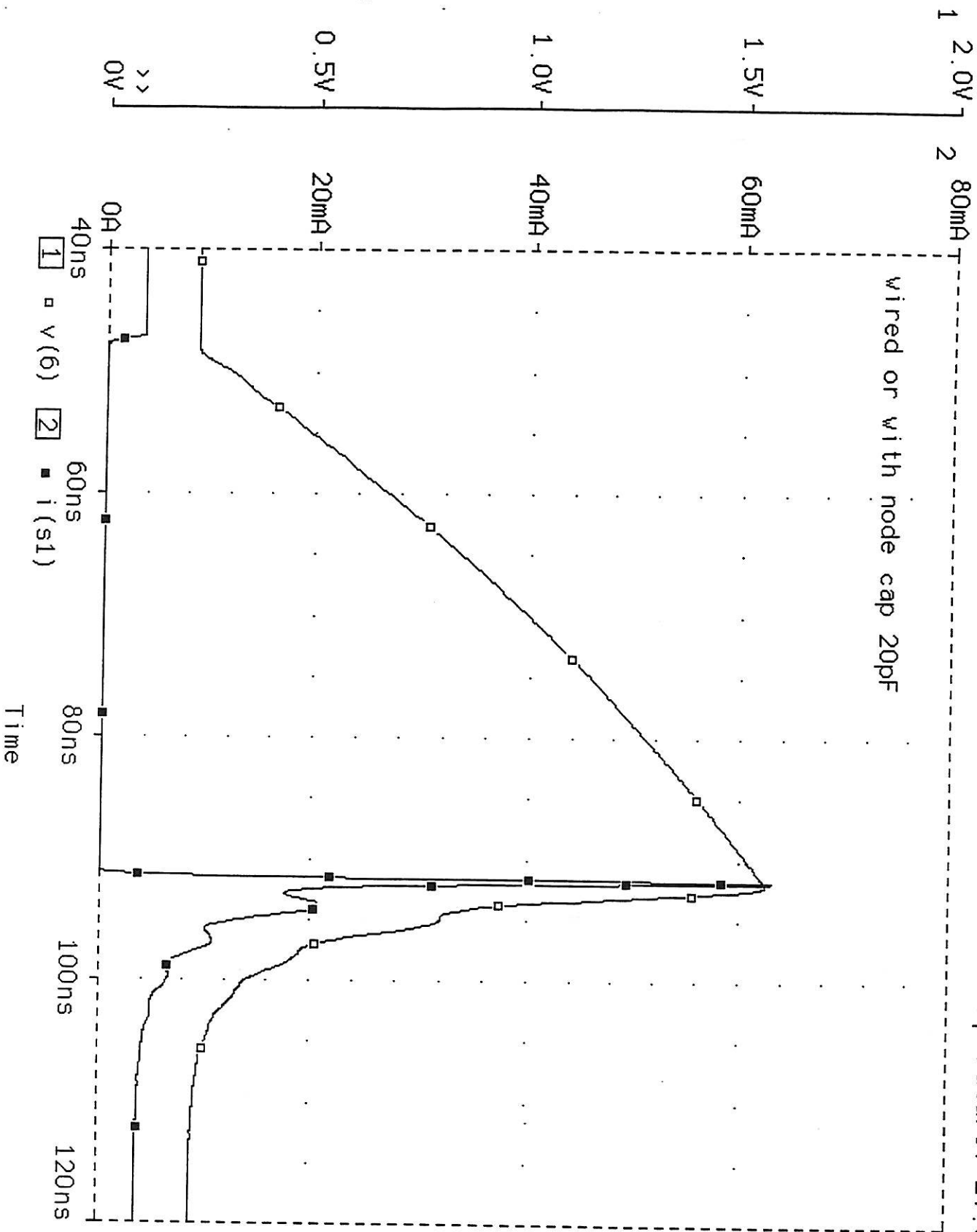
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Date/Time run: 10/13/93

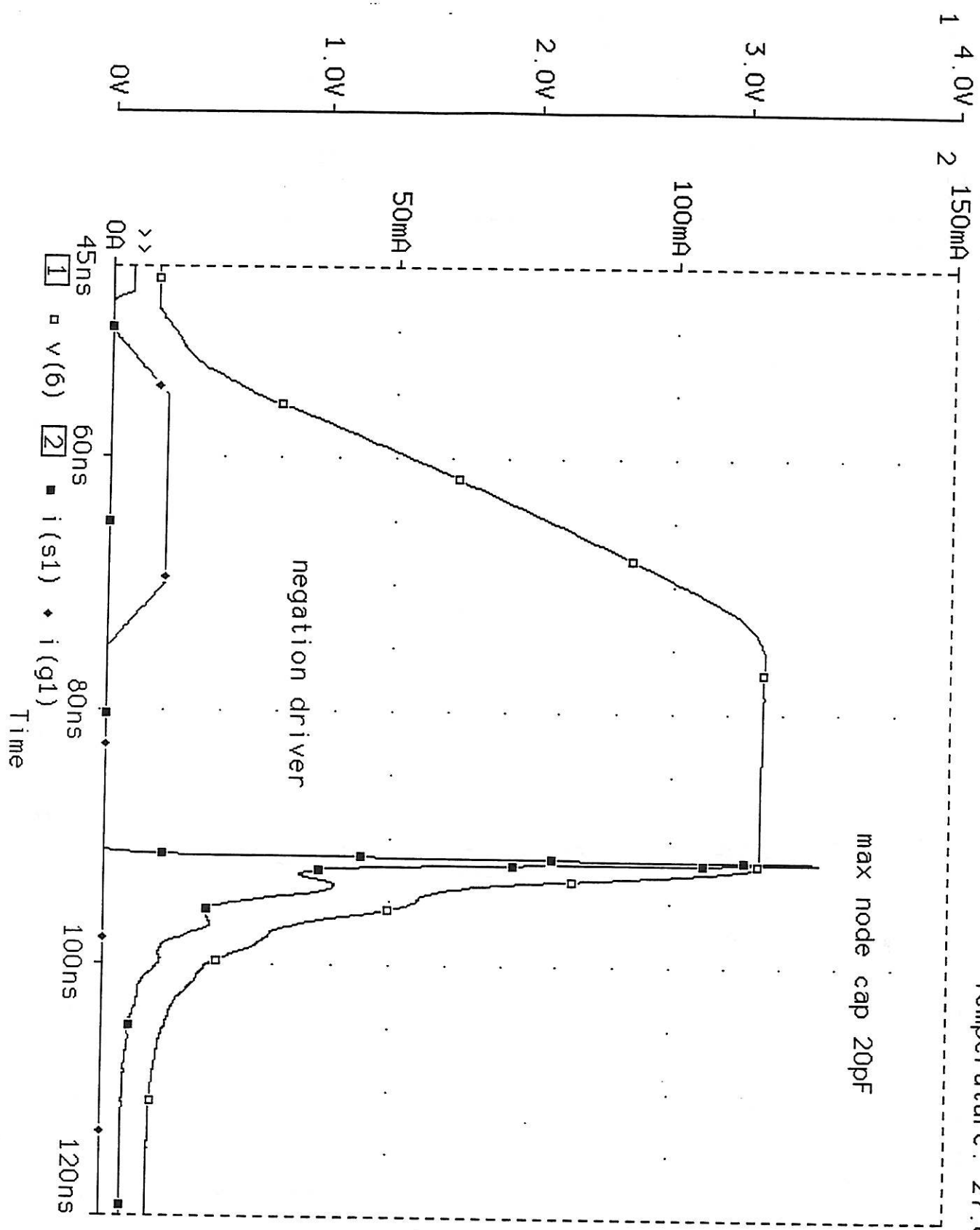
ide physical interface circuit

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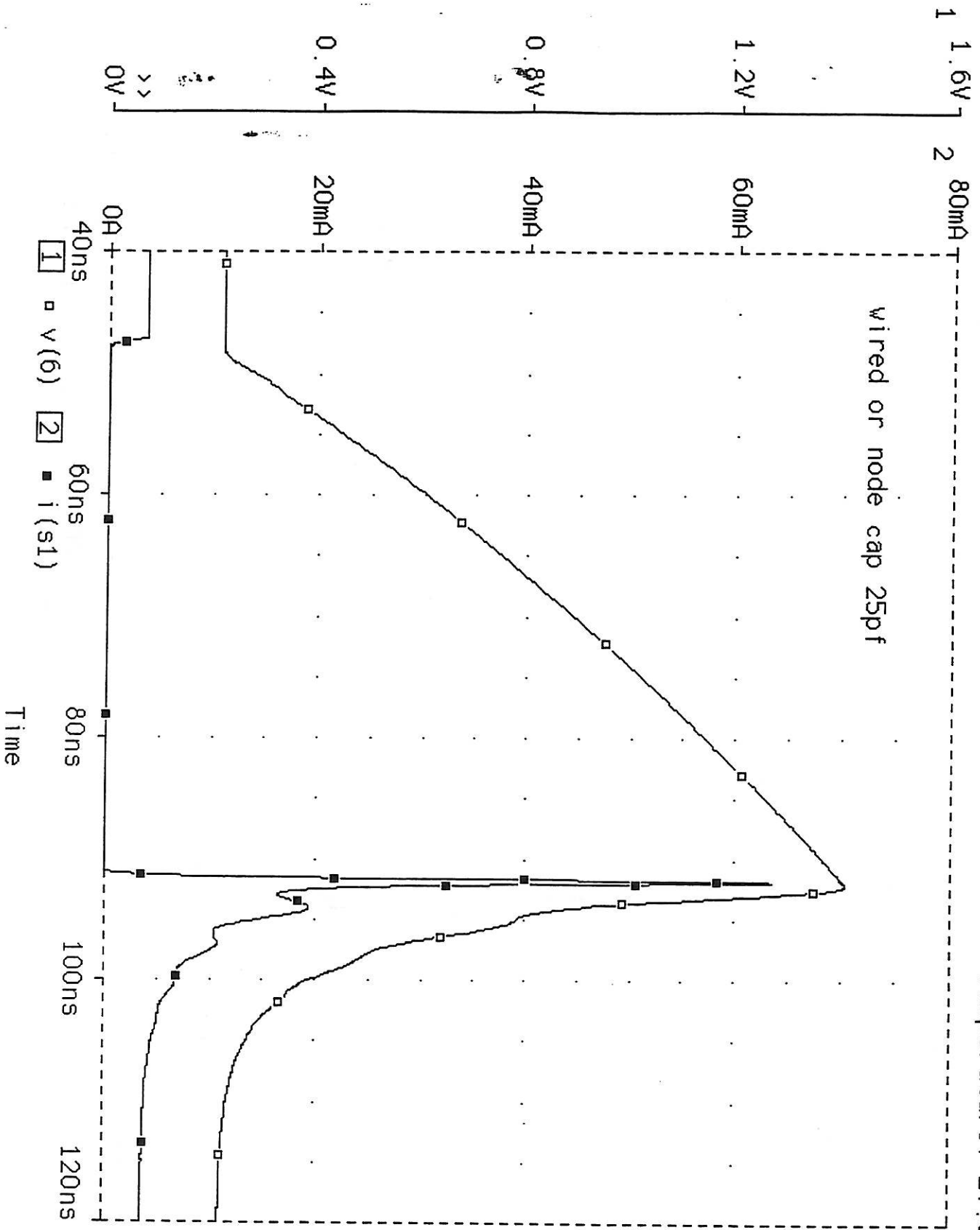
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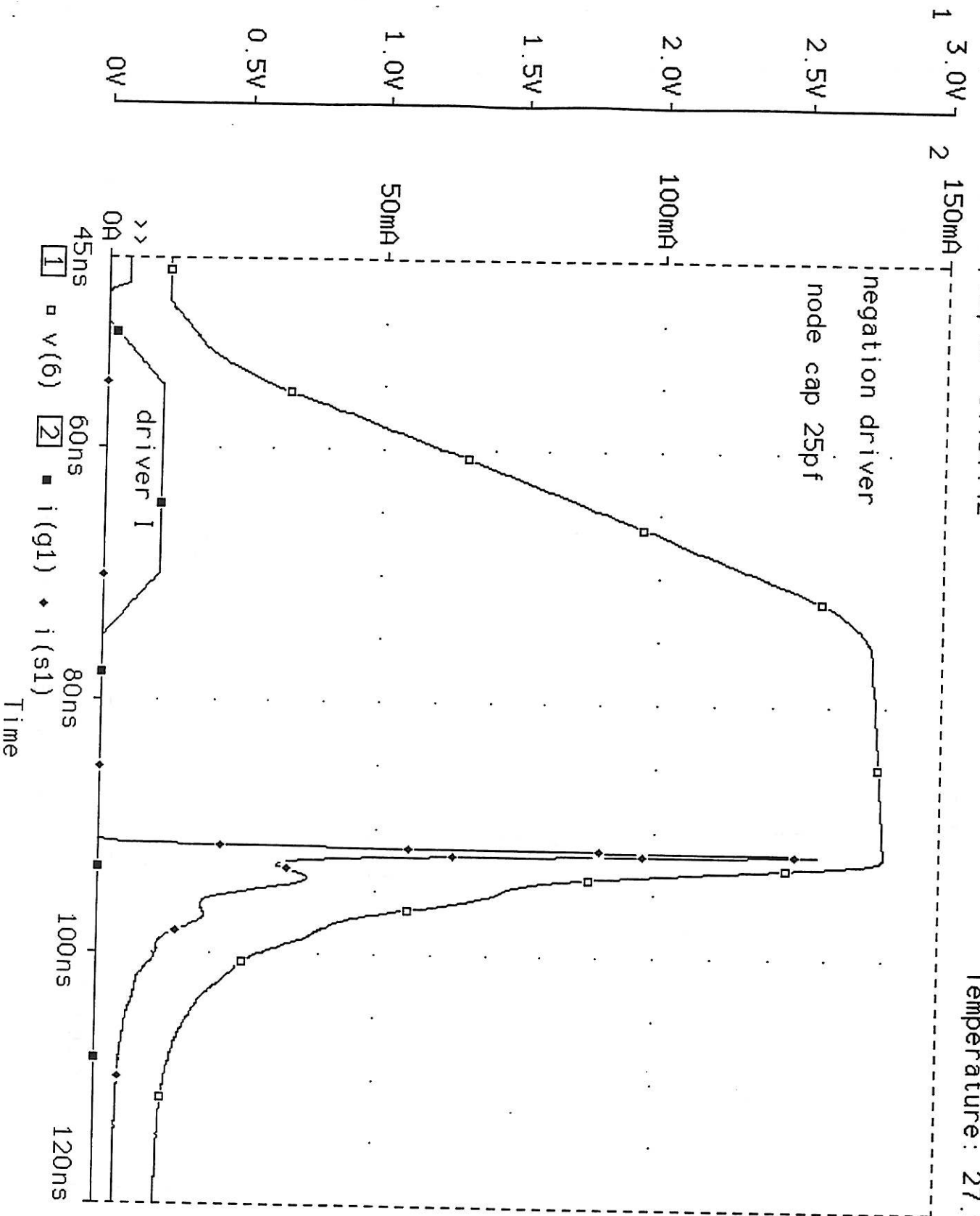
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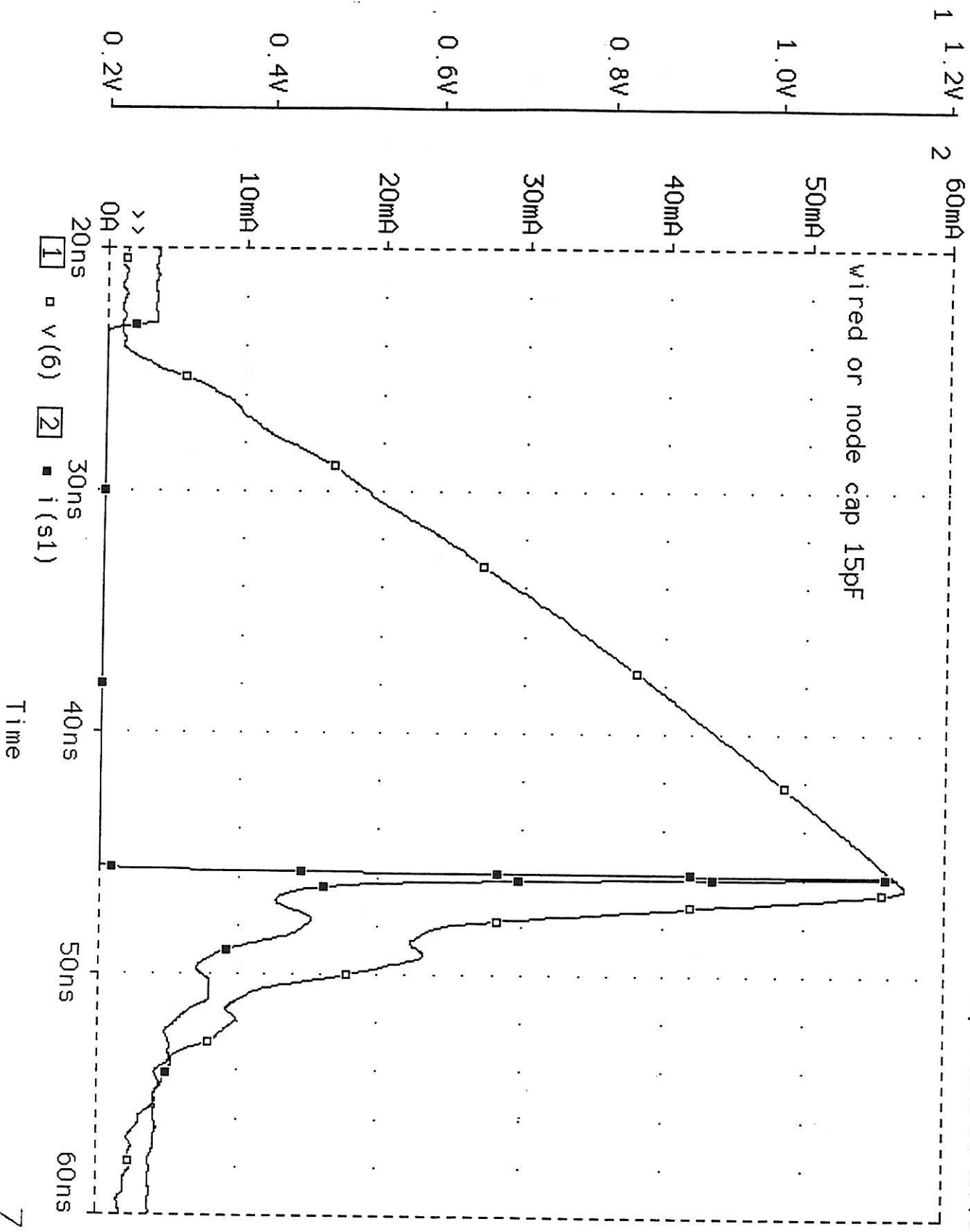
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Temperature: 27.0



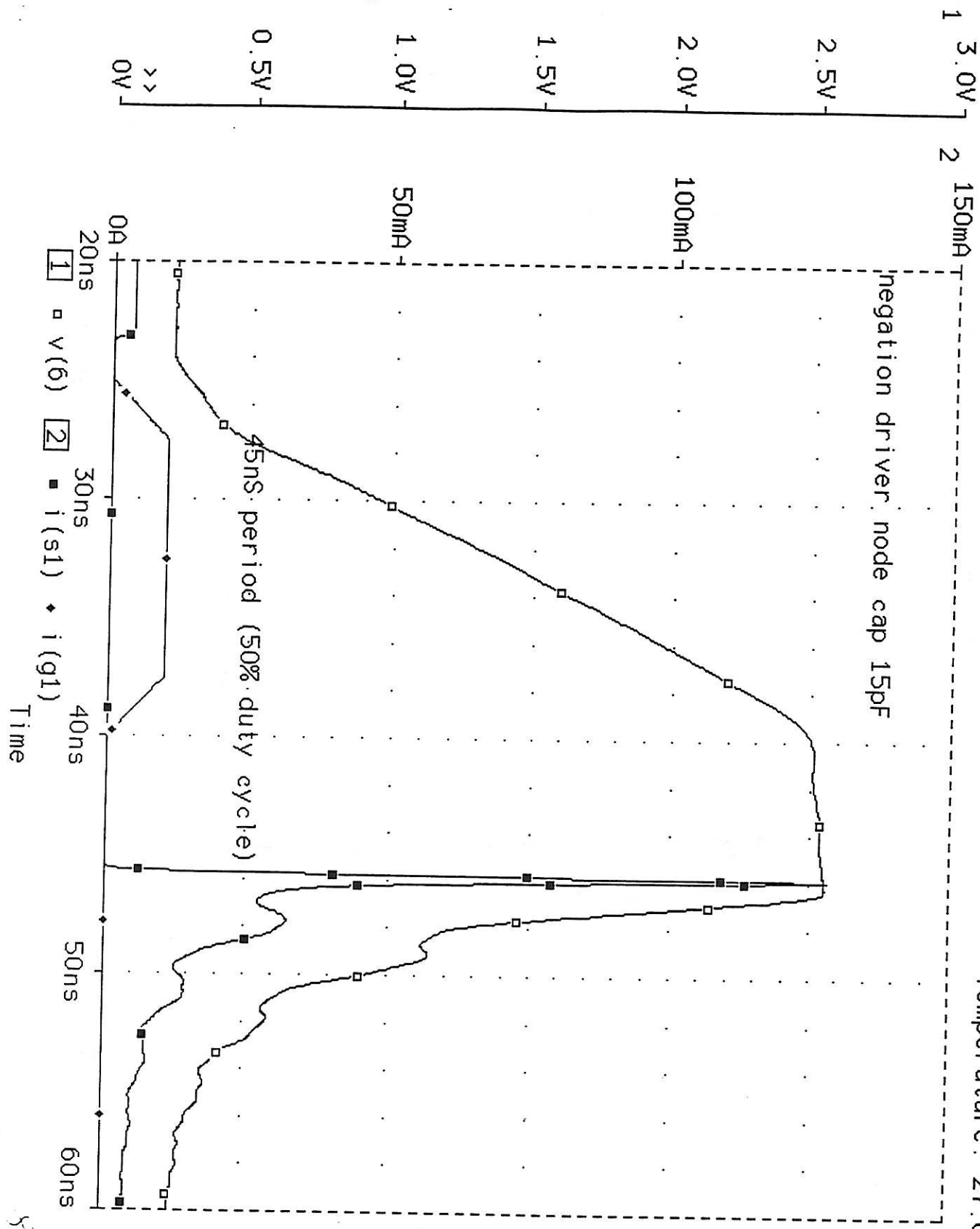
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Temperature: 27.0



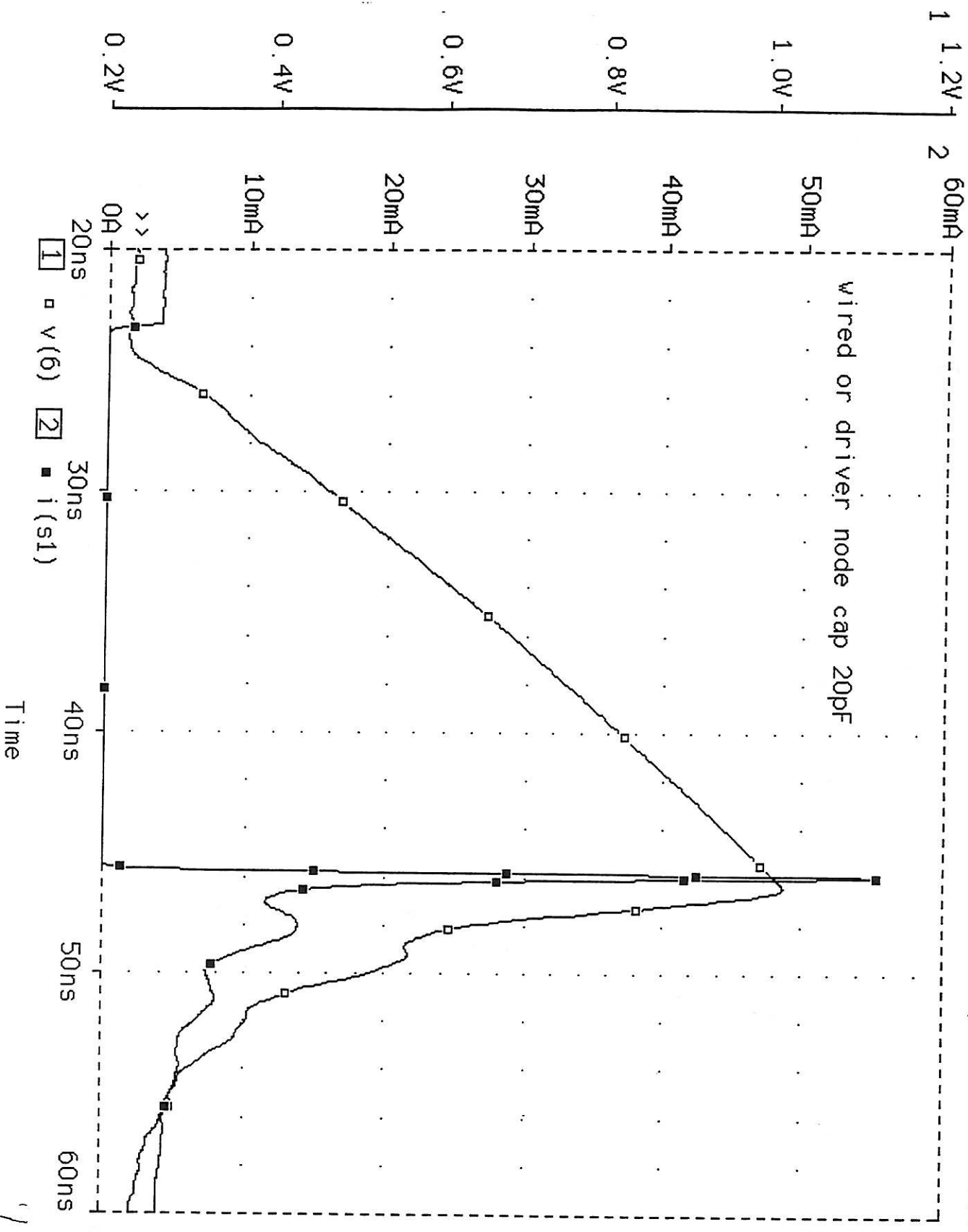
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Temperature: 27.0



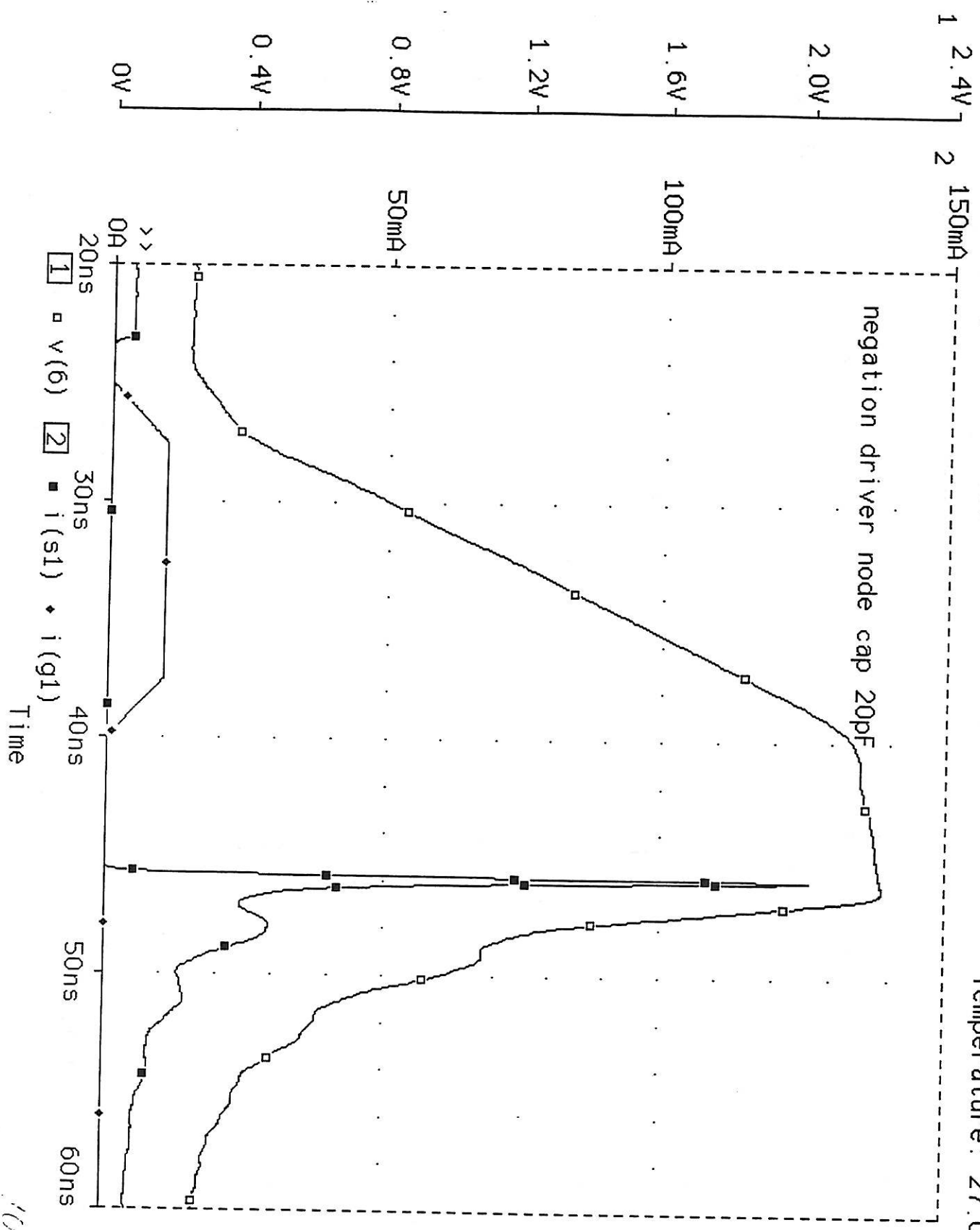
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Temperature: 27.0



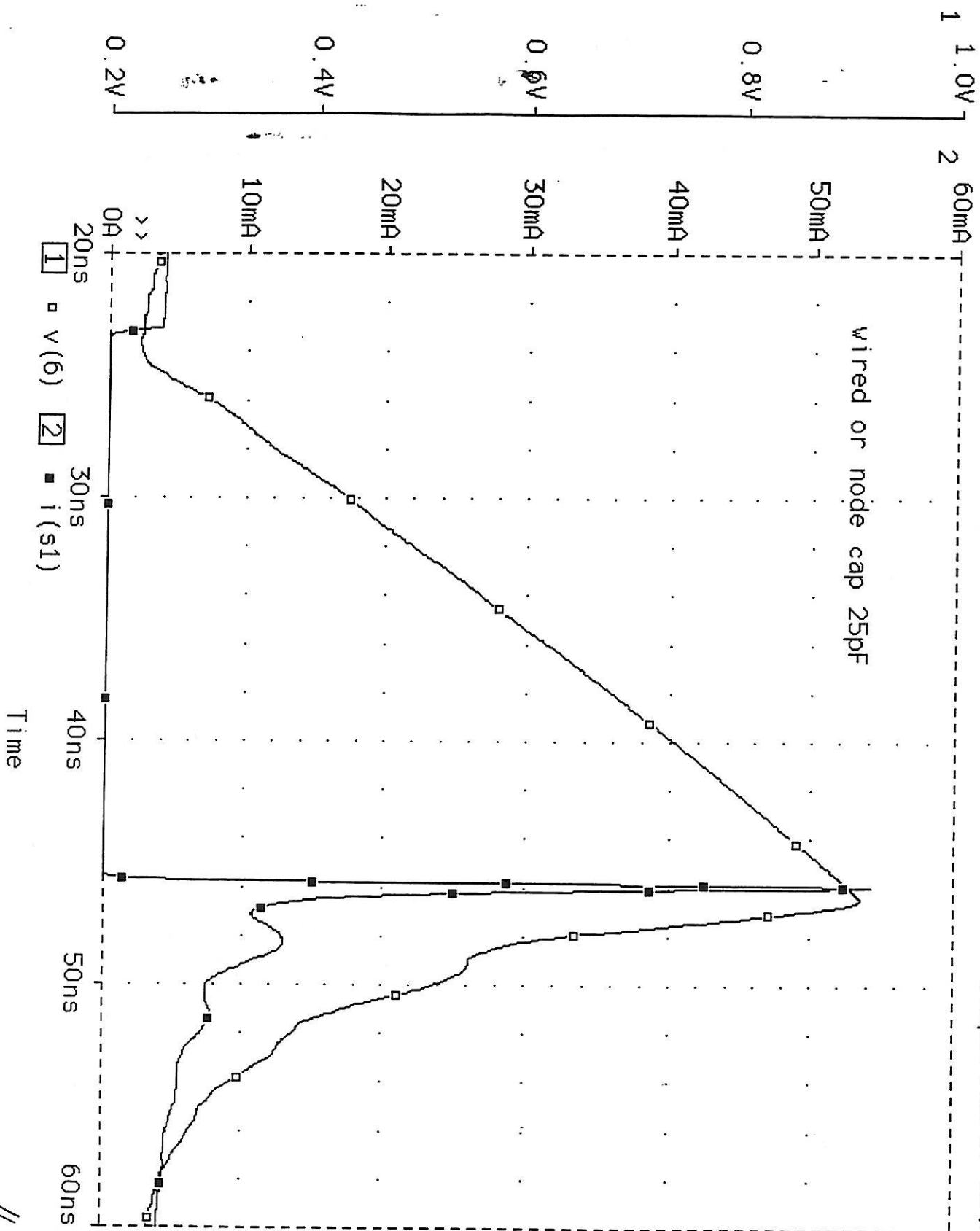
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Temperature: 27.0



Date/Time run: 10/13/93 ide physical interface circuit 08:44:56

Temperature: 27.0



Date/Time run: 10/13/93 ide physical interface circuit 08:41:50

Temperature: 27.0

