X3T9.2/93-114

To: scsi reflector
cc:
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Date: 06/28/93 03:54:05 PM
Subject: SPI clarification of REQ/ACK pulse width

I noted that new SCSI bus timing values were added for "Receive Assertion Period" and "Receive Negation Period" (in section 9). Furthermore, the definition of these values includes the voltage level at which the pulse width should be measured for single ended systems. This is all good stuff.

Unfortunately, these new values don't define how to measure the pulse width for differential signals. NOWHERE in this document is there any hint on how to measure pulse width for differential signals. How can we be so sure that someone won't have a different interpretation about how to measure differential pulse width? I am sure that the voltage levels were added for single ended because of just such a disagreement. A differential measurement rule should also be added.

The "Transmit assertion period" and "Transmit negation period" descriptions don't give any guidelines for either single ended or differential. This brings several possibilities to mind.
(a) Should I use the same levels that are defined for the receive assertion & negation periods?
(b) Should I use the 1.4 V "nominal switching threshold" level mentioned in section 7.1.3? This is what many people are doing with the SCSI-2 Standard, since this is the only level referred to that seems like a reasonable spot to measure pulse width.
(c) I have heard of chip vendors suggesting 1.0 V and other voltage levels for measuring the pulse width, none of which seem to have any basis in either SCSI-2 or SPI as a measurement level.

What should the transmit assertion & negation periods refer to as the right spot to measure pulse width? Let's add this to the SPI document to prevent future questions on this issue. Let's add both SE and Differential definitions. Let's do it before publishing the document!!