TO: **John Lohmeyer, Chairman, X3T9.2 Committee (SCSI)**

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IEEE P1285 Liaison to X3T9.2/DADI
Apple Computer

Date: **April 19, 1993**

Subject: **P1285 Liaison Report for April 1993**

Scope

IEEE P1285 is a standards group organized to define a new interface for "high-latency", non-volatile memory elements such as rotating media and solid state memory. The group is targeting configurations where storage elements are small enough to be attached directly to the motherboard. The goals are to provide support for scheduling of data transfers spanning large numbers of units and to represent the traditional secondary storage elements as an extension to the system's main memory (memory-mapped).

Issues of concurrency, latency, bandwidth, extensibility, scalability are being addressed. The increasing demand for deterministic data transfers by real-time applications is being examined. Support is to be provided for scheduling data transfers in a predetermined manner in order to support time dependent applications.

The major features of P1285 are identified below:

- o Control and data space is memory mapped using P1212
- o One controller, multiple slaves model
- o Byte addressable, true memory mapped disk architecture
- o Inherent spindle synchronization support
- o Isochronous support
- o Live insertion/removal
- o Motherboard direct attach
- o Scalability in performance and cost

IEEE P1285 Project Status

The current activity involves defining functional division between the memory unit (device) and the host/controller. Furthermore, the new functions at the unit level and at the controller/host adapter level are being discussed and defined.

The latest architecture defines a memory mapped buffer of an unspecified size which physically resides on the unit. The buffer is managed externally by the host/controller, to simplify internal unit management. The buffer is used to queue commands and to

transfer data between the host/controller and the device. This architecture is driven by IEEE P1212.

Two device level functions are being actively discussed: zero latency read (ZLR) and exclusive or (XOR) commands. A scheme favored by the group is an XOR engine that operates on two embedded segments of the device buffer. No consensus has been reached on the mechanism for ZLR.

The controller/host adapter level functions under discussion are array application oriented. They are:

- o Read Stripe - read striped data from the nexus (reconstruction disabled)
- o Read & Cache - same as Read Stripe but data is cached by the controller
- o Read Stripe & Reconstruct - Read Stripe and Reconstruct any bad block
- o Write Stripe - write striped data and reconstruct parity data

Although these are not necessarily new commands, the group wants to make sure such functions can be performed with ease through the interface.

In addition to these new functions, the group has identified more practical device level commands as follows:

- o Unit power on/off
- o Reset unit
- o Reset bus/all
- o Format unit
- o Remap unit (reallocation)
- o Read unit configuration (details TBD)
- o Read extended status (details TBD)

Details of the above commands/functions will be documented into a P1285 draft in the near future.

Upcoming Events

o P1285 tentative meeting dates and locations:

May 5/12/93 @Apple Computer, 1 Infinite Loop, Cupertino
May 5/18/93 Co-located meeting with X3T9 in Santa Fe, NM.
June 6/3/93 @Santa Clara University, Bannon Engineering Bld.
July 7/1/93 @Apple Computer, 1 Infinite Loop, Cupertino

These meetings are scheduled from 2:00-5:00 PM. However, the co-located meeting is scheduled for 5:00-8:00 PM. Please contact Martin Freeman at (415)354-0329 for exact date and location, or for additional information.