A NEW PERIPHERAL INTERFACE

RON ROBERTS
Ph. 408-432-3875
FAX 408-432-3773
email ron_roberts@maxtor.com
PERIPHERAL DEVICE INTERFACE

ANOTHER INTERFACE !!!

DESIGN GOALS

- LOW LEVEL ACCESS TO THE MEDIA... IF REQUIRED
- VARIABLE DATA TRANSFER RATES FOR PERFORMANCE VS COST TRADE-OFFS
- ALLOW VENDORS TO TAKE ADVANTAGE OF VOLUME PRODUCTION
- PROVIDE EASY IMPLEMENTATION OF ARRAYS OF DISKS
- PROVIDE SIMPLIFIED COMMAND STRUCTURES AND FLOW
- PROVIDE FOR MAXIMUM THROUGH-PUT
- PROVIDE FOR ERROR FREE TRANSFERS
PERIPHERAL DEVICE INTERFACE

ARCHITECTURAL MODEL

<table>
<thead>
<tr>
<th>System Attachment Level (SCSI, ATA, IPI3, VME, etc., etc.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peripheral Controller</td>
</tr>
<tr>
<td>Basic Device Level Attachment</td>
</tr>
<tr>
<td>Peripheral Device</td>
</tr>
</tbody>
</table>
# Peripheral Device Interface

## Architectural Model

### Attributes of Levels

<table>
<thead>
<tr>
<th>Peripheral Controller</th>
<th>Peripheral Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Interface Controls</td>
<td>All Servo Controls</td>
</tr>
<tr>
<td>Cache Memories (if required)</td>
<td>Encoder Decoder</td>
</tr>
<tr>
<td>Controls Multiple Devices (no limits)</td>
<td>Read/Write Circuits</td>
</tr>
<tr>
<td>Buffer Areas</td>
<td>Ecc on the Fly</td>
</tr>
<tr>
<td>System Specific Knowledge</td>
<td>Storage Media</td>
</tr>
<tr>
<td></td>
<td>Spindle Sync Ckts</td>
</tr>
<tr>
<td></td>
<td>Power Controls</td>
</tr>
</tbody>
</table>
PERIPHERAL DEVICE INTERFACE

INFORMATION MOVEMENT PROTOCOL

PERIPHERAL CONTROLLER

4 COMMAND WORDS TRANSMITTED

4 STATUS WORDS RCV'D

WAIT FOR INTERRUPT
(Do something else)

PERIPHERAL DEVICE

4 COMMAND WORDS RCV'D & DECODED

4 STATUS WORDS TRANSMITTED

PERFORM SPECIFIED COMMAND

TASK COMPLETED TRANSMIT 4 STATUS WORDS

MAXTOR CORPORATION
SYSTEM ENGINEERING
PERIPHERAL DEVICE INTERFACE

WHERE DOES IT FIT

IN THE HIERARCHY OF THE SUBSYSTEM ??

HOST SYSTEM

PERIPHERAL CONTROLLER

PERIPHERAL DEVICE

SCSI
ATA
etc

BASIC DEVICE INTF

TYPICAL PERIPHERAL SUB-SYSTEM

RKR 03/93

MAXTOR CORPORATION
SYSTEM ENGINEERING
PERIPHERAL DEVICE INTERFACE

INTERFACE LINES

DATA LINES 2, 4, 8, 16 + P/BYTE
SYNC LINES 2
CONTROL LINES 16 + 2P
MESSAGE LINES 6

PERIPHERAL CONTROLLER

PERIPHERAL DEVICE

MAXTOR CORPORATION
SYSTEM ENGINEERING
PERIPHERAL DEVICE INTERFACE

CONTROL SIGNALS

CONTROL SIGNALS ARE BI-DIRECTIONAL

TRANSPORTS COMMAND DATA TO THE PERIPHERAL DEVICE
TRANSPORTS RESPONSE/SENSE DATA TO THE PERIPHERAL CONTROLLER
## Peripheral Device Interface

### Command Block Format

<table>
<thead>
<tr>
<th>Command Block Word</th>
<th>Description</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Location Address</td>
<td>15</td>
</tr>
<tr>
<td>1</td>
<td>Control Information</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td>Location Address</td>
<td>15</td>
</tr>
<tr>
<td>2</td>
<td>Control Information</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td>Control Information</td>
<td>15</td>
</tr>
<tr>
<td>3</td>
<td>Control Information</td>
<td>15</td>
</tr>
</tbody>
</table>
PERIPHERAL DEVICE INTERFACE

MESSAGE SIGNALS

MESSAGE SIGNALS COMMUNICATE EXACT MESSAGES BETWEEN THE PERIPHERAL CONTROLLER AND THE PERIPHERAL DEVICE

PERIPHERAL CONTROLLER

ATTENTION

STATUS

COMMAND RECEIVED

DEVICE INTERRUPT

CONTROL VALID

DEVICE RESET

PERIPHERAL DEVICE

MAXTOR CORPORATION
SYSTEM ENGINEERING
## Peripheral Device Interface

### Message Signal Definitions

<table>
<thead>
<tr>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Attention</strong></td>
<td>Asserted by peripheral device to request service.</td>
</tr>
<tr>
<td><strong>Status</strong></td>
<td>When asserted by controller request status from the device, when negated it indicates transfer of control information.</td>
</tr>
<tr>
<td><strong>Command Received</strong></td>
<td>Asserted by device to indicate receipt of last word of control information. Remains asserted until completion of that command indicating device is in a busy state.</td>
</tr>
<tr>
<td><strong>Device Interrupt</strong></td>
<td>Asserted by the device to execution of a command or completion of any request.</td>
</tr>
<tr>
<td><strong>Device Reset</strong></td>
<td>Asserted by the controller to initialize the device.</td>
</tr>
<tr>
<td><strong>Control Valid</strong></td>
<td>Asserted by the controller to indicate information is valid on the control lines.</td>
</tr>
</tbody>
</table>
PERIPHERAL DEVICE INTERFACE

DATA SIGNALS

DATA SIGNALS ARE BI-DIRECTIONAL

DATA SIGNALS MAY CONSIST OF 2, 4, OR 8 PHYSICAL LINES
IF 4 OR 8 PHYSICAL LINES ARE USED A PARITY BIT MUST ALSO BE USED

NUMBER OF DATA SIGNALS DETERMINED BY SYSTEM PERFORMANCE REQUIREMENTS
PERIPHERAL DEVICE INTERFACE

DATA SIGNALS

BI-DIRECTIONAL SIGNALS
PARITY IS OPTIONAL FOR 2 BIT TRANSFER
MANDATORY ON 4 & 8 BIT TRANSFERS

MAXTOR CORPORATION
SYSTEM ENGINEERING

RKR 03/93
PERIPHERAL DEVICE INTERFACE

SYNC SIGNALS

SYNC SIGNALS ARE BI-DIRECTIONAL

SYNC SIGNALS ARE USED IN CONJUNCTION WITH TRANSFER OF DATA, COMMAND, AND STATUS BETWEEN THE PERIPHERAL CONTROLLER AND THE PERIPHERAL DEVICE
PERIPHERAL DEVICE INTERFACE

SYNCRONIZATION

VALID SYNC SEQUENCE

WHILE SYNC 0 IS ASSERTED, AND WHEN SYNC 1 IS ASSERTED, THE DURATION OF SYNC 1 BECOMES VALID SYNC TIME.

SYNC SIGNALS ARE SYNCRONIZED WITH THE CLOCK OF THE SENDING END OF THE INTERFACE.
PERIPHERAL DEVICE INTERFACE

TIMING CONSIDERATIONS

WORD 0
WORD 1
WORD 2
WORD 3
VALIDATE
STATUS 1
STATUS 2
STATUS 3

COMMAND OVERHEAD 1

MAXIMUM BUS XFER RATE

VARIES BY PRODUCT
(MAX = 150 uSEC)

PREDICTABLE AND CONSISTENT LATENCY

MAXTOR CORPORATION
SYSTEM ENGINEERING
# Peripheral Device Interface

## Timing Specifications

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Clock Frequency</td>
<td>50 MHz</td>
</tr>
<tr>
<td>Maximum Transfer Rates: (Non-Buffered)</td>
<td></td>
</tr>
<tr>
<td>2 Bit</td>
<td>12.5 MBytes/SEC</td>
</tr>
<tr>
<td>4 Bit</td>
<td>25.0 MBytes/SEC</td>
</tr>
<tr>
<td>8 Bit</td>
<td>50.0 MBytes/SEC</td>
</tr>
<tr>
<td>Maximum Command Transfer Time</td>
<td>320 nsec</td>
</tr>
<tr>
<td>Maximum Command Validation Time</td>
<td>150 usec</td>
</tr>
<tr>
<td>Maximum Status Transfer Time</td>
<td>320 nsec</td>
</tr>
</tbody>
</table>

**Note:**
Timing based on a maximum media transfer rate of 100MHz
PERIPHERAL DEVICE INTERFACE

CONFIGURATION POSSIBILITIES

SCSI, ATA(IDE), IPI2, 1394, FC(X),

PERIPHERAL CONTROLLER

BASE-1

DEVICE

BASE-1

DEVICE

BASE-1

DEVICE

BASE-1

DEVICE

RADIAL CONNECTION
PERIPHERAL DEVICE INTERFACE

ADVANTAGES OF INTERCONNECTION SCHEME

- PROVIDES LOW LEVEL ACCESS TO MEDIA (if required)
- SIMPLIFIES PERIPHERAL DEVICE Firmware
- LESS COSTLY PERIPHERAL DEVICES
- EASE OF IMPLEMENTATION FOR ARRAYS OF DISKS (RAID's ??)
- PERIPHERAL GUIDED VS SYSTEM AFTER THOUGHT
- PERFORMANCE ORIENTED WITH LESS $ THAN SCSI (PER SYSTEM)