**To:** X3T9.2 Committee Membership

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**Subject:** SBP Command Block CDB Alignment

SBP command blocks have been laid out with the intent of aligning all data items on natural boundaries. That is, assuming the base of the command block is on an 64-byte boundary, all n-byte quantities are aligned on n-byte boundaries. In particular, the 16-byte CDB field is 16-byte aligned within the SBP command block.

Unfortunately, this does not achieve the desired end, since common CDB fields are not aligned relative to the start of the CDB. The CDB may be aligned, but fields within it are not. For example, the following illustrates a 12-byte CDB embedded within an SBP command block. The CDB is shown in bold. Note that the Logical Block Address and Transfer Length fields are miss aligned.

| Byte | 0 | 1 | 2 | 3 |
|---|---|---|---|---|
| 0 | Next Command Address (MSQ) | | | |
| 4 | Next Command Address (LSQ) | | | |
| 8 | Reserved | | LUN | |
| 12 | Codes | | Flags | |
| **16** | **Operation Code** | **Reserved** | **Logical Block Address (high)** | |
| **20** | **Logical Block Address (low)** | | **Transfer Length (high)** | |
| **24** | **Transfer Length (low)** | | **Reserved** | **Control** |
| **28** | **unused** | | | |
| 32 | Transfer Length | | | |
| 36 | Control | | Reserved | Sense Length |
| 40 | Data Buffer Address (MSQ) | | | |
| 44 | Data Buffer Address (LSQ) | | | |
| 48 | Status FIFO Address (MSQ) | | | |
| 52 | Status FIFO Address (LSQ) | | | |
| 56 | Sense Buffer Address (MSQ) | | | |
| 60 | Sense Buffer Address (LSQ) | | | |

Correcting this requires skewing the CDB by two bytes, so that it will apparently be miss aligned. The proper correction is to move the Reserved and Sense Length bytes before the CDB and the Control doublet before the Transfer Length quadlet.. This places all control information at the beginning of the command block, and all data transfer control information adjacent. Note that the Control doublet contains (or will contain) data transfer control information. This transforms the previous example to the following.

| Byte | 0 | 1 | 2 | 3 |
|---|---|---|---|---|
| 0 | Next Command Address (MSQ) | | | |
| 4 | Next Command Address (LSQ) | | | |
| 8 | Reserved | | LUN | |
| 12 | Codes | | Flags | |
| 16 | Reserved | Sense Length | **Operation Code** | **Reserved** |
| 20 | **Logical Block Address** | | | |
| 24 | **Transfer Length** | | | |
| 28 | **Reserved** | **Control** | **unused** | |
| 32 | **unused** | | (Data Transfer) Control | |
| 36 | Transfer Length | | | |
| 40 | Data Buffer Address (MSQ) | | | |
| 44 | Data Buffer Address (LSQ) | | | |
| 48 | Status FIFO Address (MSQ) | | | |
| 52 | Status FIFO Address (LSQ) | | | |
| 56 | Sense Buffer Address (MSQ) | | | |
| 60 | Sense Buffer Address (LSQ) | | | |

The alignment for a 10-byte CDB is:

| Byte | 0 | 1 | 2 | 3 |
|---|---|---|---|---|
| 0 | Next Command Address (MSQ) | | | |
| 4 | Next Command Address (LSQ) | | | |
| 8 | Reserved | | LUN | |
| 12 | Codes | | Flags | |
| 16 | Reserved | Sense Length | **Operation Code** | **Reserved** |
| 20 | **Logical Block Address** | | | |
| 24 | **Reserved** | **Transfer Length** | | **Control** |
| 28 | **unused** | | | |
| 32 | | | (Data Transfer) Control | |
| 36 | Transfer Length | | | |
| 40 | Data Buffer Address (MSQ) | | | |
| 44 | Data Buffer Address (LSQ) | | | |
| 48 | Status FIFO Address (MSQ) | | | |
| 52 | Status FIFO Address (LSQ) | | | |
| 56 | Sense Buffer Address (MSQ) | | | |
| 60 | Sense Buffer Address (LSQ) | | | |

While not perfect, this is the best that can be achieved while retaining compatibility with SCSI-2.