X3T9.2/93-7

Quantum

EXTERNAL MEMO

X3T9.2/93-7

DATE: January 11, 1993

TO: John Lohmeyer

CC: X3T9.2 Membership

FROM: Jim McGrath
Quantum Corporation
phone: 408-894-4504
fax: 408-894-3208

SUBJ.: Support of Local Bus in ATA

I suggest we standardize the support for a local bus implementation of the ATA interface. Several de facto implementations are currently under development, and the industry would best be served by common agreement on the following items:

- **Timing**: Obviously cycle times and low level timings must be addressed. 120 ns cycle times is one obvious requirement, although other timings may be desirable.
- **Driver/Cable/Termination**: Going reliably faster (remember there is no parity) may require some of the solutions already developed for Fast Single-Ended SCSI.
- **Pacing**: Disk controllers using DRAM must have the capability to dynamically insert wait states on the local bus when their interface chip FIFOs become empty. Standardizing the timings associated with I/O Channel Ready is one solution.
- **Firmware**: Identify Drive should be updated to allow the drive to inform the host of its capabilities. I do not think a new Set Features value will be required.

And anything else people desire. This activity can be done in ATA-2 and/or SFF. I also suggest ad hoc meetings in between our normal meetings both to allow for faster development of a proposal and the attendance of people who would not normally attend a plenary or working group (e.g. ASIC designers). Overall I envision this activity being modeled after the Fast DMA work of last year.