TO: John Lohmeyer, Chairman, X3T9.2 Committee (SCSI)

From: Dennis Pak
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           Apple Computer

Date: December 7, 1992

Subject: P1285 Status Report for December '92

Scope

IEEE P1285 is a standards group organized to define a new interface for "high-latency", non-volatile memory elements such as rotating media and solid state memory.   The group is targeting configurations where storage elements are small enough to be attached directly to the motherboard. The goals are to provide support for scheduling of data transfers spanning large numbers of units and to represent the traditional secondary storage elements as an extension to the system's main memory (memory-mapped).

Issues of concurrency, latency, bandwidth, extensibility, scalability are being addressed. The increasing demand for deterministic data transfers by real-time applications is being examined. Support is to be provided for scheduling data transfers in a predetermined manner in order to support time dependent applications.

The major features of P1285 are identified below:
- Control and data space is memory mapped using P1212
- One controller, multiple slaves model
- Byte addressable, true memory mapped disk architecture
- Inherent spindle synchronization support
- Isochronous support
- Live insertion/removal
- Motherboard direct attach
- Scalability in performance and cost

IEEE P1285 Project Status

In the last two meetings, issues on the lower level, alpha, interface, lead by Chris Hamlin, have been discussed actively. The development focus is on latency characterization and real-time scheduling of multi-threaded events. Chris has promised a document outlining the scope, features, and the definition of the interface in the near future in order to set the overall direction for the alpha

development.

One of the primary candidates for the beta level interface is 'RAMLink' which is a single-master/multiple-slaves interface at 500 MBytes/s. The latest focus is how to provide hints to the device to maximize its cache usage (dynamic decision on read ahead or most recently used).

An overview of the two interface levels, alpha and beta, was given at the co-located meeting in Sunnyvale, CA. Martin Freeman, in place of Chris Hamlin, presented the alpha level; Dave James gave an overview of the RAMLink interface.

One key component in the alpha level is the characterization of mechanical latencies which was again identified during the co-located meeting. P1285 has been concentrating on this issue as well as the alpha protocol/interface definition.

The strategic development plan for either the alpha or beta level was not a topic of discussion at the meeting. Further discussion on this matter is expected at the January Grass Roots meeting.

The P1285 reflector is up and running. The monthly meeting minutes and announcements are posted on the reflector. People who want to receive information from the reflector should contact Dennis Pak at 'dennis.pak @applelink.apple.com'.

Upcoming Events

• The third grass roots meeting proposed for January 14, 1993, 9:00 AM - 11:00 AM at Santa Clara University, Santa Clara, CA.

• P1285 meeting dates and locations:

December	12/11/92	@Santa Clara University, Santa Clara, CA.
January	1/7/93	@Apple Computer (location TBD)
February	2/4/93	@Santa Clara University, Santa Clara, CA.
March	3/4/93	@Apple Computer (location TBD)

These meetings are from 2:00-5:00 PM

Open Issues

• Forward the minutes of the second grass roots meeting (Larry Lamers).

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