X3T9.2/92-217-Rev 0

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Subject: SCSI Caching Large Segment Control

Concern was raised at the October 1992 X3T9.2 plenary meeting relative to the SCSI-3 Caching Page's capability to handle large cache segment sizes. The present definition uses a two byte field which allows the setting or reporting of up to 64 kilo byte segments. Larger segments would only be manageable by the number of segments field rather than the size field.

Because of this issue the question of whether or not the segment size documentation of the Caching Page should have been in logical blocks rather than bytes was raised. The consensus of the plenary was that it was academic whether or not the documentation was in error. It had been accepted as documented, implementations have already been made, and it is too late to change from bytes to logical blocks.

Upon reflection the November working group readdressed this issue. They realized there was an alternative that would allow enjoying the cake without consuming it. Consequently the working group recommended the following change to the SCSI-3 Caching Page.

The following descriptions include only the new SCSI-3 items. The proposed change is shown underlined.

Logical Block Cache Segment Size Proposal

Caching Page:

Caching Page

Bit / Byte	7	6	5	4	3	2	1	0
0	PS	Reserved	Page Code (08h)					
1	Page Length (12h)							
2	**IC**	**ABPF**	**CAP**	**DISC**	**SIZE**	WCE	MF	RCD
3	Demand Read Retention Priority				Write Retention Priority			
4	(MSB)							
5	Disable Pre-fetch Transfer Length							(LSB)
6	(MSB)							
7	Minimum Pre-fetch							(LSB)
8	(MSB)							
9	Maximum Pre-fetch							(LSB)
10	(MSB)							
11	Maximum Pre-fetch Ceiling							(LSB)
12	**FSW**	**LBCSS**	**DRA**	RESERVED				
13	**NUMBER OF CACHE SEGMENTS**							
14	(MSB)							
15	**Cache Segment Size**							(LSB)
16	RESERVED							
17	(MSB)							
18	**NON CACHE SEGMENT SIZE**							
19								(LSB)

The Initiator Control (IC) enable bit (Bit 7 Byte 2), when set to one, requests that the SCSI device use the Number of Cache Segments or Cache Segment Size fields, dependent upon the Size bit, to control the caching algorithm rather than the target's own adaptive algorithm.

The Abort Pre-Fetch (ABPF) bit (Bit 6 Byte 2), when set to one, with the DRA bit equal to zero, requests that the SCSI device abort the pre-fetch upon selection. The ABPF set to one takes precedence over the Minimum Pre-fetch bytes. When set to zero, with the DRA bit equal to zero, the termination of any active pre-fetch is dependent upon Caching Page bytes 4 through 11 and is operation and/or vendor specific.

The Caching Analysis Permitted (CAP) bit (Bit 5 Byte 2), when set to one, requests that the SCSI device perform caching analysis during subsequent operations. When set to zero, CAP requests that caching analysis be disabled to reduce overhead time or to prevent non pertinent operations from impacting tuning values.

The Discontinuity (DISC) bit (Bit 4 Byte 2), when set to one, requests that the SCSI device continue the pre-fetch across time discontinuities, such as across cylinders (or tracks in an embedded servo drive), up to the limits of the buffer, or segment, space available for pre-fetch. When set to zero, the DISC requests that pre-fetches be truncated (or wrapped) at time discontinuities.

The Size Enable (SIZE) bit (Bit 3 Byte 2), when set to one, indicates that the Cache Segment Size is to be used to control caching segmentation. When SIZE equals zero, the Initiator requests that the Number of Cache Segments is to be used to control caching segmentation. Simultaneous use of both number of segments and segment size is vendor specific.

The Force Sequential Write (FSW) bit (Bit 7 Byte 12). when set to one, indicates that multiple block writes are to be transferred over the SCSI bus and written to the media in an ascending, sequential, logical block order. When the FSW bit equals zero, the target is allowed to reorder the sequence of writing addressed logical blocks in order to achieve a faster command completion.

The Logical Block Cache Segment Size (LBCSS) bit when set to one, indicates that the Cache Segment Size field units shall be interpreted as logical blocks. When the LBCSS bit equals zero the Cache Segment Size field units shall be interpreted as bytes. The LBCSS shall not impact the units of other fields.

The Disable Read-Ahead (DRA) bit (Bit 5 Byte 12), when set to one, requests that the target not read into the buffer any logical blocks beyond the addressed logical block(s). When the DRA bit equals zero, the target may continue to read logical blocks into the buffer beyond the addressed logical block(s).

The Number of Cache Segments (Byte 13) advises the target how many segments the host requests that the cache be divided into.

The Cache Segment Size field (Bytes 14 and 15) indicates the requested segment size in Bytes. This standard assumes that the Cache Segment Size field is valid only when the SIZE bit is one.
If the Non Cache Buffer Size field (Bytes 17-19) is greater than zero, this field advises the target how many bytes the initiator requests that the target allocate for a buffer function when all other cache segments are occupied by data to be retained. If the number is at least one, caching functions in the other segments need not be impacted by cache misses to perform the SCSI buffer function. The impact of the Non Cache Buffer Size equal 0 or the sum of this field plus the Cache Segment Size greater than the buffer size is vendor specific.

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