TO: John Lohmeyer, Chairman, X3T9.2 Committee (SCSI)

From: Dennis Pak
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Apple Computer

Date: October 12, 1992

Subject: P1285 Status Report for October '92

Scope

IEEE P1285 is a standards group organized to define a new interface for "high-latency", non-volatile memory elements such as rotating media and solid state memory. The group is targeting configurations where storage elements are small enough to be attached directly to the motherboard. The goals are to provide support for scheduling of data transfers spanning large numbers of units and to represent the traditional secondary storage elements as an extension to the system's main memory (memory-mapped).

Issues of concurrency, latency, bandwidth, extensibility, scalability are being addressed. The increasing demand for deterministic data transfers by realtime applications is being examined. Support is to be provided for scheduling data transfers in a predetermined manner in order to support time dependent applications.

The major features of P1285 are identified below:

- Control and data space is memory mapped using P1212
- One controller, multiple slaves model
- Byte addressable, true memory mapped disk architecture
- Inherent spindle synchronization support
- Isochronous support
- Live insertion/removal
- Motherboard direct attach
- Scalability in performance and cost

Update on the Second Grass Roots Meeting

The second grass roots meeting was held on Thursday, October 1, 1992 at Quantum in Milpitas, CA, hosted by Jim McGrath. Participants were Martin Freeman, Jim McGrath, Chris Hamlin, David James, Larry Lamers, and Dennis Pak. Some of the highlights of the meeting were (Please refer to the meeting minutes for detail):

- X3T9 decided to establish a liaison with P1285.

- A liaison relationship to SFF was recommended.
- The future role of grass roots was discussed.
- Updates on PCMCIA, DADI, P1394, RAMLink, and P1285 projects were given.

The P1285 group is exploring a concept of an abstract "low-level" interface. The interface would be designed for scaling real-time behavior (motion and time). The goal would be to design an interface which would provide direct control of a particular memory unit and yet abstract enough to use on a number of different memory unit types.

The concept will be presented during the November X3T9 Working Group week. The presentation is currently scheduled for Thursday, Nov. 12, '92, from 9 AM to 11 AM at the Sheraton Hotel (room TBD). The objective and the value of the intended work will be discussed. Coordination issues will be deferred to a later meeting.

IEEE P1285 Project Status

Two levels of interface are being investigated; alpha and beta. The emphasis on the alpha(low) level is on time, motion, and cost (especially in aggregated arrays), while the emphasis of the beta (intelligent, memory mapped) level is on ease of use and performance.

The P1285 reflector is up and running. The October meeting minutes will be posted to the reflector within the next few days. People who want to receive information from the reflector should contact Dennis Pak at 'dennis.pak@applelink.apple.com'.

Upcoming Events

- A co-located meeting on Nov. 12, '92 in Sunnyvale, CA.
- A P1285 working group's meeting on Dec. 11, '92 at Santa Clara University, Santa Clara, CA.
- The next grass roots meeting during the week of Jan. 25, '93.

Open Issues

- Appointment of X3T9.2/DADI liaison to P1285.
  My official responsibilities include attending DADI meetings and reporting any relevant issues back to P1285. The responsibility of reporting P1285 activities to X3T9.2 belongs to the X3T9.2 liaison. I'll continue to provide this report for now, however, I would like to formally request an X3T9(.2) liaison appointment as soon as possible.