To: ATA Committee

From: Mehran Ramezani
Emulex Corporation
(714)668 5331 Tel
(714)668 6654 Fax

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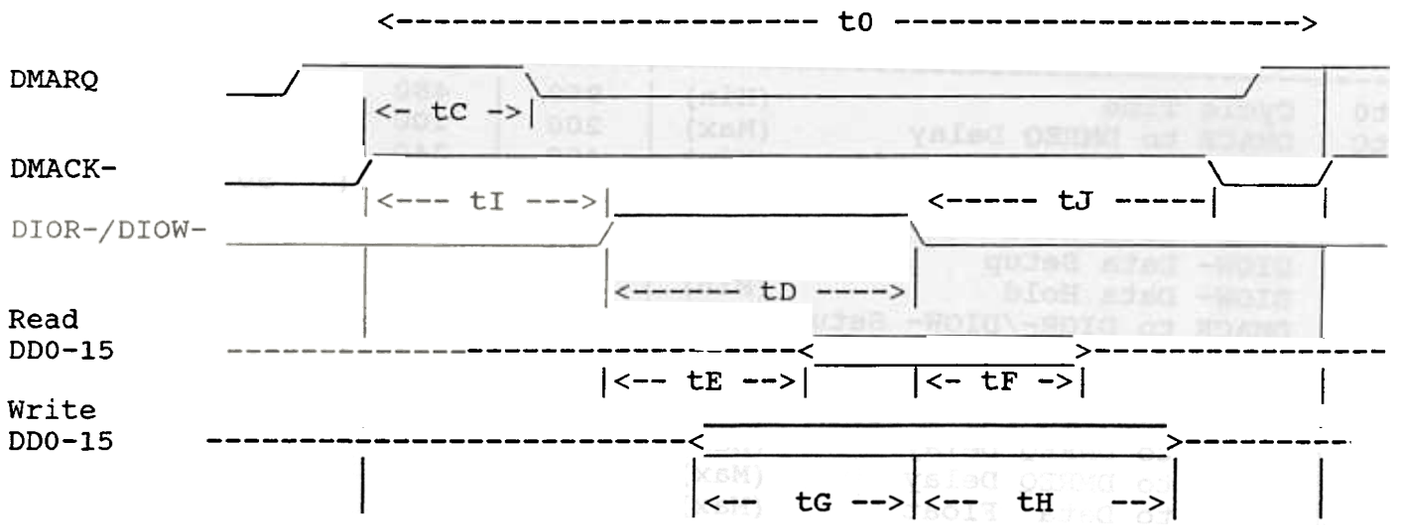
Subject: DMA Timing Changes in ATA Document

I would like to propose the following changes to the "AT Attachment Interface Document, Figure 11-3: DMA DATA TRANSFER":

A) The definition for "tE" is changed from "Data Setup (Min)" to "Data Access (Max)".

B) The modes 0, 1 and 2 are defined for single transfer DMA cycles. If these modes are to be preserved, there would be a need to create a fourth mode (Mode 3), to accommodate the timing requirements of EISA DMA Type "B", Demand Mode.

Note: It may be possible, by modifying some of the timing parameters of either mode 1 or mode 2, to accommodate the needs of EISA Type "B" DMA. And then create a new feature in SET FEATURES Command, to handle Multiple Transfers (Demand Mode) vs. Single transfer DMA.


<-------------------- t0 -------------------->
DMARQ
<- tC ->
DMACK-
<--- tI --->
<----- tJ -----
DIOR-/DIOW-
<------ tD ---->
Read
DD0-15
<
>
<-- tE -->
<- tF ->
Write
DD0-15
<
>
<-- tG -->
<-- tH -->

B) Multiple Transfers DMA Cycle Mode 3

	DMA Timing Parameters		Mode 0 nsec	Mode 1 nsec	Mode 2 nsec	Mode 3 nsec
t0	Cycle Time	(Min)	960	480	240	480
tC	DMACK to DMREQ Delay	(Max)	200	100	80	---
tD	DIOR-/DIOW- 16-bit	(Min)	480	240	120	215
tE	DIOR- Data Access	(Max)	250	150	50	150
tF	DIOR- Data Hold	(Min)	5	5	5	5
tG	DIOW- Data Setup	(Min)	250	100	35	100
tH	DIOW- Data Hold	(Min)	50	30	20	20
tI	DMACK to DIOR-/DIOW- Setup	(Min)	0	0	0	0
tJ	DIOR-/DIOW- to DMACK Hold	(Min)	0	0	0	0
tKr	DIOR- Negated Pulse Width	(Min)	---	---	---	50
tKw	DIOW- Negated Pulse Width	(Min)	---	---	---	215
tLr	DIOR- to DMREQ Delay	(Max)	---	---	---	120
tLw	DIOW- to DMREQ Delay	(Max)	---	---	---	40
tM	DIOR- to Data Float	(Max)	-	-	-	20

FIGURE 11-3: DMA DATA TRANSFER