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TO: Membership of X3T9.2

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SUBJECT: Selection Mechanism for Demand-type DMA in the 3.0 ATA Prop.

One of the public review comments on the 3.0 ATA Proposal is the addition of Demand Mode DMA transfers (similar to EISA type 'B'). The ATA proposal must also contain a mechanism for the device to indicate if it supports this feature as well as a mechanism to support this feature. This mechanism should be fully backward compatible and provide expansion capability for future DMA enhancements (different protocols, such as EISA type 'C' as well as timing improvements).

Currently, the Identify Drive Information data structure has two words to describe the DMA data transfer capabilities. Bit 8 of Word 49 is used to indicate if DMA data transfers are supported at all. Bits 15-8 of Word 52 are used to describe which DMA data transfer cycle timing modes are supported. There are currently three valid entries for this field, which correspond to the three defined DMA data transfer cycle timing modes. These are: 0 (960 ns cycle), 1 (480 ns cycle) and 2 (240 ns cycle). It is assumed that if any mode other than 0 is supported, then all slower cycles are also supported. There is no support for the Demand-type protocol in the current ATA document.

The first problem is identifying to the system that Demand-type DMA transfers are supported by the device. The currently proposed Demand-type DMA timing cycle uses a different protocol than the existing modes and has a 480 ns. cycle definition. The simple solution of defining this new Demand-type cycle as mode 3 would break the existing compatibility assumptions as supporting the new Demand-type DMA does not imply that all three single-transfer DMA timing modes are supported. The simple solution of replacing either of the existing single-transfer modes with the new Demand-type timing and protocol would not be backward compatible.

We would like to propose that two new words be specified in the Identify Drive Information data structure, one to identify both the supported and current Single-Transfer type DMA timing cycles, and one to identify the supported and current Demand-type DMA timing cycles.

Word 60 would describe the Single Transfer DMA modes. The lower eight bits indicate which modes are supported, with each bit mapped to the corresponding mode, i.e., bit 0 active indicates Single Transfer DMA type 0 is supported. The upper eight bits indicate the current mode, with each bit mapped to the corresponding mode, i.e., bit 8 active indicates Single Transfer DMA type 0 is currently selected. If Demand-type is currently enabled, or if DMA is not currently enabled, this field should contain zero.

Word 61 would describe the Demand Type DMA modes. The lower eight bits indicate which modes are supported, with each bit mapped to the corresponding mode, i.e., bit 0 active indicates Demand Type DMA mode 0 is supported. The upper eight bits indicate the current mode, with each bit mapped to the corresponding mode, i.e., bit 8 active indicates Demand Type DMA mode 0 is currently selected. If Single Transfer is currently enabled, or if DMA is not currently enabled, this field should contain zero.

Table 1. Proposed Valid Entries for Words 60 and 61

Bits	Word 60 - Single Transfer DMA
15:8	Bit position encoded current single transfer DMA Mode
7:3	Reserved
2	Single transfer DMA Mode 2 supported (240 ns cycle)
	Single transfer DMA Mode 1 supported (480 ns cycle)
0	Single transfer DMA Mode 0 supported (960 ns cycle)
Bits	Word 61 - Demand Type DMA
15:8	Bit position encoded current single transfer DMA Mode
7:1	Reserved
0	Demand Type DMA Mode 0 supported (480 ns cycle)

The second part of the problem is selecting which DMA mode is requested by a DMA Transfer command. We propose to add two new commands to the Set Features command.:

O3h Enable Demand-type DMA with type from Sector Count value\*

83h Disable Demand-type DMA\*

\* These commands are Vendor-specified

These allow commands allow for future enhancement of the Demand-type DMA protocol. The default value (83h) is backwards compatible.