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Technical Communication

TO: ANSI X3T9.2 Committee SPI Work Group

DATE: Tak Asami

RE: Pin Capacitance of a SCSI Controller LSI

cc: 4-27-92

In the recent SPI Work Group meetings, importance of the node capacitance specification was brought up. This capacitance plays a major role on reflection problem and hot-plugging issue. Majority of the capacitance is from the LSI controller, yet such information is not readily available. This memo is written to supply information to help further analysis on the matter, to help develop the proper specification.

We do not test each device shipped for the pin capacitance, nor do we know anyone who does, with a possible exception of DRAM manufacturers. This is primarily due to (a) magnitude of the pin capacitance is far smaller than the tester capacitance, making the calibration difficult, and (b) such test is time consuming and drive up the test cost prohibitively high. However, we can estimate fairly accurately how much capacitance to expect by extracting the layout database information. The numbers presented here are derived using this method, and are not guaranteed by Western Digital. However, if a given silicon is processed within the specified tolerance (I presume it will not pass the production test were it not the case), then it is reasonable to expect a pin capacitance within the presented value.

The table below is the estimated Cin values for WD33C93B device. The are sorted by different class of drivers.

Table 1: WD33C93B Cin (PLCC44)

Driver Class	Cin
Active Negation Driver (60mA)	17.8pF
Active Negation Driver (48mA)	15.2pF
Open Drain Driver	12.6pF
Host Side Pins	5.18pF

Each pins, except Host Side Pins, are also attached to a hysteresis receiver. The package contribution to Cin is 1.2pF for PLCC-44 package.

From these figures, it is reasonable to assume a pin capacitance of 20pF when estimating the node capacitance. It also suggests the difficulty of specifying a node capacitance limit much less than 25pF.