MEMORANDUM -- 27 Apr 1992

TO: John Lohmeyer, Chairman, X3T9.2

FROM: Bill Spence

SUBJECT: SCSI Implementation in a 3.3 v Environment

The question has several times been raised: What would be the problems in implementing SCSI in a device (e.g., a notebook computer) powered by 3.3 volts. Herewith some thoughts. The purpose of raising this question is to anticipate any way that it might impact the SPI standard.

Two cases are here analyzed, both single-ended:
- Operation on a conventional SCSI bus, presumably on a temporary basis so that files can be exchanged with a conventional system.
- Quasi-SCSI operation with power-saving considerations

CONVENTIONAL

It appears to be very simple to operate a 3.3 volt device on a conventional SCSI bus, but there may be a gotcha to watch for:
- Active negation drivers in the exterior equipment. The low current sourcing capability planned for active-negation drivers limits their destructive capability. But if the terminator was missing at the 3.3 v device end of the bus, a negation signal from an active-negation driver could cause a momentary reflection voltage of some 5 volts or more. 3.3 v receivers might need protection.

Receiver input characteristics could be just as presently specified in the standard. Driver assertion capabilities would need to be the same also. And the fact that signal assertion on conventional buses produces momentary currents of up to 80 or 90 ma in some cases must be respected.

If the internal terminator is powered from the TERMPWR line--itself powered by some conventional external device--then the internal terminator can be any conventional type. Since all terminator types announced to date can operate with each other, no special problems are foreseen.

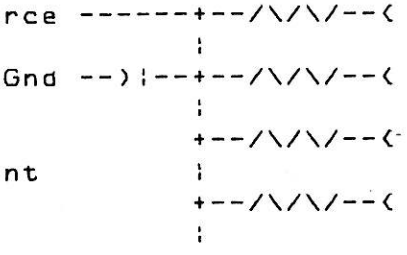
REDUCED POWER

This may be an unrealistic area of analysis. (I am not privy to any reason to introduce a SCSI bus into a low power device.) But to cover the matter, a quasi-SCSI operation at considerably lower power is certainly possible. Some considerations:

- Power voltage. It is presumed that the voltage of the battery-supplied power will vary over the range from 3.6 to 2.7 volts.

- Cable impedance. Considering the short distances and low node capacitances to be expected, it is likely that the highest practical impedance cables should be employed. Assuming that they must be 0.025-in pitch ribbon cables, they should have AWG 30 or even finer conductors and the dielectric should be of the foamed-Teflon class. Such cables probably could achieve about 100 ohms s/e impedance. If all busing is on boards, it may not be critical but again should strive for higher impedance.

- Terminator. A quite simple terminator probably would suffice. If a regulator could be developed to hold something approaching 2.5 v on the terminator internal node, it would be an improvement and would save power. See below.



- Operating modes.
  Two modes are possible, depending on special chip development. In standard mode, it still would be required that negated signals be 2.0 v or more. Theoretically, to achieve 2.0 v with 100 ohm cables, at least 18 ma min terminator current is required, leading to terminator resistors of 137 ohms. (It is assumed that the asserted signal is 0.2 v.) In restricted voltage mode, special receivers would require no higher than, say, 1.6 v in a negated signal. Then the terminator resistors could be 174 ohms.

  In actuality, depending on how small the system is, it is likely that far higher terminator resistance would provide acceptable operation. "First step" achievement of the required negation voltage level would not be necessary.

PROVISIONS IN THE STANDARD

Receivers which recognize negation at 1.6 v meet all the requirements of the present Standard. The reverse is not true; components which would operate in the reduced-power modes set forth above would require more restrictive specifications than presently in the Standard.