X3T9.2/92-38

Proposal for a Glitch Immunity Specification

This document attempts to define a worst case envelope for the waveforms that are likely to be encountered on the signal lines of an average SCSI physical channel immediately following assertion and deassertion.

These signal distortions (usually referred to as "glitches") are caused by the impedance imbalance of the physical channel and are the main cause of corrupted data transfers. As the elimination of glitches is practically an impossible task the next best thing is to make the signal receivers immune to their occurrence. Towards this goal it is important to define a set of reference cases to design against.

The following proposal is the result of theoretical analysis as well as experimental measurements of a large number of single ended SCSI devices available on the market. It includes both the waveforms generated by standard open drain drivers as well as the waveforms produced by the new active deassertion drivers.

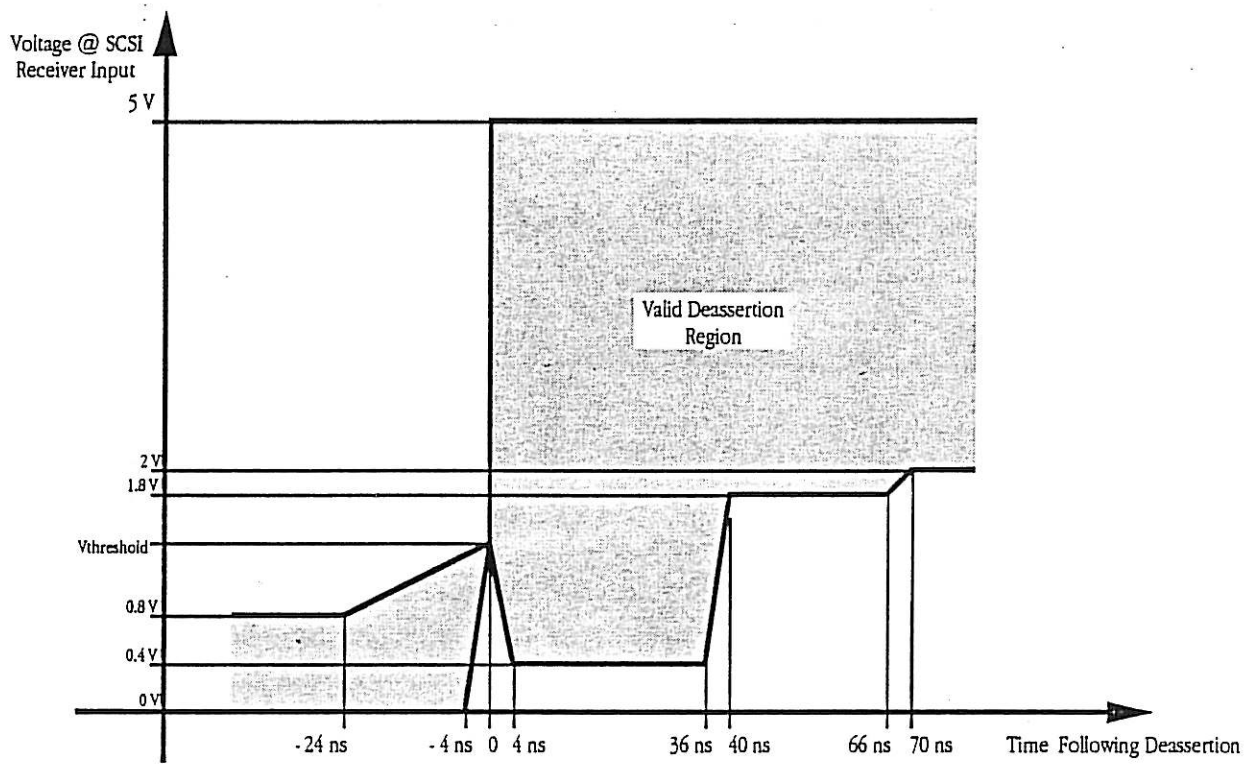

Figure 1: Worst Case Signal Envelope Following Deassertion.

This proposal is limited to single ended SCSI systems with a total cable length of no more than 6 meters. It considers cables with single ended impedance between 65 Ω and 120 Ω, drivers generating signals with a transition time of not less than 4 ns (10% to 90%) and devices with a total node load capacitance values of less than 50 pF.

Figure 1, page 2 describes the proposed worst case signal envelope immediately following deassertion while Figure 2, page 2 presents the proposed worst case signal envelope immediately following assertion.

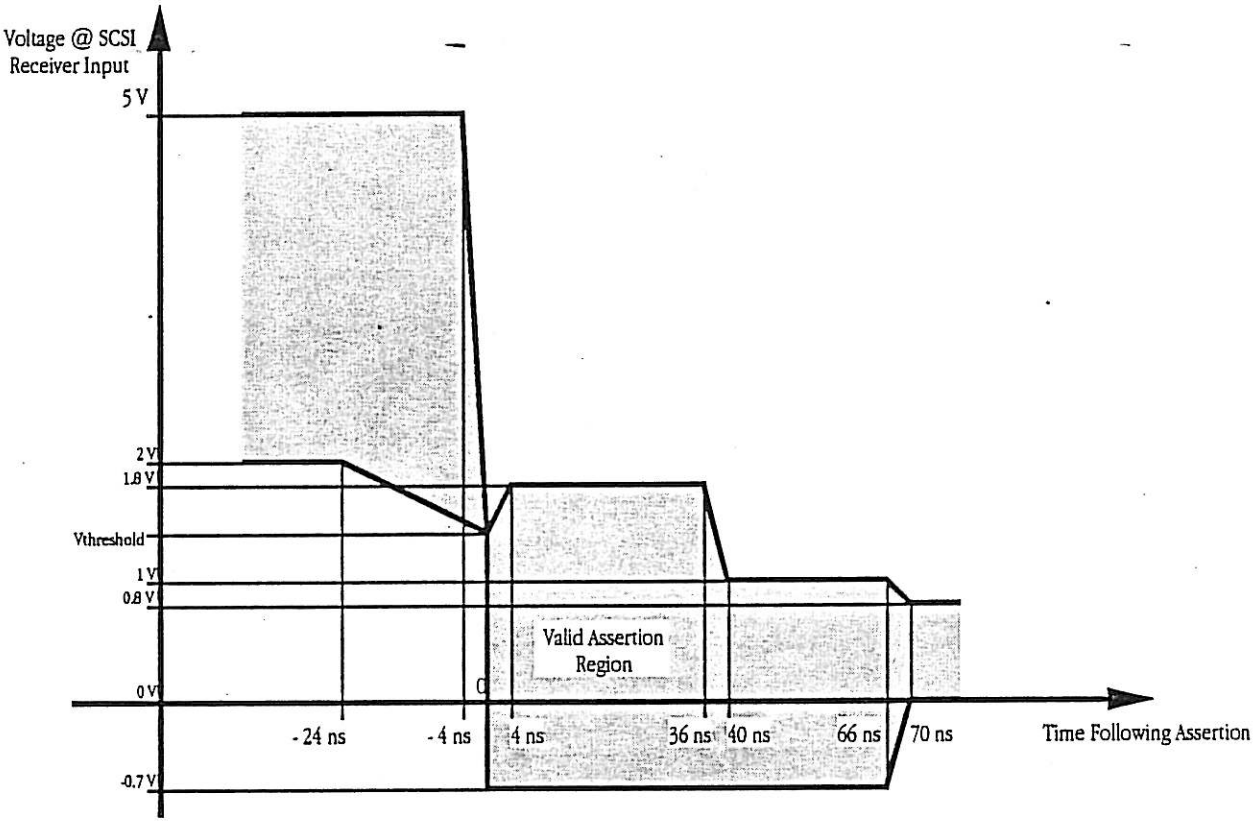

Figure 2: Worst Case Signal Envelope Following Assertion.

Following this specification will result into a clear overdesign of the signal receivers used on a physical channel implemented according to the latest committee proposals for cable impedance, node capacitance and signal transition times. Unfortunately such implementations represent at this time a very small minority of the installed base. On the other hand the proposal contains a relatively optimistic estimate of the physical channel behavior considering some of the SCSI implementations available on the market today. The glitch timing considered in this proposal is clearly outside the acceptable boundaries for SCSI 3 operation and imposes a performance penalty on all

fast SCSI implementations. Under these circumstances it may be useful to implement the receiver glitch immunity circuit as a user/software selectable option. Thus for very high quality physical channels this option can be disabled enabling maximum transfer rates while poor physical layer implementations will still work with an unavoidable performance penalty.

The second problem that this proposal creates is the added cost associated with the additional circuitry required. This can be minimized by implementing the glitch "eater" circuits on the /REQ and /ACK line receivers only.