To: X3T9.2 - SPI February 16, 1992

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Subject: Specifications for SPI transceivers

At the December meeting a list of SCSI transceiver specifications that are presently missing from any SPI documents was developed. Following is a list of these specifications.

A credible analysis of the bus length, ability to support hot plugging, ability to operate fast, and other key configuration variables is very difficult without most of these specifications.

Several chip vendors have indicated that they are willing to supply the data for their products - but the mechanics of collecting, collating, and presenting this information is presently lacking.

This document is intended to give hard copy of a description of the missing parameters and may serve as a crude outline for data collection and presentation.

Discussion of the mechanics of taking this effort forward is requested from the committee.

Drivers:

- .Is active negation used - if so on what lines?
- .Guaranteed assertion level at 48 mA
- .Guaranteed slew rate on assertion
- .Worst case skew on the same chip
- .Capacitance/inductance at the chip pin
- .Power off leakage
- .Active negation
  - voltage clamping limits if any
  - current sourcing limits
  - time to tristate after turn on
  - tristate leakage
  - tristate transients

Receivers:

- .DC switching thresholds
- .Hysteresis levels (if any)
- .Input filtering: type / delay / which lines?
- .Worst case skew
- .Clamping?
- .General guaranteed glitch rejection criteria
- .Capacitance/inductance (again)
- .Input leakage (same as tristate leakage if active negation is used)
- .ESD protection
- .Latch up protection
- .Maximum/minimum high state input voltage level (latch up/oxide breakdown concern)