High Speed Serial Bus

Project 1394 of the Microcomputer Standards Committee of the IEEE Computer Society

Note:
49 Mbps 1394 physical layer
is updated to 100 Mbps w.2 e.
See attached document for
details.

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X3T9.2/91-172

Goals

- **Alternate Bus**
  - Bridging between different parallel busses
  - Redundant path for configuration and maintenance
  - For extremely low cost modules
- **Low cost peripheral bus**
- **Bus bridge**
- **Compatible architecture with other IEEE 32-bit busses**
  - Follow 1212 CSR standard (control and status register)

Goals (cont.)

- **Modest cost**
  - < $15 for cable, socket & interface ICs (very large volume)
- **High bandwidth**
  - Fast as possible given cost goals
  - Lower CPU overhead via simpler protocols & assumption of memory bus model
  - Performance extensibility
- **Add isochronous service**
  - from 64 kbps for voice to 1.5 Mbps for stereo HiFi sound to >20 Mbps for compressed video

"Isochronous" ??

- **Iso (same) chronous (time) :**
  - Uniform in time
  - Having equal duration
  - Recurring at regular intervals
- **Examples**

  (source and destination for real-time data)

ISDN	8 kHz x 8 bits	64 kbps
CD	44.1 kHz x 16 bits x 2 channels	1.4 Mbps
DAT	48 kHz x 16 bits x 2 channels	1.5 Mbps
Video	25 or 30 fps	variable

Goals for External Cable

- **Reduce EMC problems**
  - Low voltage swing, low current, low skew differential signal.
  - Shielding & isolation designed in from the start.
- **Improved ergonomics**
  - Small, flexible cable
  - Robust small connectors with self-locking feature
  - No terminators, few topology rules

Goals for Backplane

- **Two conductors (single-ended)**
  - Two differential pairs for compatible busses (SCI)
- **Direct repeater to cable media**
- **Usable in FastBus, Futurebus, VME, NuBus, Multibus II, SCI**

Unsupervised!

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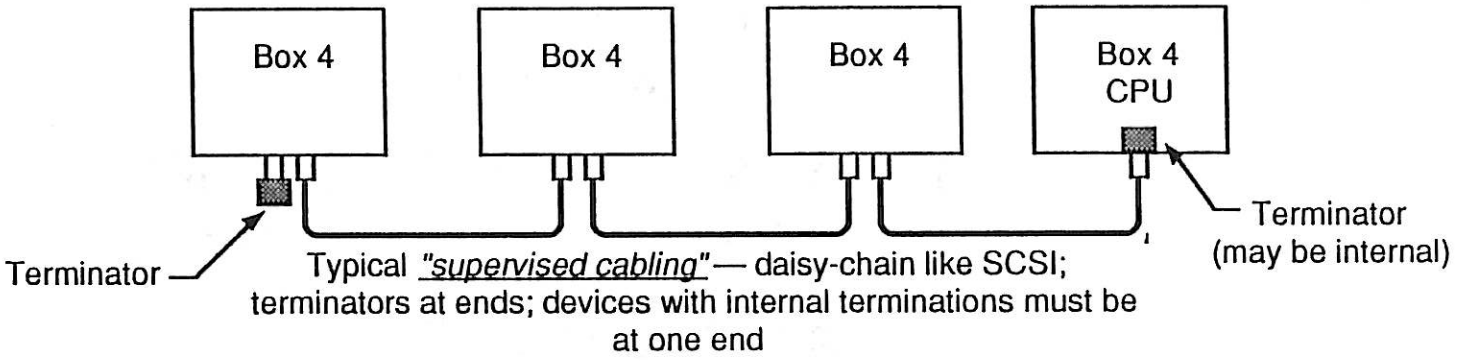

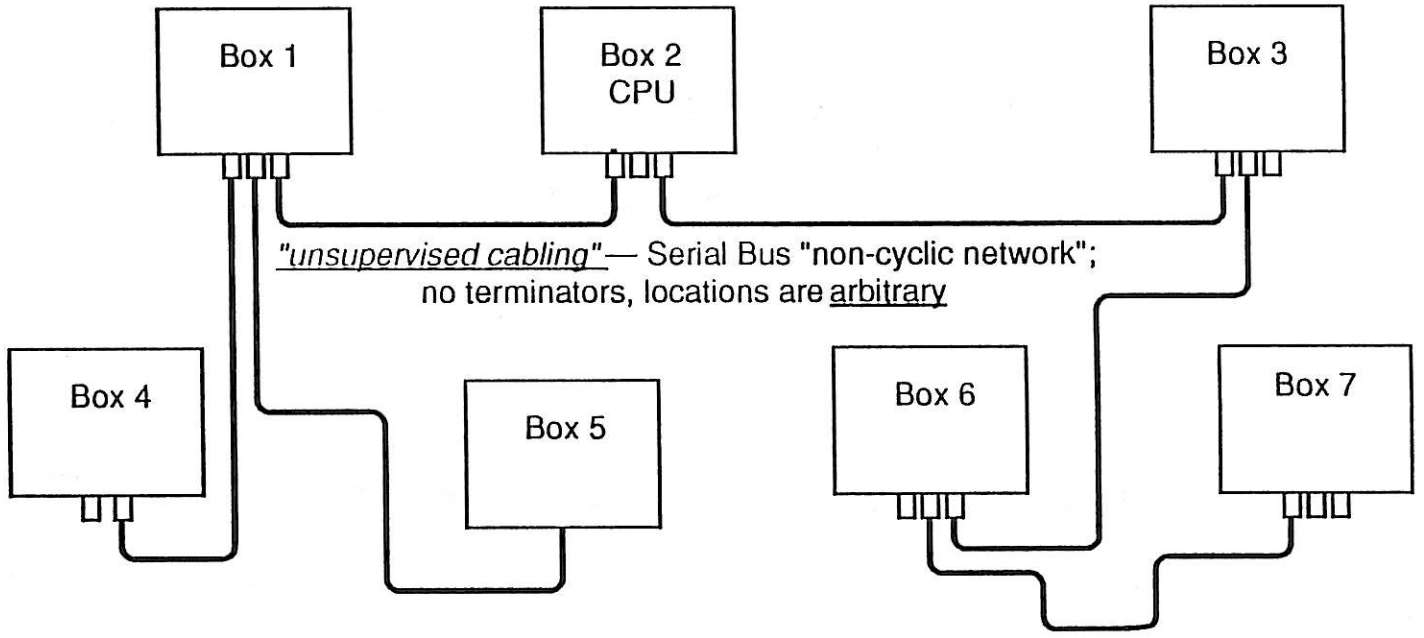

Protocols

- **P1394 High Speed Serial Bus**
  - "Memory-bus-like" logical architecture
  - Serial implementation of 1212 architecture
- **1212 CSR Architecture**
  - Standardized addressing
  - Well-defined control and status registers
  - Standardized transactions
  - Standardized DMA and other Unit-specific features in the future

1212 Module Architecture

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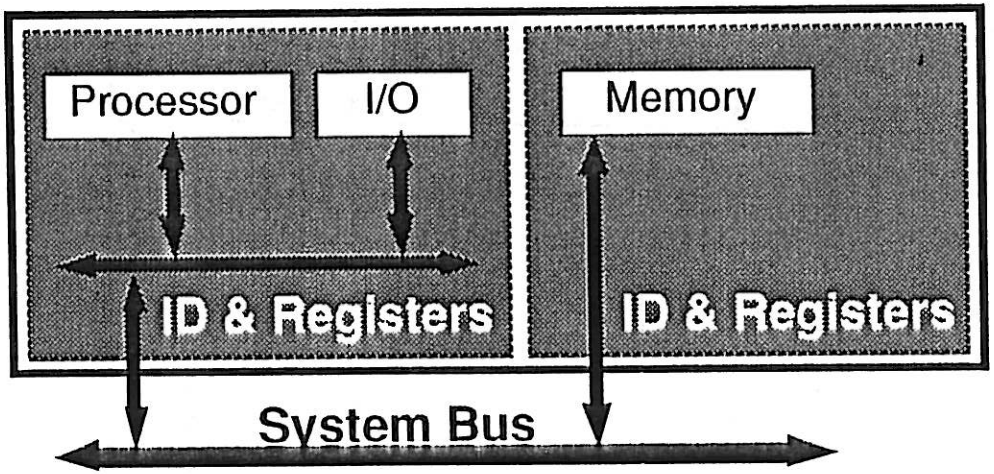
Module Architecture



Module	Replace together
Node	Initialize and test together
Unit	Independent in normal operation

1212 Addressing

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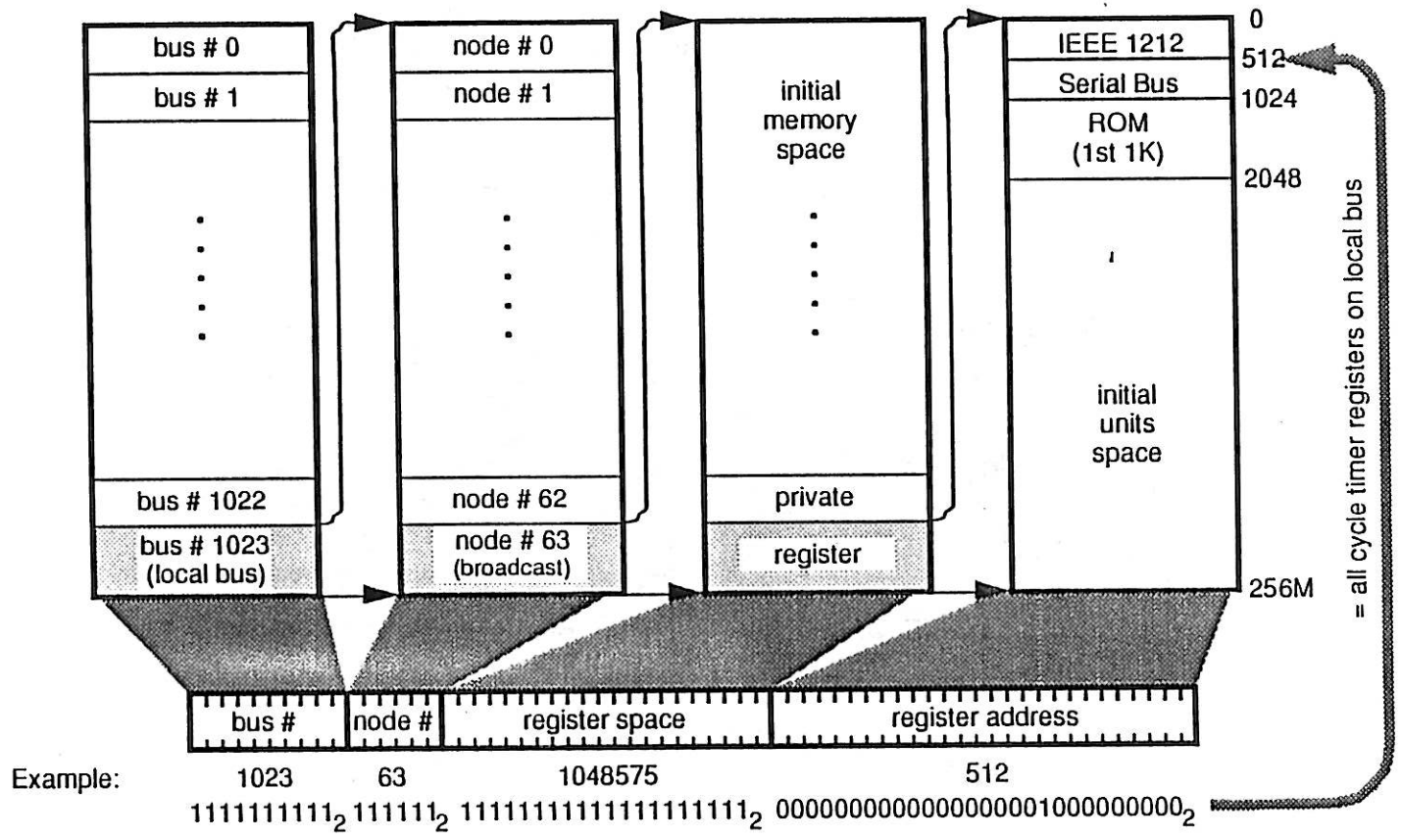

- **The serial bus uses 1212 direct 64-bit addressing**

Protocol Stack

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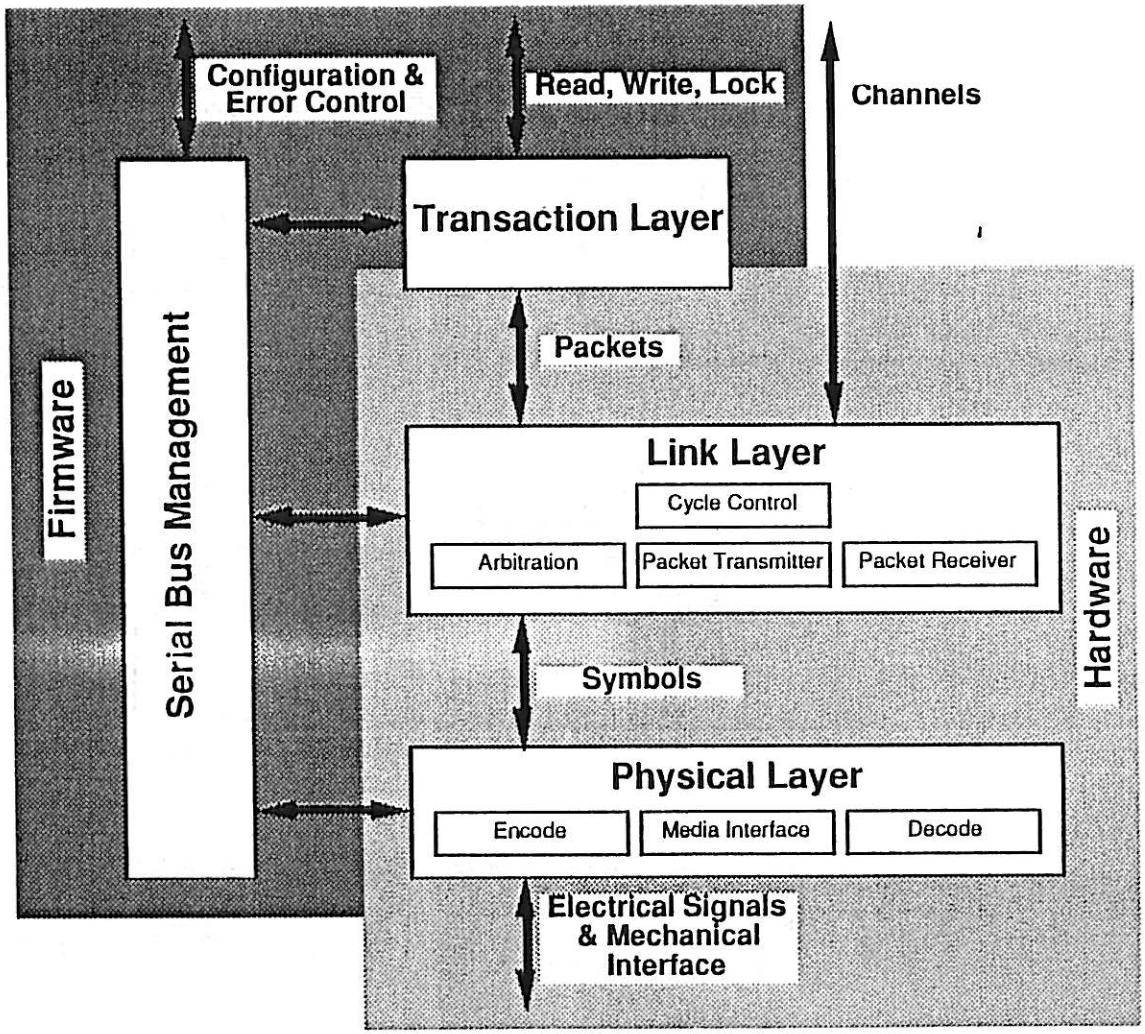

Physical Layer Topology

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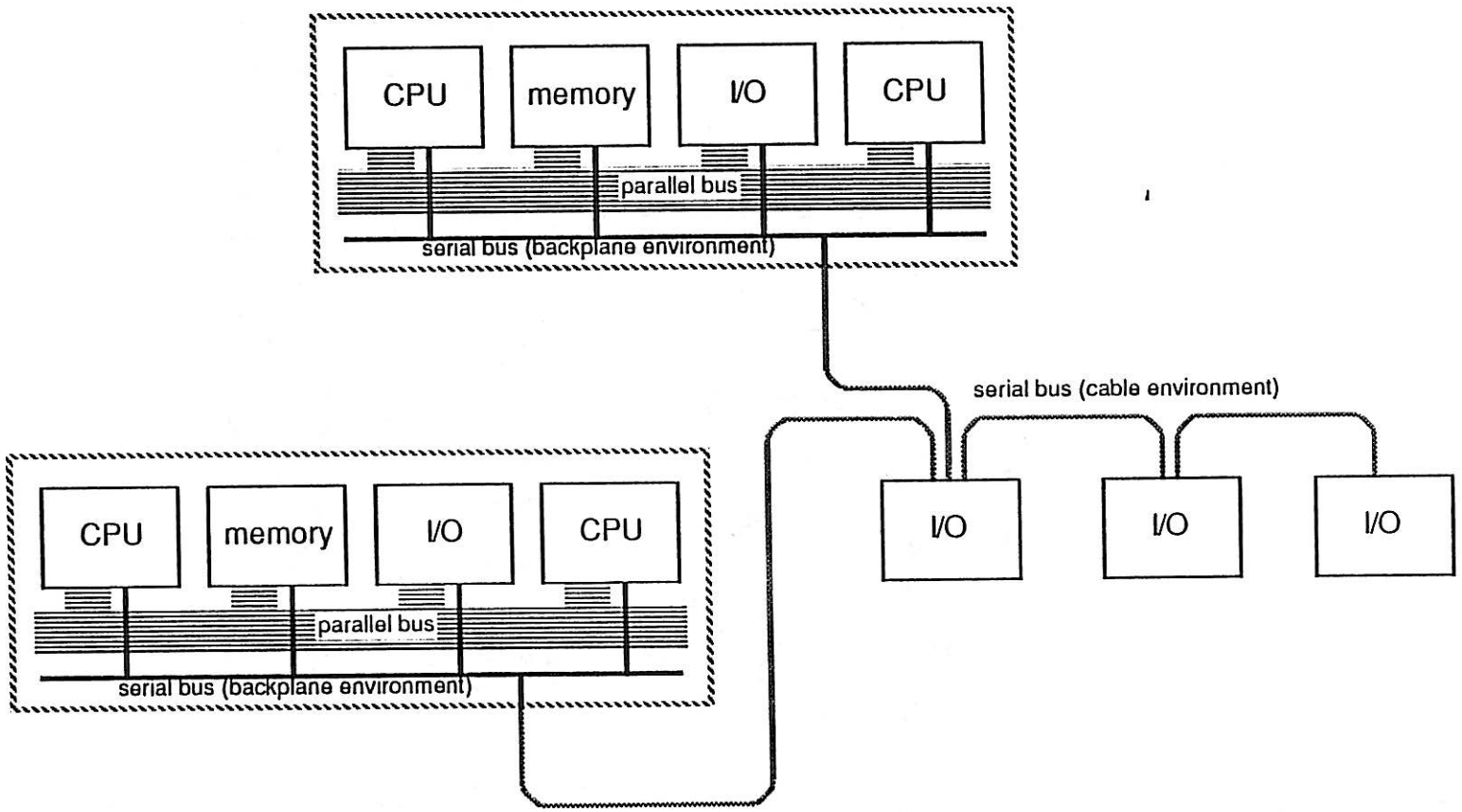
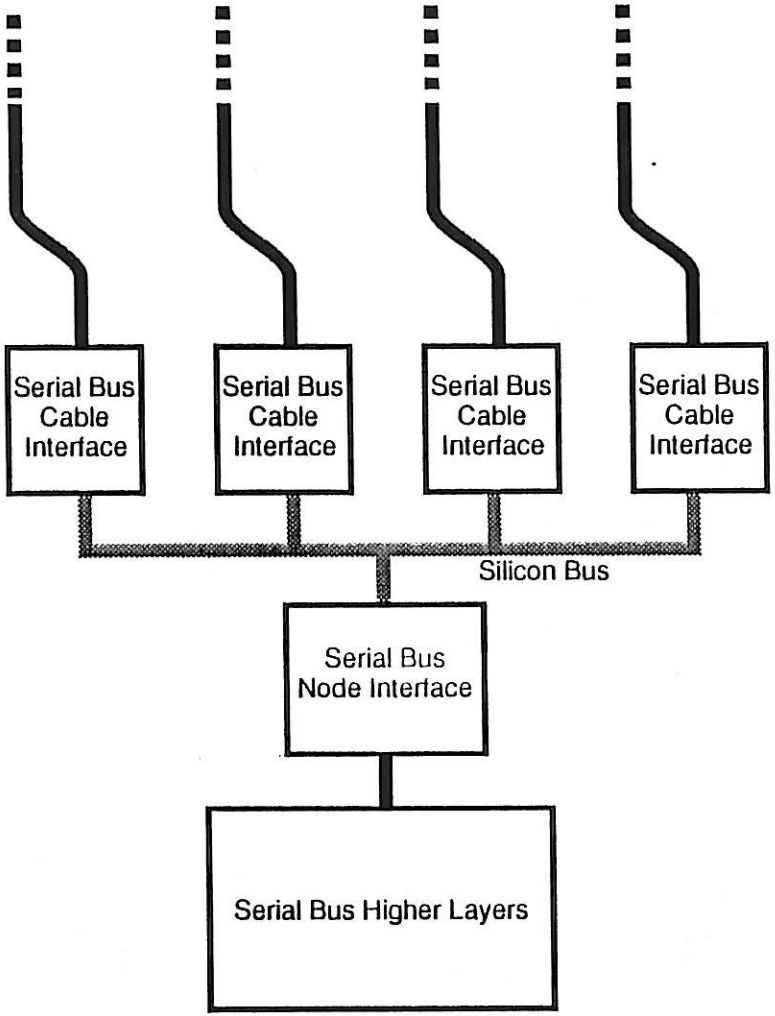
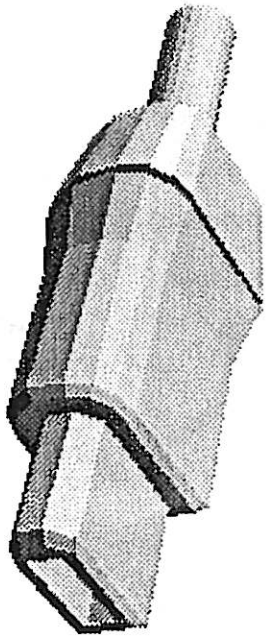


Cable Interface



- Silicon bus provides "or"ing of signal
- Cables and transceivers are bus repeaters
- Limit of 6 cable hops and 10 meters of cable between any two nodes

Cable Interface Features



- **3-pair shielded cable**
- **Small and rugged connector**
  - Two sockets in the same area as one mini-DIN socket
- **CMOS transceiver**
  - 300 mv peak-to-peak
  - 4 ma drive
  - < 160 ps random jitter (at 6 sigma)
  - < 500 ps worst case jitter

Cable Assembly Example

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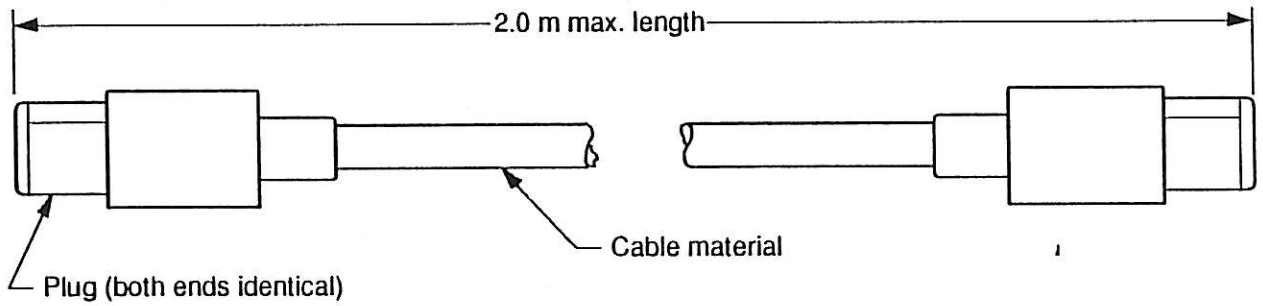
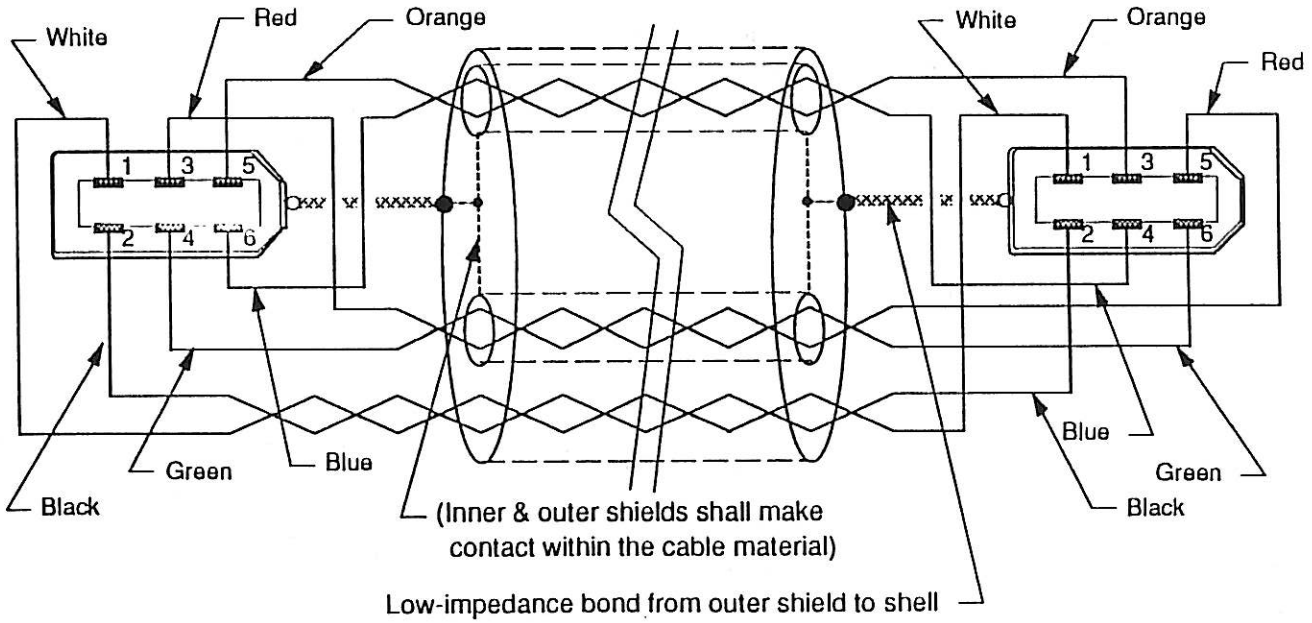


End "A"

End "B"



Cable Media Example

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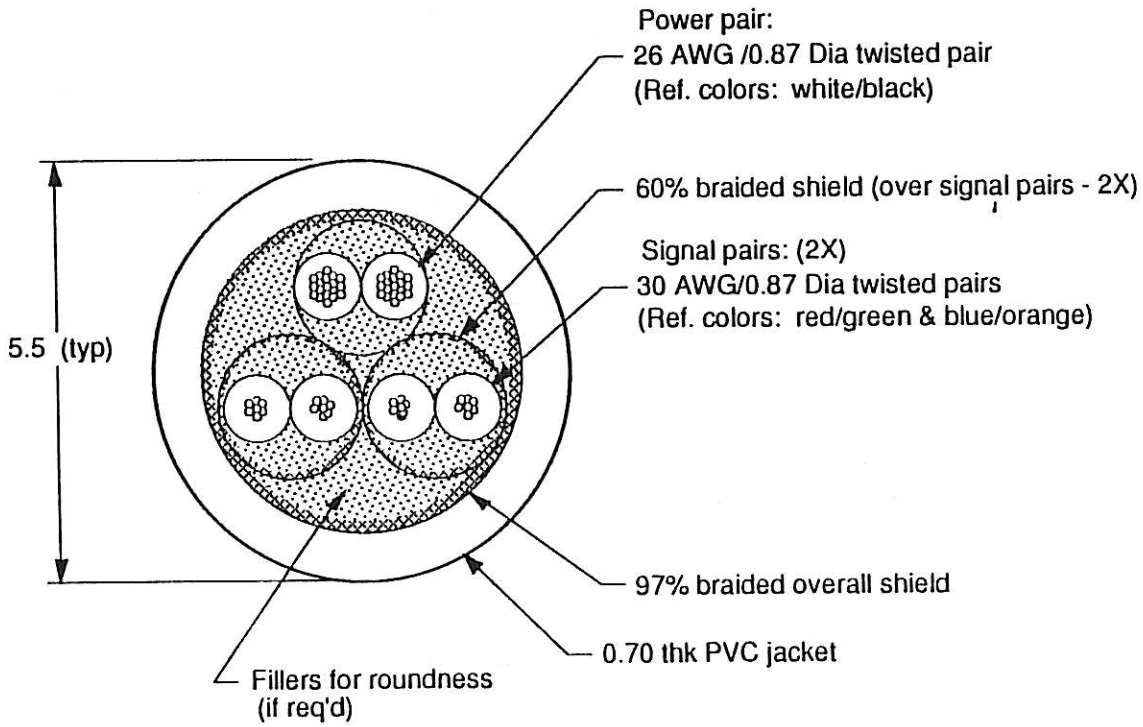

Notes:
1. Signal pairs impedance Zo = 115 Ω nominal
   (Dielectric is foamed polyethylene, εr = 1.7)

- **Capable of operation beyond 400 Mbaud for a few metres**

Cable Interface Features

- **Live attach/detach**
  - System protected from power on/off cycling
  - Higher layers provide simple management
    - remote power control
    - "I'm here!" message to notify monarch
- **Peripheral power**
  - 8-40 VDC carried by cable
  - Each peripheral interface needs 1/4 - 1/2 watt while active
  - Total available power is system dependent
    - Node power requirements must be declared in configuration ROM
  - Cable system allows up to 1.5 A (60 watts) per link
    - Nodes can either source or sink power
    - Multiple power sources on one bus provide additional flexibility
  - Further specification needed

Physical Layer

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- **49.152 Mbaud data transport**
  - DAT, ISDN & compressed video rate-compatible
  - 2 Mbaud full duplex rate for arbitration and acknowledgement
  - 196 Mbaud growth path
- **Data encoding**
  - 4B5B block code with NRZI translation for simple clock recovery with good efficiency
  - Yields ≈ 40 Mbps burst data rate

Link Layer

- **Flexible addressing using 1212 architecture**
  - Direct 64-bit addressing (48 bits per node)
  - Hierarchical addressing for up to 63 nodes on 1023 busses
  - Standardized register addresses
- **Flexible packet formats**
  - Optimized for 4-byte data
  - Optional 0-256 byte packets
    - Longer packets at higher speeds
    - Actual limit is 60 µsec per packet
- **Immediate acknowledge**
  - Normal ack < 1 µsec
  - Non-hogging retry mechanism

Link Layer (cont.)

- **Fair and urgent access**
  - Bit-serial arbitration
  - Automatic assignment of addresses
  - Access opportunities split between fair and priority modes
- **Isochronous transport**
  - Optional
  - Multiple "channels" each 125 µsec "cycle" period
  - 41 ns max jitter in 125 µsec clock
  - Variable channel size up to ~480 bytes/cycle
    - Up to ~1900 bytes/cycle at 196 Mbaud

Link Layer Operation

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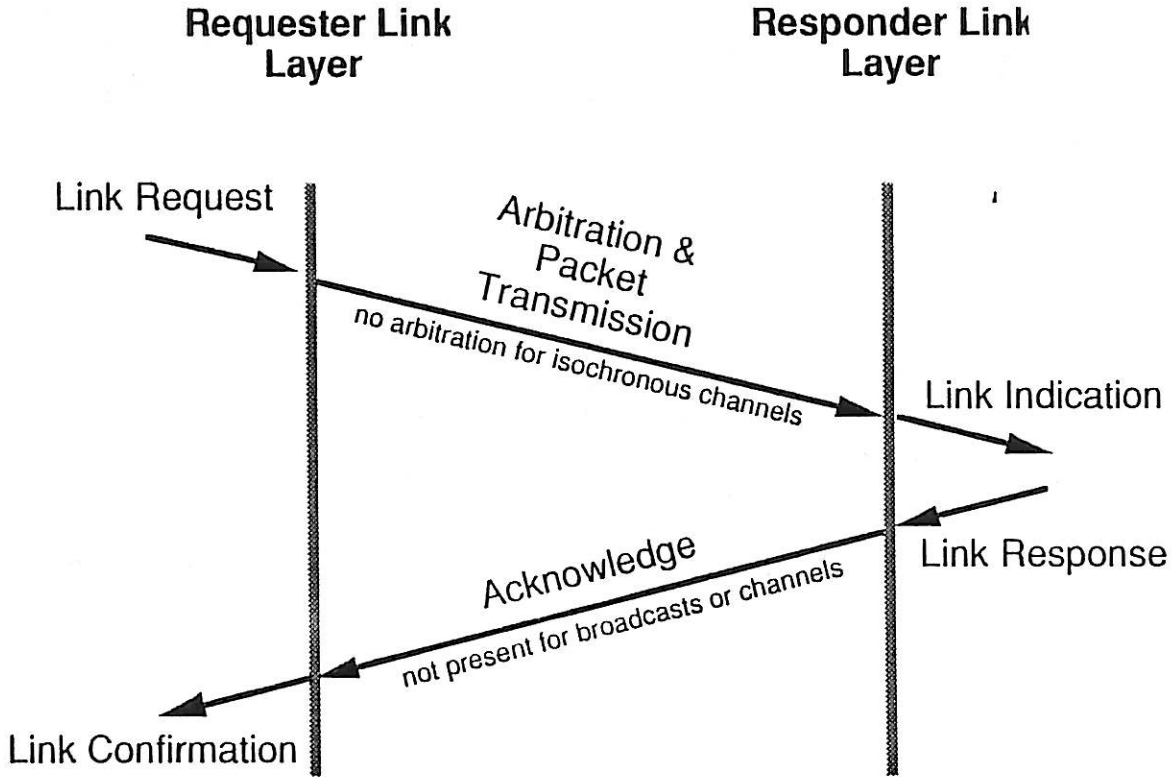

Example Packets

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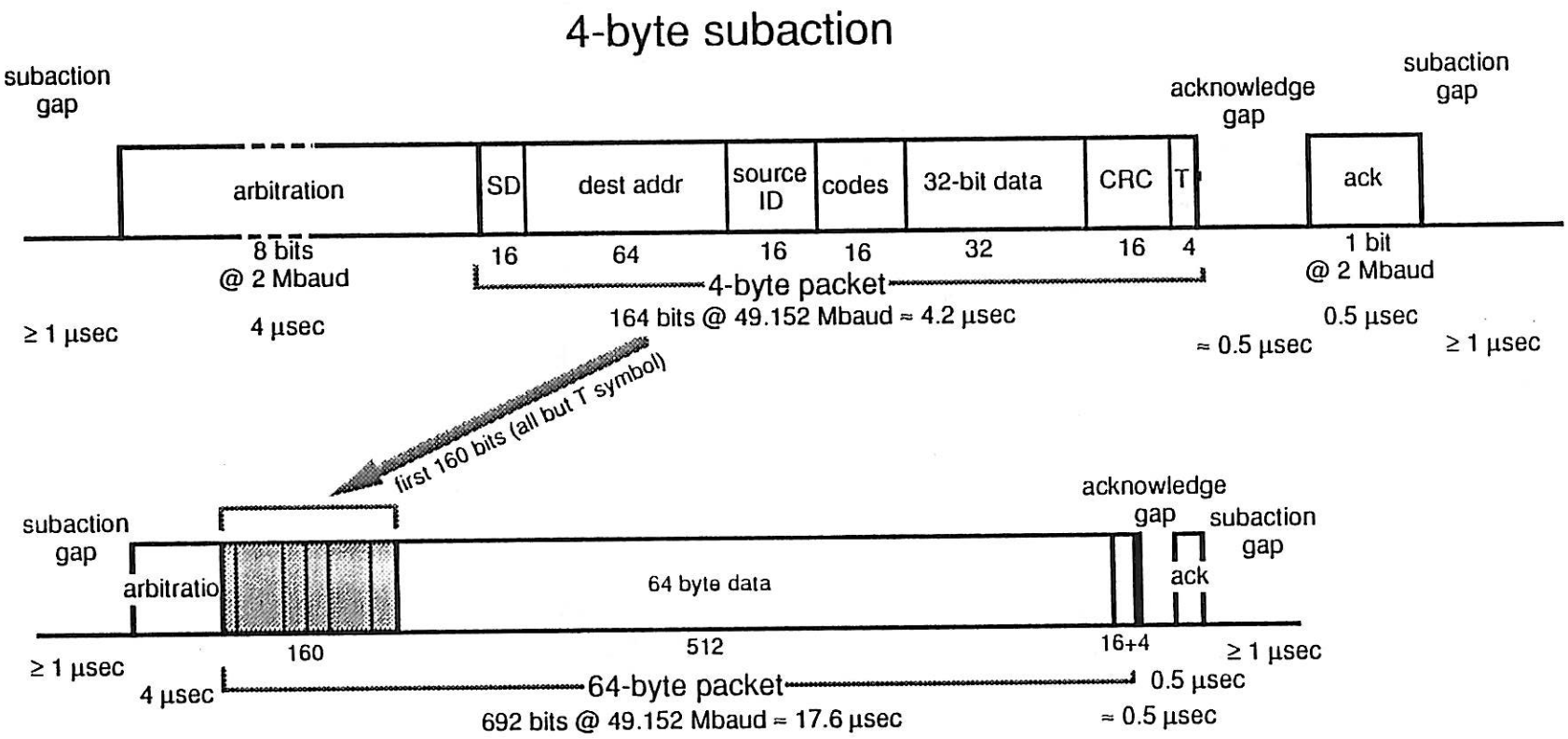
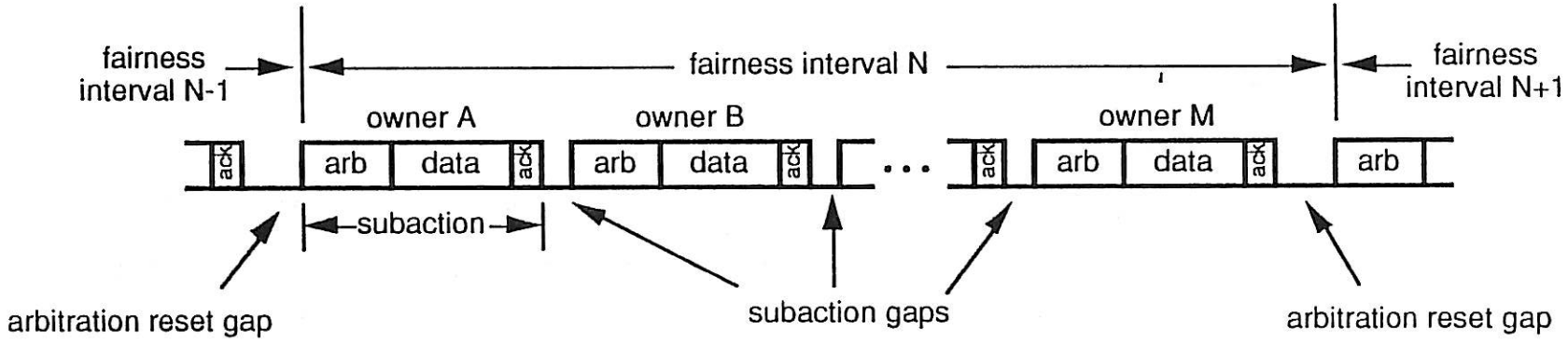
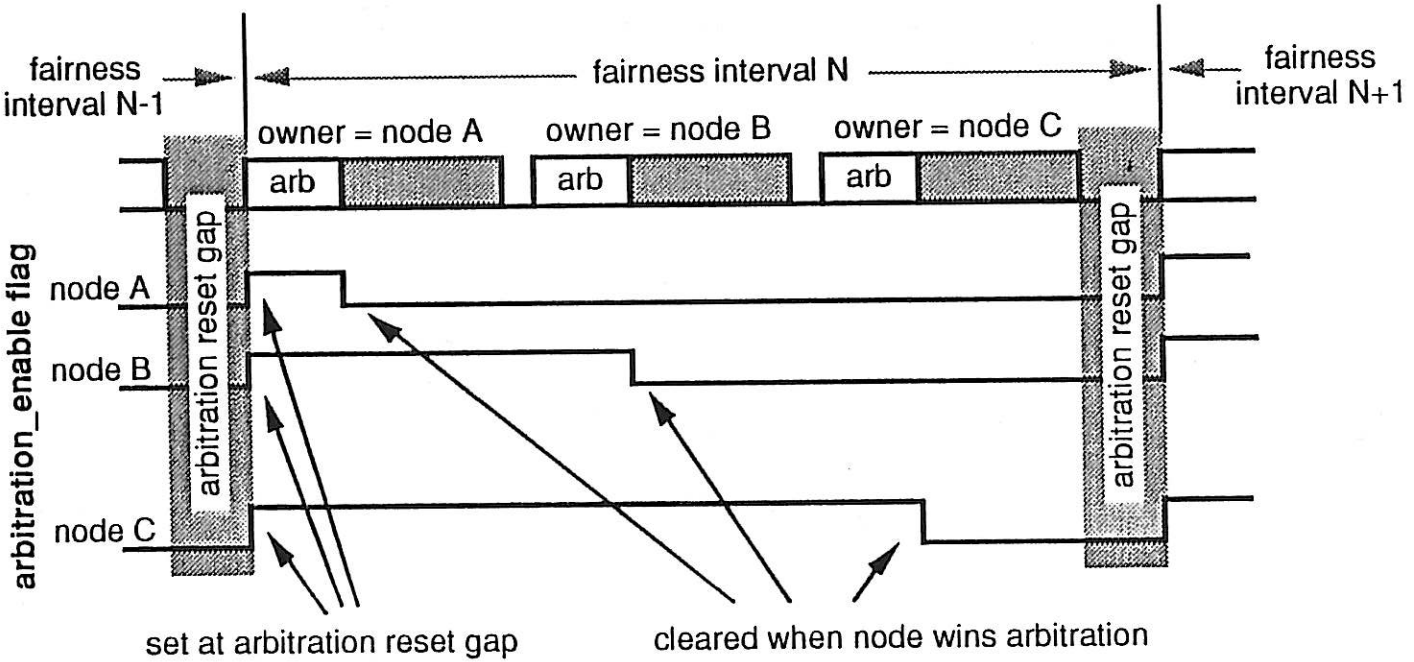


Fairness Cycle



- **Fairness Cycle is bounded by arbitration reset gaps**
- **Reset gaps are longer than normal subaction gaps**

Fairness Arbitration



- **Each node gets one access opportunity each Fairness Cycle**

Fair & Urgent Access Sharing

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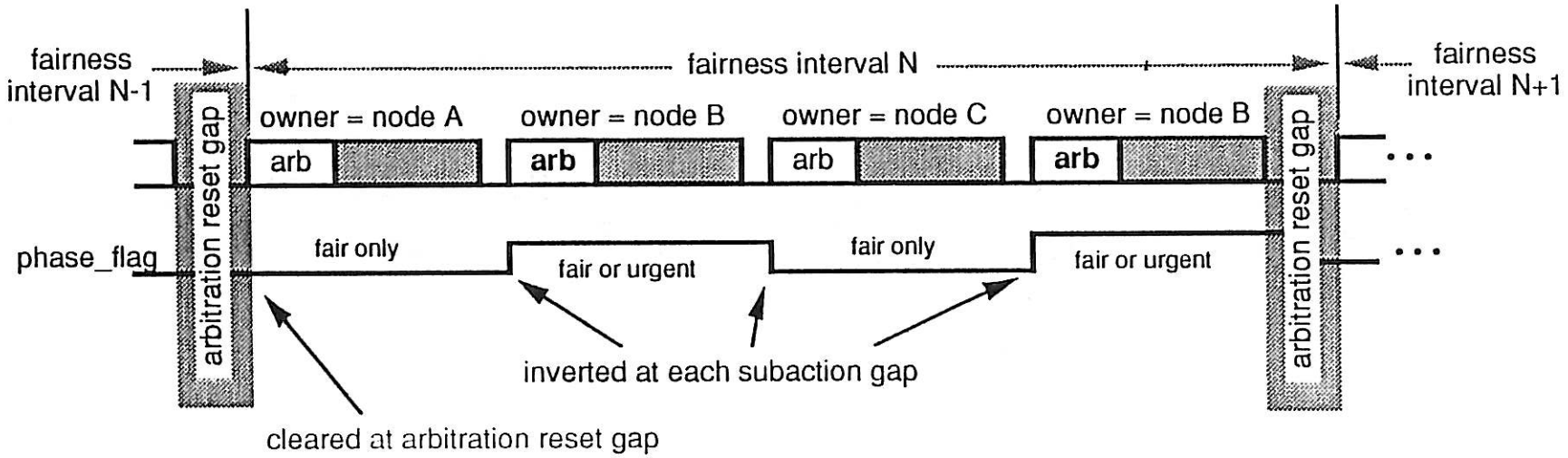

- **Node ID of A > node ID of B > node ID of C**

Cycle Structure

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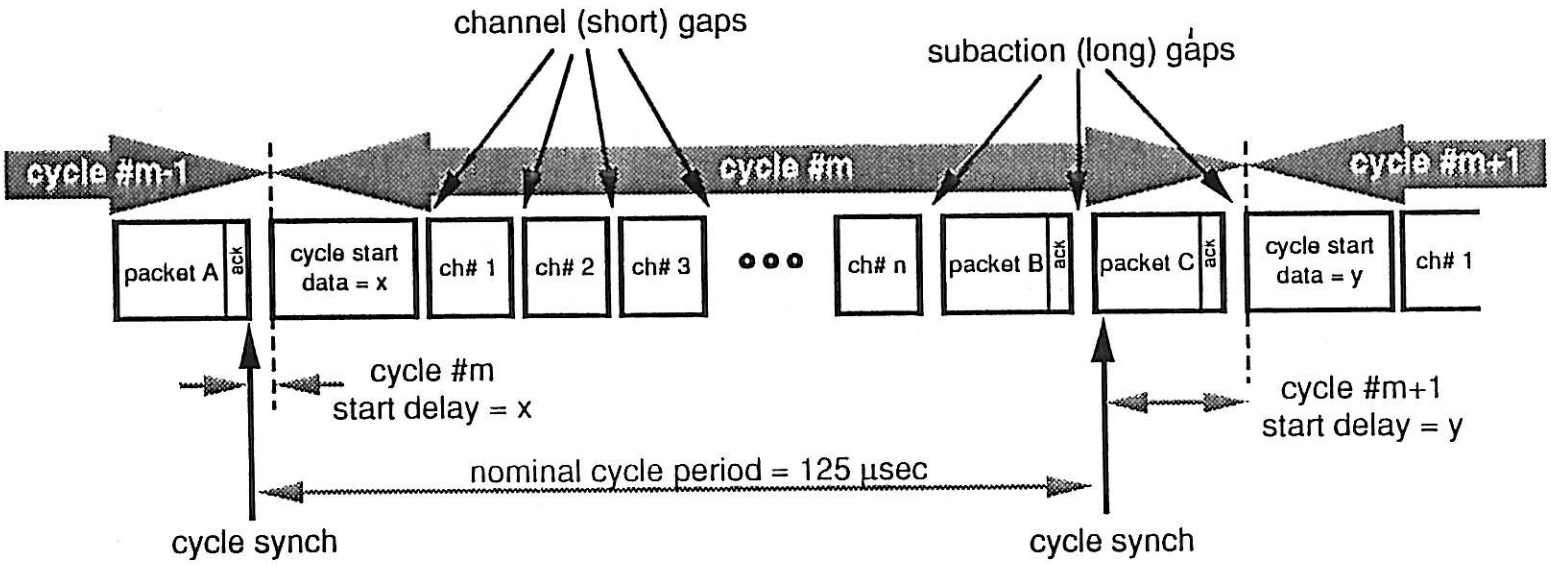

Transaction Layer

- **Multiple transaction types**
  - Optimized for 4-byte operations
  - Read and write quadlet are required
  - Variable-length block operations optional
  - Lock transactions optional
    - Swap and Compare-and-swap are needed for distributed sharable-list DMA
- **Advanced management**
  - Automatic address assignment (no switches)
  - Standardized addresses from 1212 architecture
    - command, status, interrupt, etc.
  - Configuration ROM from 1212 architecture
    - device type, name, manufacturer, power requirements, capabilities, driver code

Transaction Layer Operation

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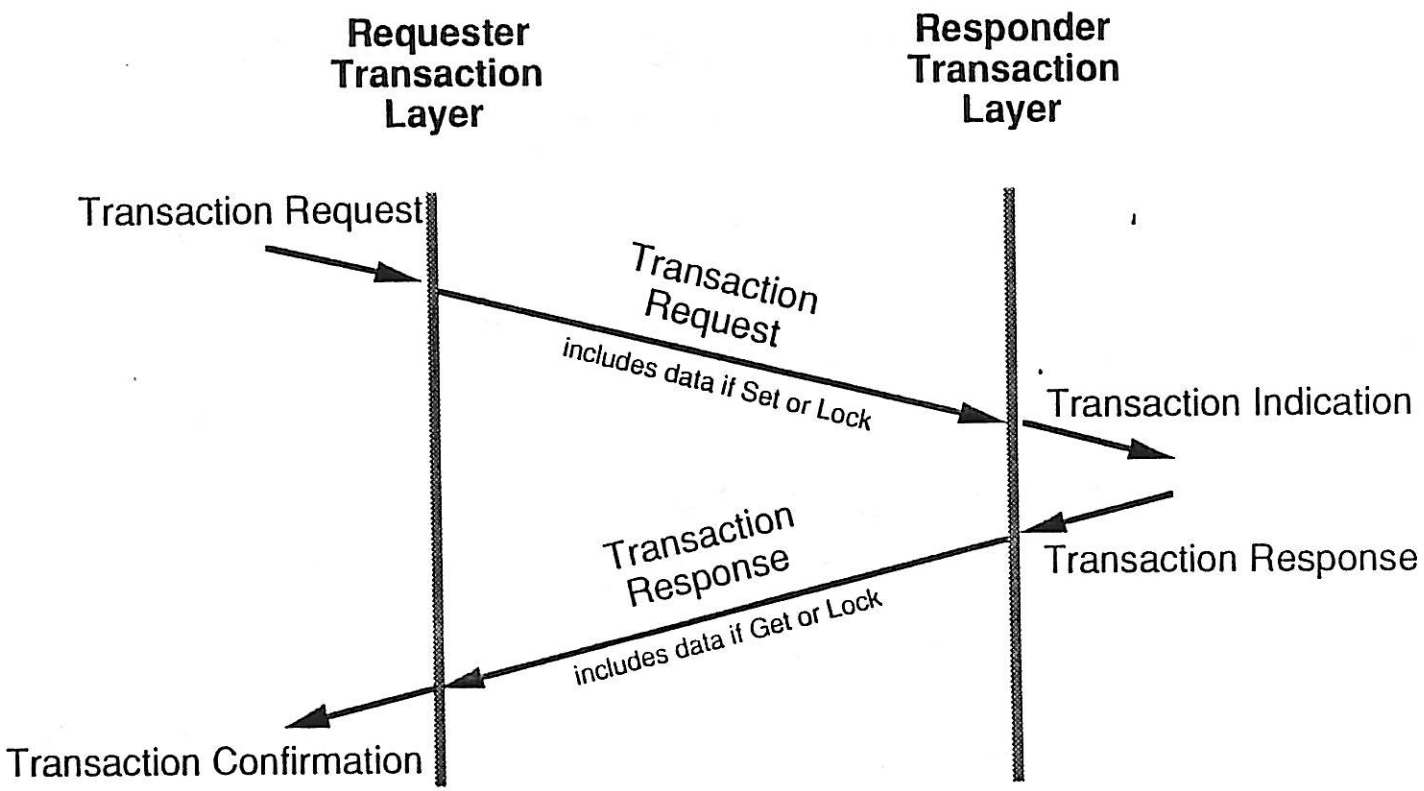

Split Transaction

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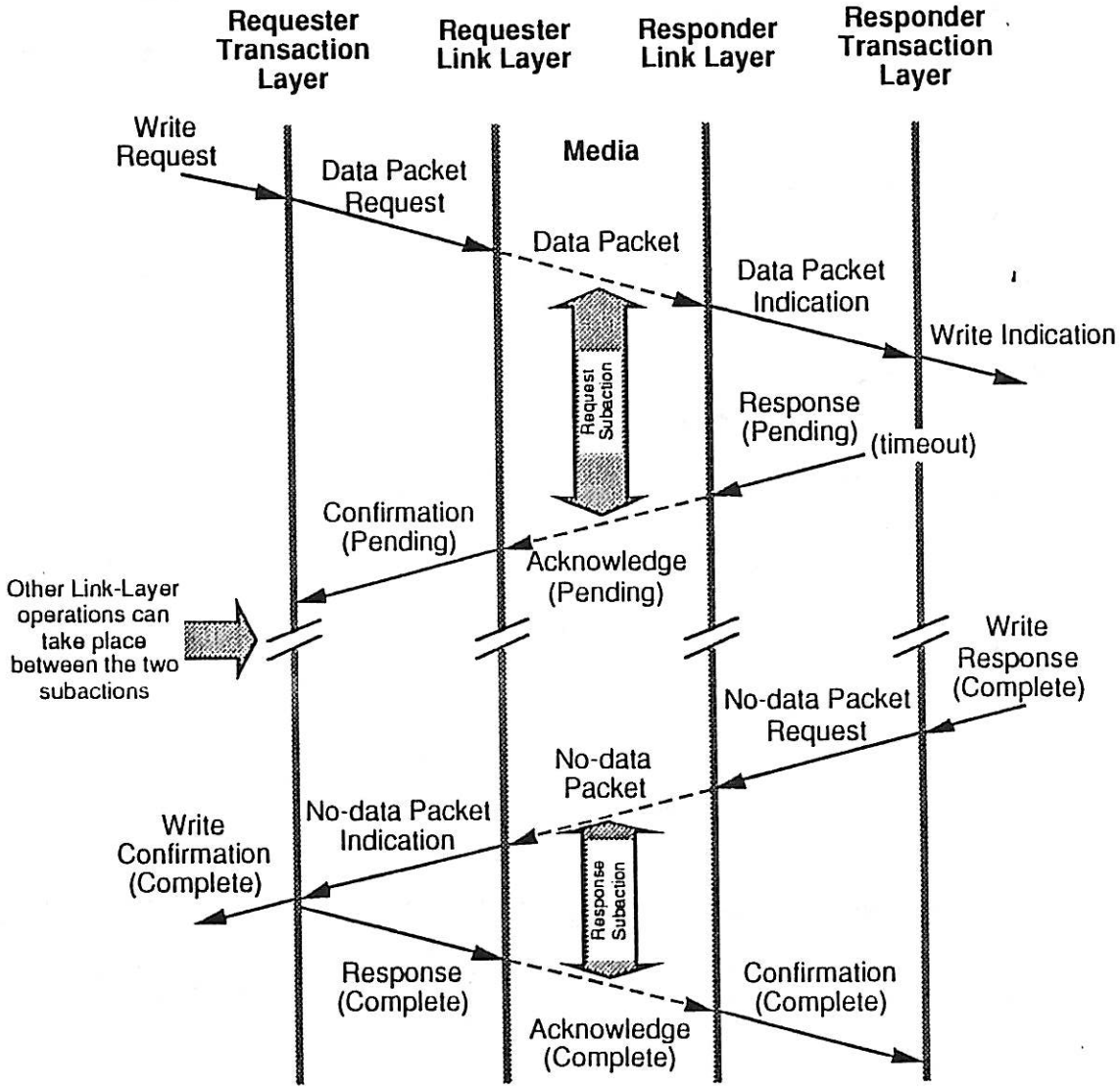

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Fast Transaction

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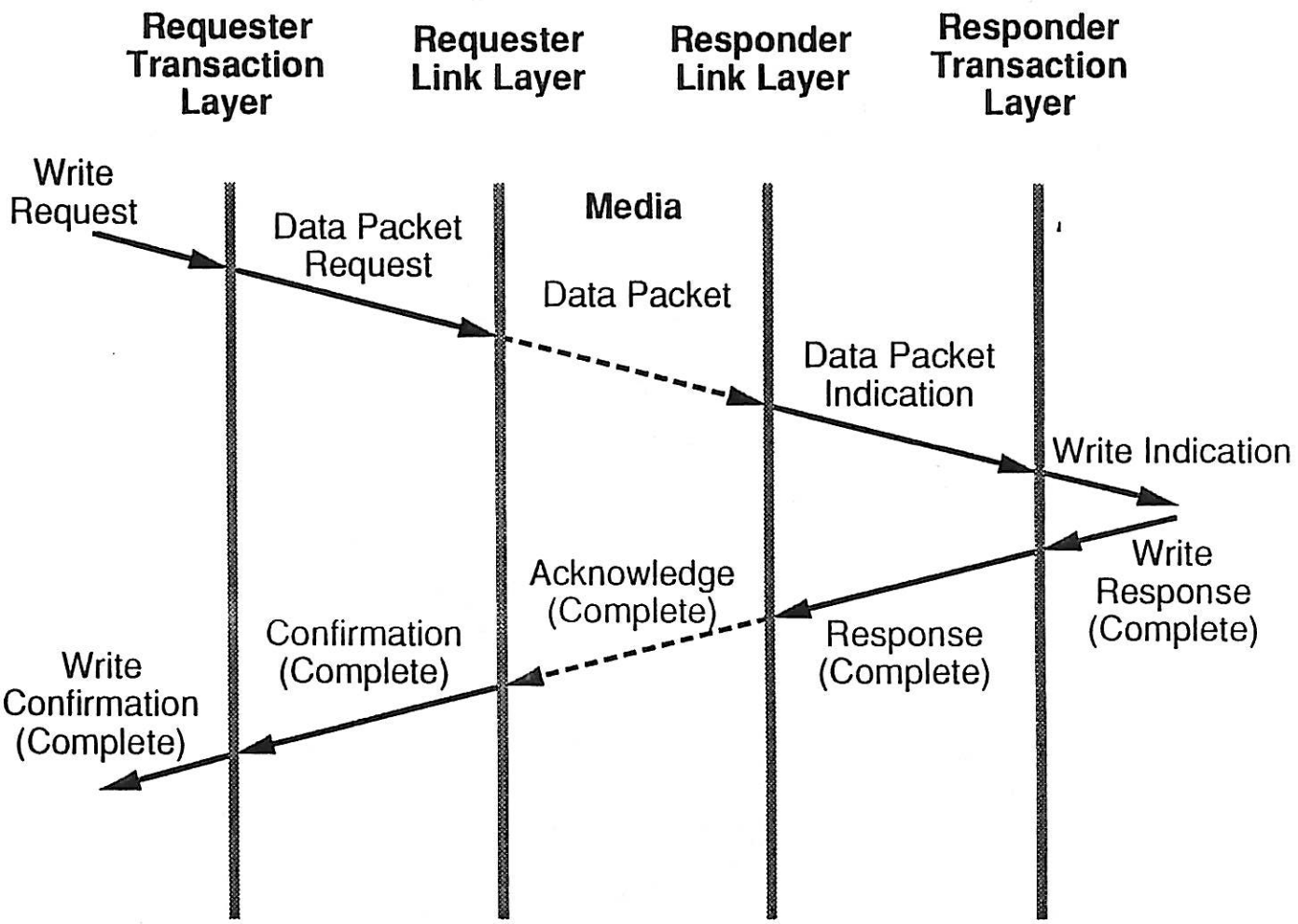

Higher Layers

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- **Configuration**
  - Using 1212 configuration ROM
  - Automatic minimal configuration
  - Extensive self-identification possible
  - Software finishes configuration, possible user interaction
- **Bridges to other busses**
  - Full support for 1212 transactions and addressing
  - Can use LAN as bus extender
  - High interest in SCSI adapter
- **DMA standard in development**
  - Part of P1212.1 standard
  - Need standard command interface
    - Unfortunately beyond scope of P1212.1

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Development Schedule

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- **Current draft 4.1**
  - Link layer and transaction layer mostly complete
    - Detailed simulation has been completed
    - Minor changes to fields have been proposed
  - Physical layer needs more work
    - Initial simulations and implementations look good
    - Connector & cable work almost complete
    - Scalable speed/lower cost proposal coming
- **Working group to be finished winter-spring 1992**
  - Formal approval within working group
  - Foward to Microcomputer Standards Committee

Resynchronizing Physical Layer

Michael Teener
Roger Van Brunt
Florin Oprescu
Apple Computer, Inc.
September 10, 1991

Why Change Now?

- **History**
  - Pressure to increase speed and lower cost
    - I/O bus requirements increasing fast
  - Clock recovery most complex part of Physical Layer
  - Possible patent problems with 4B5B code
- **Roger & Florin observation:**
  - 2nd signal pair unused during packet transmission
  - Use to carry explicit clock
- **Further improvements**
  - Resynchronize data at each node
  - Automatic speed scaling

Advantages

- **Simpler**
  - No analog circuitry for clock recovery
  - No coding of data to guarantee clock edges
- **Higher performance**
  - Single hop for clock and data before resynch
  - Jitter margins much improved
  - 100 Mbit/sec for the same or lower cost as 40 Mbit/sec
- **Scalable performance much easier**
  - 200 Mbit/sec possible very, very soon with CMOS
  - 400 Mbit likely with BiCMOS technology

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Basic Design

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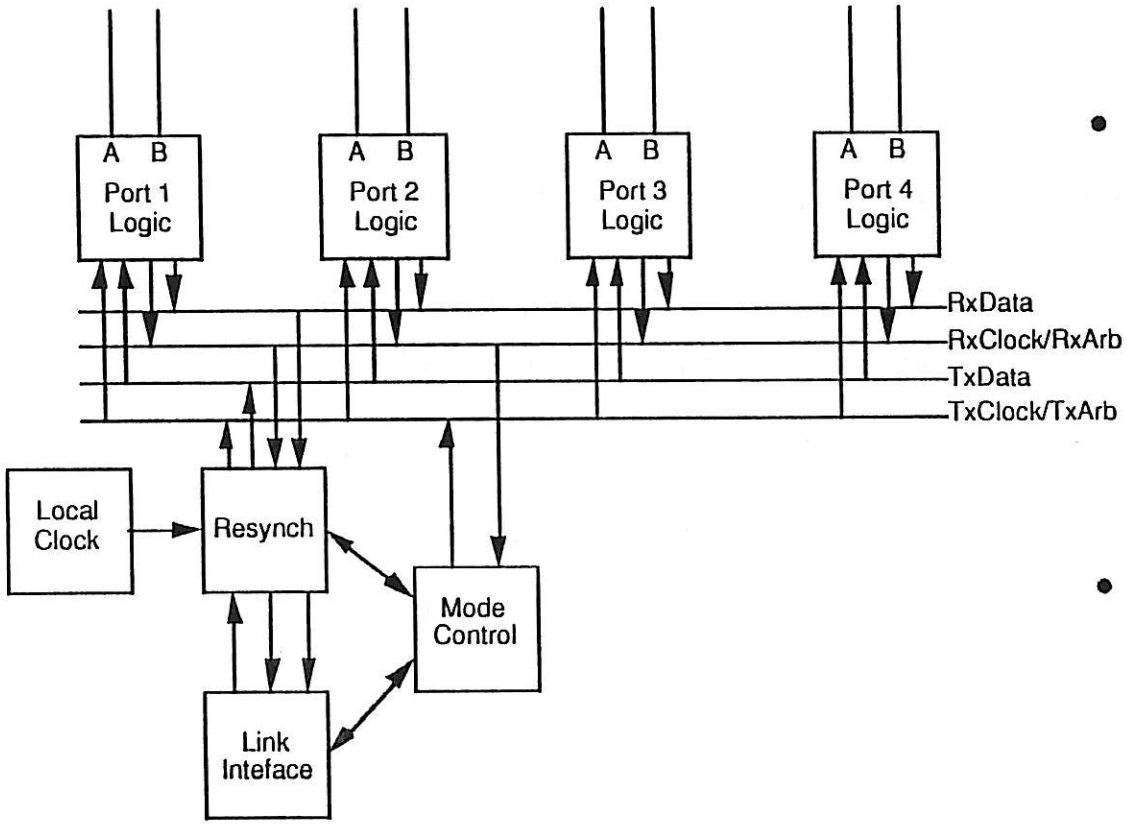

- **Redefine TPO and TPI interface signals**
  - TPA is transmit arb, transmit clock, receive data
  - TPB is receive arb, receive clock, transmit data
  - Both are bidirectional signals
- **Resynchronize repeated packet data signals**

Mode Shifts

- **Arbitration operation is unchanged except:**
  - TPA is tristated after driving signal pair to "0"
  - Hysterisis required on receivers
- **Shift to packet mode (resynch)**
  - On winning node, start driving TPB high
  - On losing nodes, port that is receiving arb signals will see a high signal on TPA.
  - Starts driving TPB on other ports.
- **Shift back to arb mode at end of packet (no clock)**

Arbitration Data Flow

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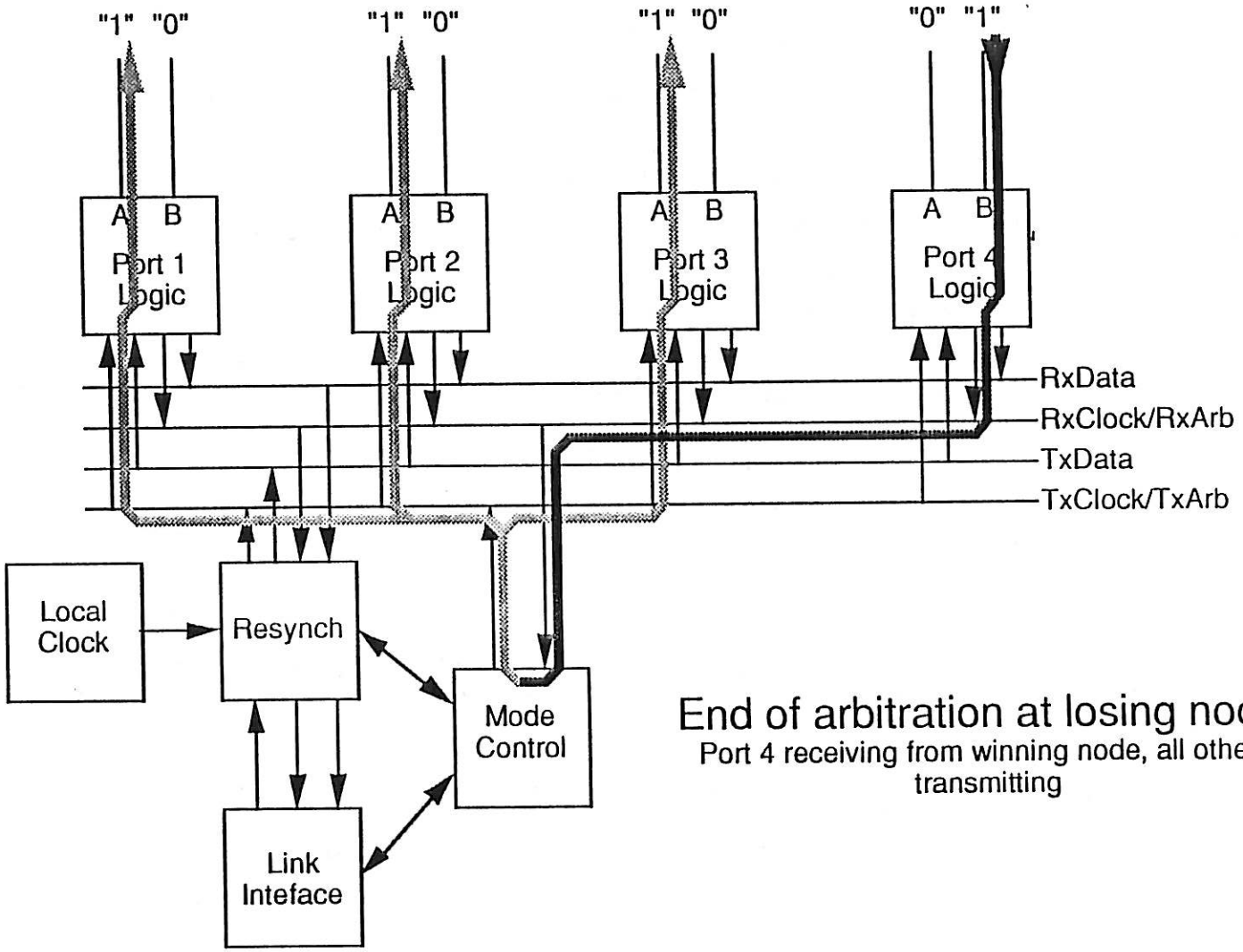

End of arbitration at losing node:
Port 4 receiving from winning node, all others transmitting

Data Packet Repeat

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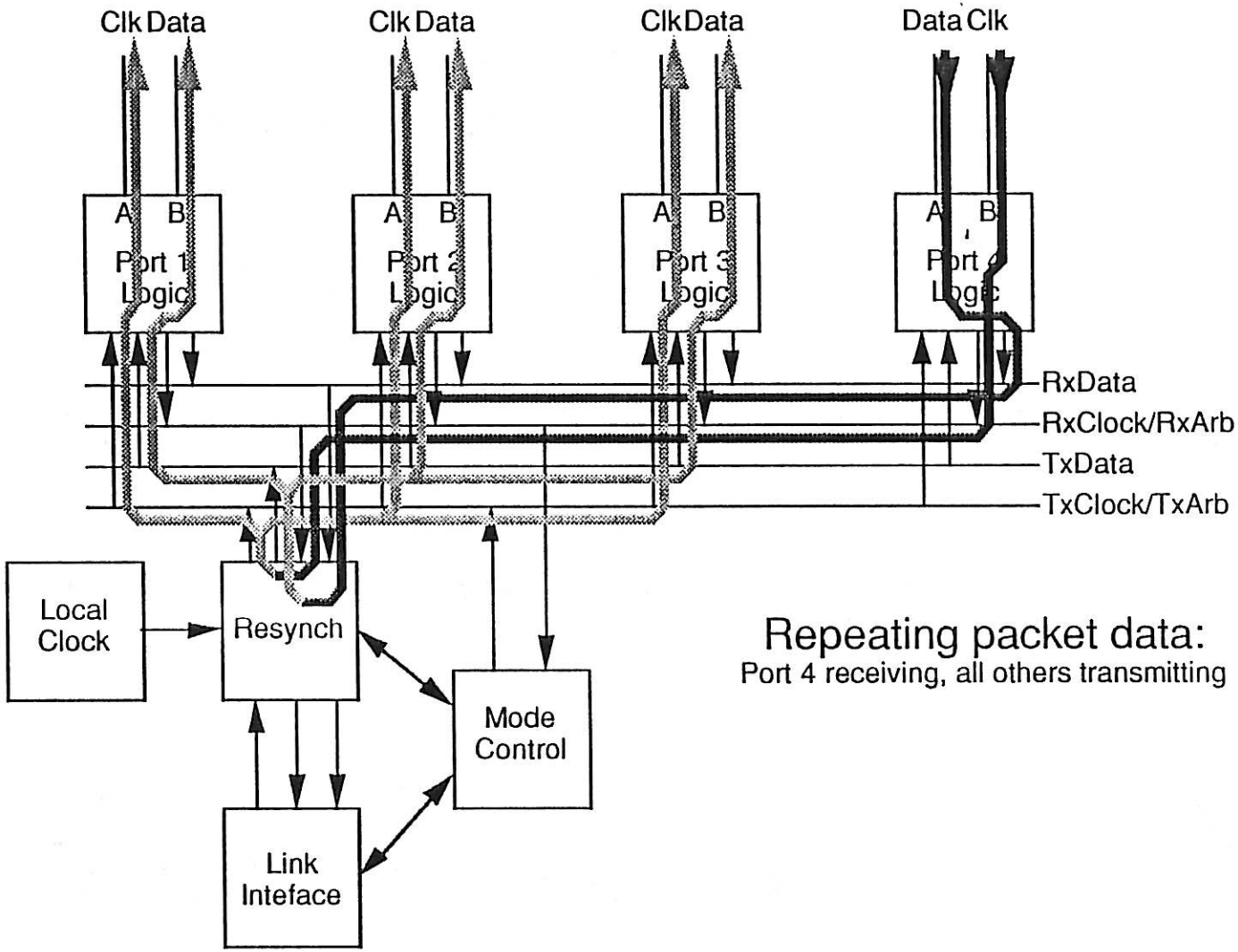

Repeating packet data:
Port 4 receiving, all others transmitting

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Packet Data Encoding

- **First data bit is clocked at 100 Mhz**
- **If high, double clock speed and get next bit**

  Repeat until a low data bit is found
- **If low, clock is unchanged**

  Next bit is start of link packet

Example Packet Start

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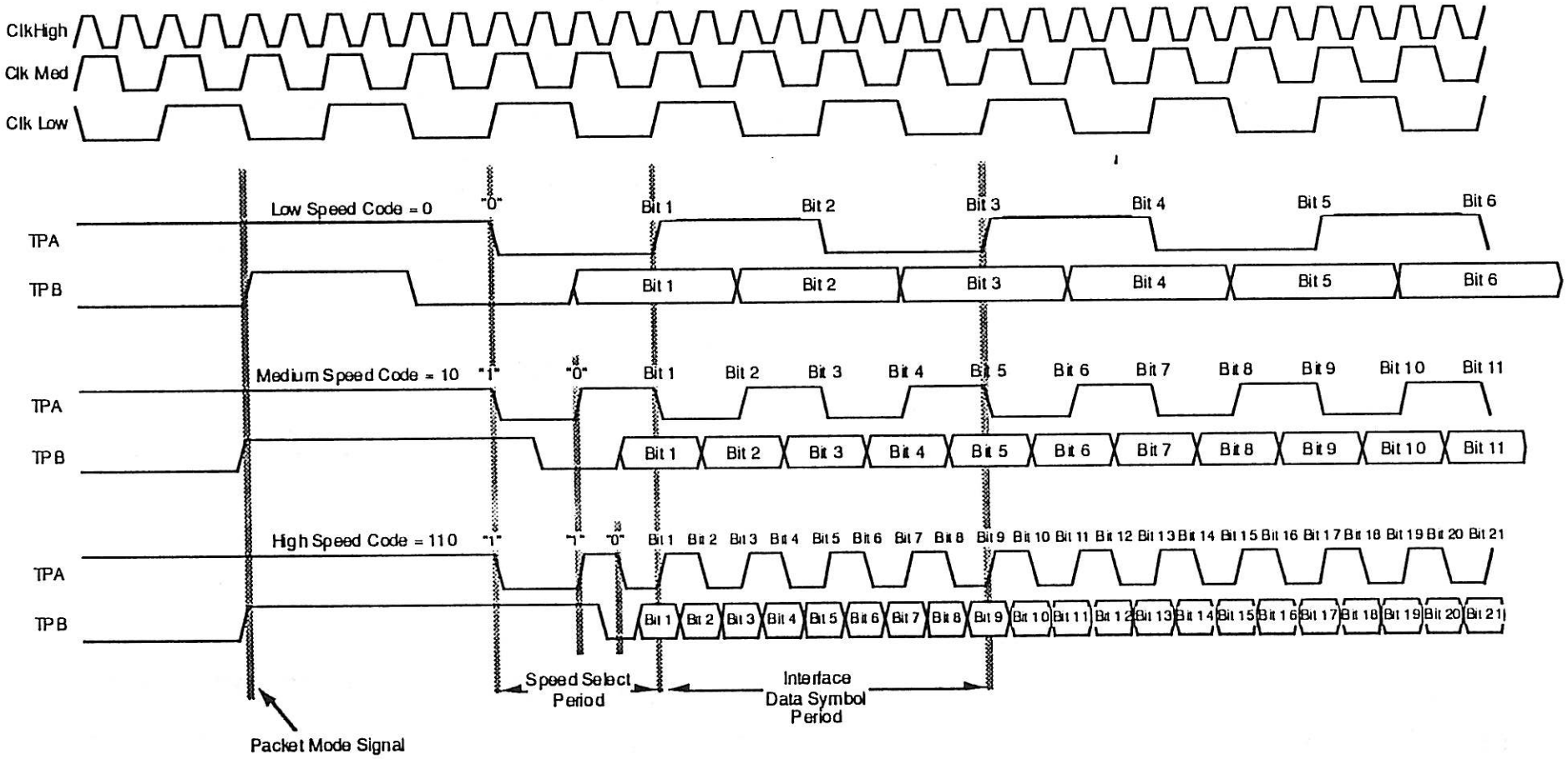

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Link Layer Changes

- **No 4B5B code**
  - Just NRZ data
- **Variable speed**
  - Speed code associated with each packet
  - Implementations probably use variable width interface
    - 2 bits @ 50 Mhz = 100 Mbits/sec
    - 4 bits @ 50 Mhz = 200 Mbits/sec
    - etc.

System Concerns

- **Configuration ROM must include speed capabilities**
  - Requester free to use higher speed if responder and the path to it is capable
- **Backplane interface**
  - 100 Mbit/sec possible with ECL
  - What are BTL limits?
- **Do we want to specify an upper limit?**