X3T9.2/90-196

---------- NCR Intracorporation

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Subject: Feasibility Of Totem Pole Termination for Low Power Differential SCSI

Attached is a document that examines the feasibility of using the old differential SCSI termination architecture for low power, high speed differential SCSI. It is possible to use the old architecture and consume only 1 Watt of power for the bus drivers. The following specifications would need to be imposed:

Rterm	650/135/650	Ohms
VOD	0.5	Volts
|VID|	0.2	Volts
VDD	4.5 - 5.5	Volts
Vterm	4.0 - 5.25	Volts
VOcmr	1.0 - 3.5	Volts
VIcmr	0.0 - VDD	Volts

order to meet the speed requirements of 20MEG xps, the drivers should be totem pole but with only active assists in one direction and continuous drive in the other. These power figures are based upon only 13 drivers being active at once.

If you have any questions, please feel free to give me a call.

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This document examines the feasibility of using the old differential SCSI architecture for low power, high speed differential SCSI. The dominant concern with this method is power consumption. IC driver power should be limited to a total(driver, receiver, and misc. analog) of 1.5W. Another concern exists with what happens to an undriven bus. An unbiased, undriven bus can float to an undetermined state. It is better to have a slightly biased bus than a High-Z biased bus.

The first section of this document determines the power consumption of a single driver with a pulldown for BUS- and a pullup for BUS+. The pullup current is called I1. The pulldown current is called I2. Ileak is the amount of current being injected into the bus by inactive drivers. Vasst is the asserted voltage between BUS+ and BUS- measured at the active driver. Ra is half the value of the upper and lower bias resistors on the terminator networks. Rb is half the value of the center resistor in the terminater network. 'n' is the number of drivers on the bus(note: only one driver, in the middle of the bus is active). Vt_min is the minimum Vterm potential allowed. Vt is the terminator voltage(i.e. Vterm). Vc is the IC power supply voltage. Rc is the series line resistance in one line for one quarter of the bus length. Vclear is the minimum driver clearence between the driver output and the IC power rail.

This analysis looks at i_limit different combinations of I2. NOTE: I1 is a function of Ra, Rb, Rc, I2, Vasst, and Vt. It also looks at nine different values of Ra: from 150, to 350 ohms. NOTE: Rb is a function of Ra and Zterm. Zterm is the desired termination impeadance and is fixed at 122 ohms. It has been previously determined that the worst case power consumption occurs when Vt is at its maximum value and Vc is at its maximum value. The values of I1 and I2 must be increased by K to overcome the worst case effects of bus leakage.

Calculate the value of Rc. 'ro' is the unit resistance (ohns/meter) of 28 guage copper wire at 70 degrees Celsius. L is the total length of the bus in meters.

ro := 0.2456 L := 25.0

$$Rc := ro \cdot \frac{L}{4}$$

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j_limit := 8
i_limit := 100
j := 0 ..j_limit
i := 0 ..i_limit
n := 16
Ileak := .00005
Zterm := 122.0
Ra_min := 150.0
Ra_inc := 25
Vt_min := 4.00
Vt := 5.25
Vc := 5.5
Vasst := 0.5
Vclear := 0.700
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Determine conductance values from resistance values.

$$Gc := \frac{1}{Rc}$$

Define the standard leakage value:

$$K := n \cdot Ileak$$

Determine the value of Ra for this interation:

$$Ra_j := Ra\_min + Ra\_inc \cdot j$$

$$Ga(ra) := \frac{1}{ra}$$

Determine the value of Rb from Ra and Zterm:

$$Rb(ra) := \frac{Zterm \cdot 2 \cdot ra}{4 \cdot ra - Zterm} \qquad Gb(ra) := \frac{1}{Rb(ra)}$$

Determine the point where I1 = I2 = Isym:

$$Isym(vasst,ra,vt) := \frac{vasst \cdot (2 \cdot ra + Rb(ra)) + vt \cdot Rb(ra)}{4 \cdot ra \cdot Rc + 2 \cdot ra \cdot Rb(ra) + 2 \cdot Rb(ra) \cdot Rc} + K$$

Now solve the system equation using determinants.

Define some common factors.

$$FAC1(ra,i2) := i2 - \frac{Vt}{ra} \qquad FAC2(i2) := i2 \cdot Rc - Vasst$$

$$GAB(ra) := Ga(ra) + Gb(ra) \qquad GAC(ra) := Ga(ra) + Gc$$

$$GBC(ra) := Gb(ra) + Gc \qquad GABC(ra) := Ga(ra) + Gb(ra) + Gc$$

$$SYS(ra) := \begin{bmatrix} (-1) \cdot GABC(ra) & Gb(ra) & Gc \\ Gb(ra) & (-1) \cdot GAB(ra) & 0 \\ 0 & 1 & -1 \end{bmatrix} \qquad VEC(ra,i2) := \begin{bmatrix} 0 \\ FAC1(ra,i2) \\ FAC2(i2) \end{bmatrix}$$

$$f(ra,i2) := SYS(ra)^{-1} \cdot VEC(ra,i2)$$

$$VP(ra,i2) := f(ra,i2)_0 \qquad VM(ra,i2) := f(ra,i2)_1 \qquad V1(ra,i2) := f(ra,i2)_2$$

VP is the nodal potential with respect to ground on BUS+ at terminator:
VM is the nodal potential with respect to ground on BUS- at terminator:
V1 is the nodal potential with respect to ground on BUS+ at the driver:

Determine the value of I1:

$$I1(ra,i2) := (V1(ra,i2) - VP(ra,i2)) \cdot Gc$$

Pp is the power dissapated by the BUS+ driver:

$$Pp(ra,i2) := (Vc - V1(ra,i2)) \cdot (I1(ra,i2) + K)$$

Pm is the power dissapated by the BUS- driver:

$$Pm(ra,i2) := (VM(ra,i2) - i2 \cdot Rc) \cdot (i2 + K)$$

Pchip is the amount of power dissapated by the IC.

$$Pchip(ra,i2) := Pp(ra,i2) + Pm(ra,i2)$$

Define I2 to go from 0 to 0.06.

$$I2_i := 0.06 \cdot \frac{i}{i\_limit}$$

Monitor the deasserted potential across Rb at the terminator and in the middle of the bus. In this case the worst case bus leakage would be in the same direction as the asserting bus drivers.

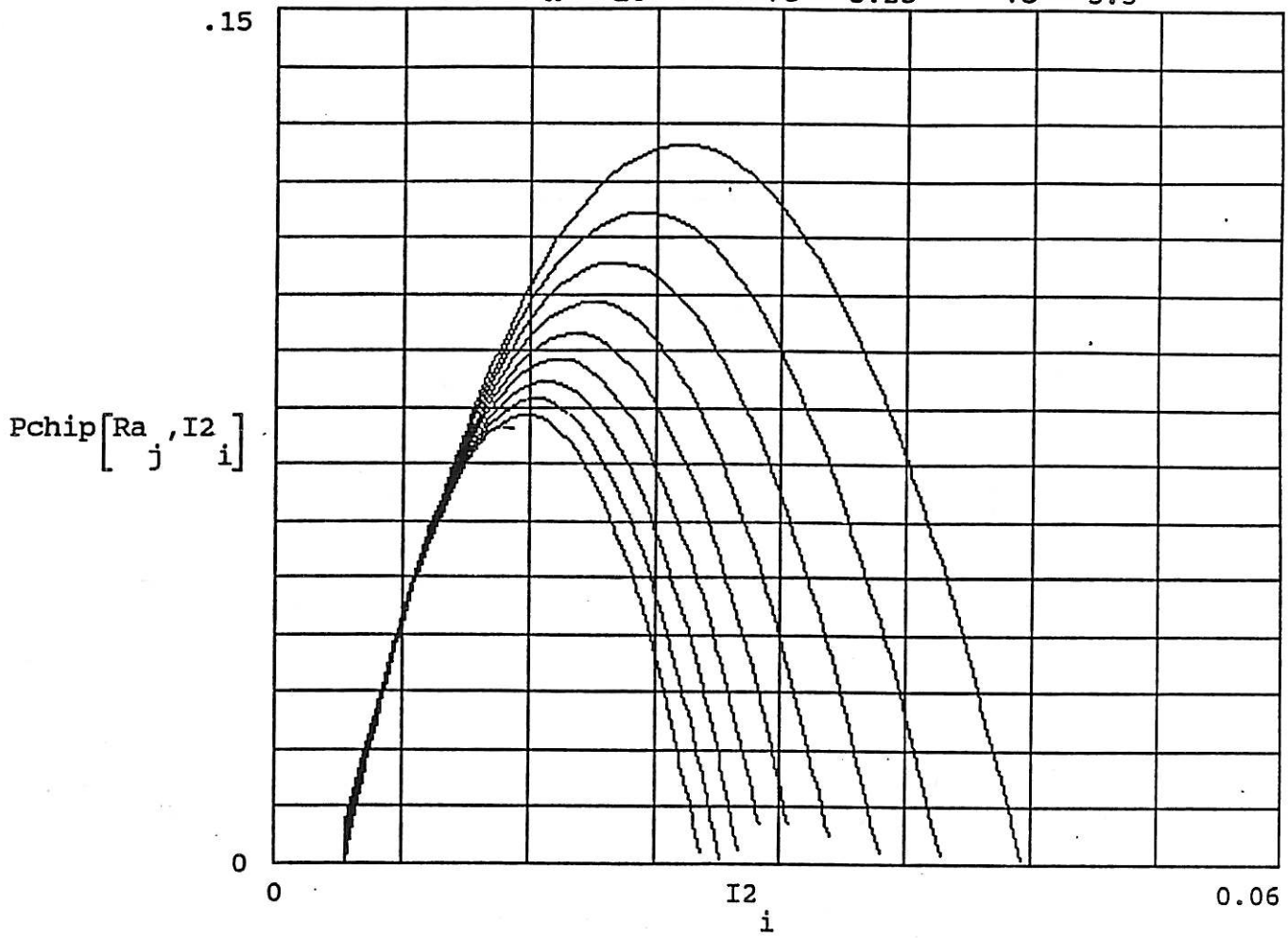
$$In(ra) := \frac{Vt\_min + K \cdot Rb(ra)}{2 \cdot ra + Rb(ra)}$$

$$Vdast(ra) := (K - In(ra)) \cdot Rb(ra)$$

$$Vdasd(ra) := 2 \cdot K \cdot Rc + (K - In(ra)) \cdot Rb(ra)$$

Vasst = 0.5 Rc = 1.535 Ileak = $5 \cdot 10^{-5}$

n = 16 Vt = 5.25 Vc = 5.5



Ra j
150
175
200
225
250
275
300
325
350

Rb[Ra j]
76.569
73.875
71.976
70.566
69.476
68.609
67.904
67.317
66.823

Vdasd[Ra j]
-0.7621
-0.6459
-0.5587
-0.491
-0.4367
-0.3924
-0.3554
-0.3241
-0.2973

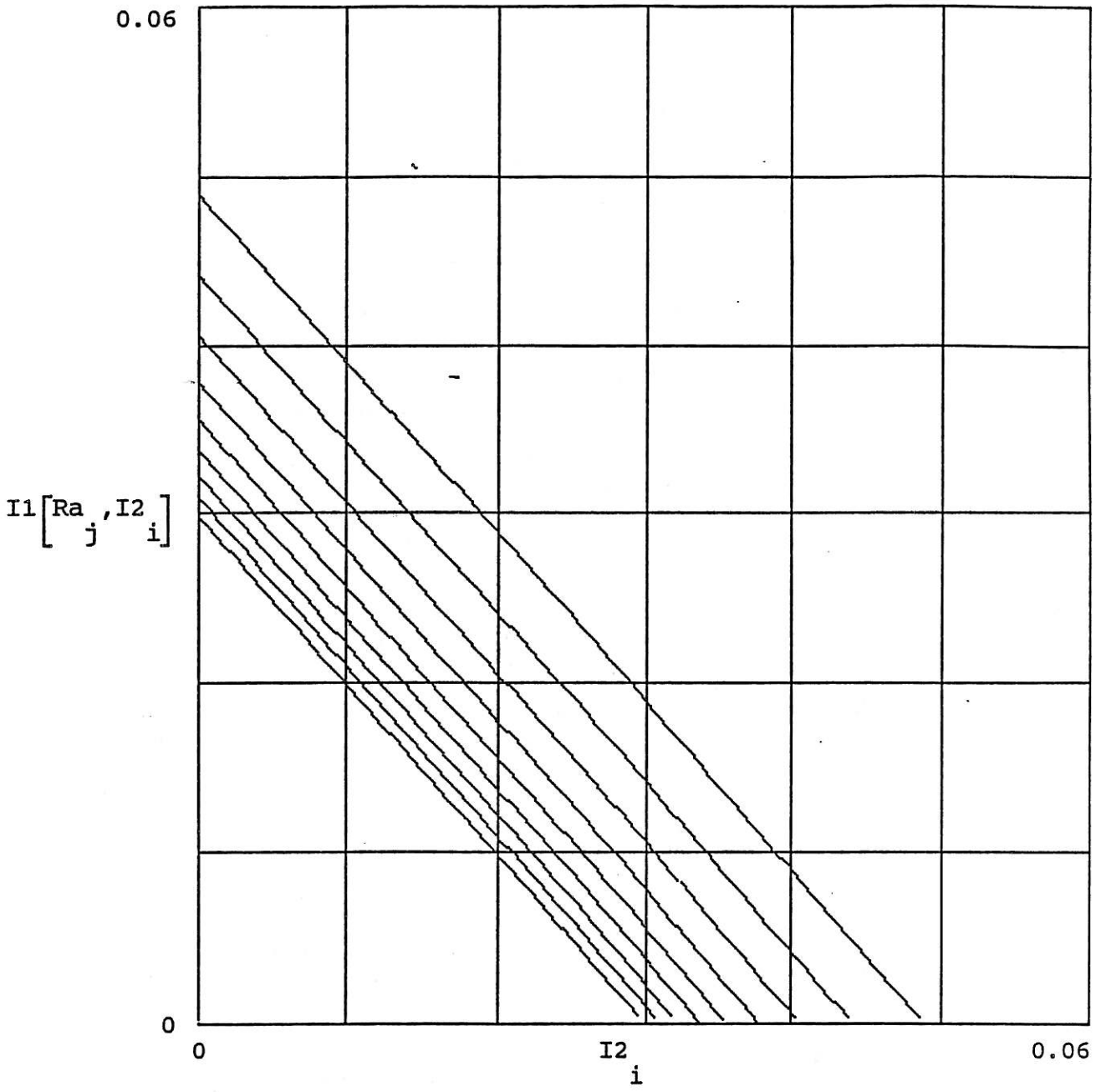
Vdast[Ra j]
-0.7645
-0.6483
-0.5612
-0.4934
-0.4392
-0.3948
-0.3579
-0.3266
-0.2998

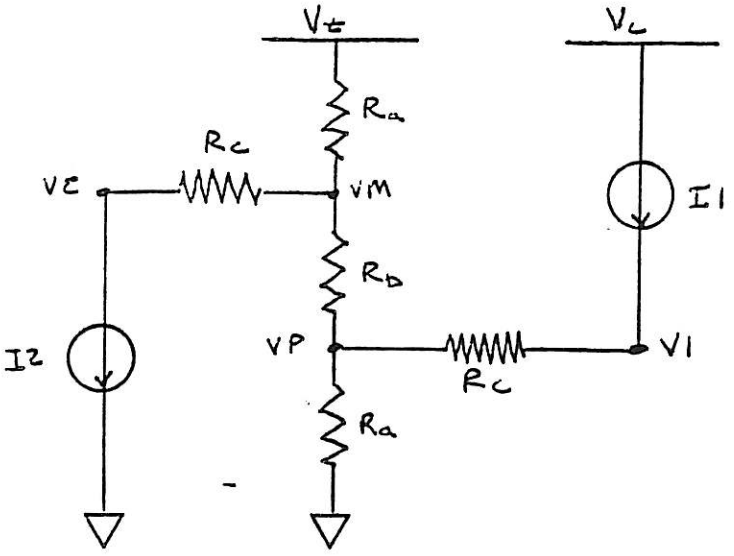
Ra j
150
175
200
225
250
275
300
325
350

Isym[Vasst, Ra_j, Vt]
0.02527
0.02289
0.0211
0.01971
0.0186
0.01769
0.01693
0.01629
0.01574

Pchip[Ra_j, Isym[Vasst, Ra_j, Vt]]
0.12593
0.114
0.10504
0.09807
0.09248
0.08791
0.08409
0.08085
0.07807

Define the relationship between I1 and I2:





$V_{assL} = VI - VZ$

FIGURE 1 - CIRCUIT USED FOR CALCULATING IC POWER COMSUMPTION

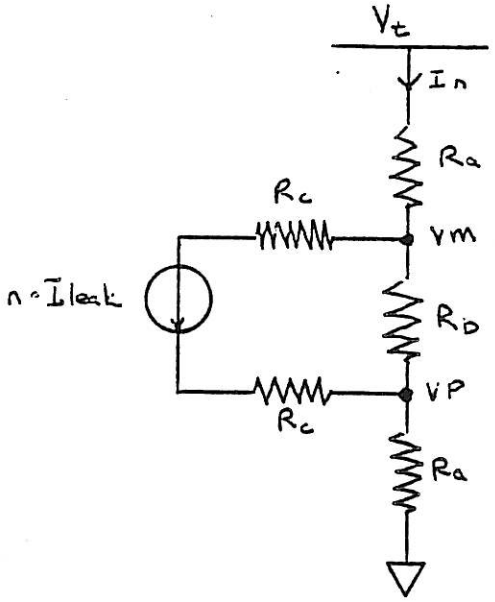


FIGURE 2 - CIRCUIT USED FOR CALCULATING MINIMUM DEASSERTION POTENTIAL