Date: November 15, 1990

To: John Lohmeyer, Senior Consulting Engineer
Location: E&M Wichita

From: Luke A. Perkins, Analog Design Engineer
Location: Microelectronic Products Division
Extension: 262 VP: 463-0262

Subject: Feasibility Of Totem Pole Termination for Low Power Differential SCSI

Attached is a document that examines the feasibility of using the old differential SCSI termination architecture for low power, high speed differential SCSI. It is possible to use the old architecture and consume only 1 Watt of power for the bus drivers. The following specifications would need to be imposed:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rterm</td>
<td>650/135/650 Ohms</td>
</tr>
<tr>
<td>VOD</td>
<td>0.5 Volts</td>
</tr>
<tr>
<td></td>
<td>0.2 Volts</td>
</tr>
<tr>
<td>VDD</td>
<td>4.5 - 5.5 Volts</td>
</tr>
<tr>
<td>Vterm</td>
<td>4.0 - 5.25 Volts</td>
</tr>
<tr>
<td>VOcmr</td>
<td>1.0 - 3.5 Volts</td>
</tr>
<tr>
<td>VICmr</td>
<td>0.0 - VDD Volts</td>
</tr>
</tbody>
</table>

In order to meet the speed requirements of 20MEG xps, the drivers should be totem pole but with only active assists in one direction and continuous drive in the other. These power figures are based upon only 13 drivers being active at once.

If you have any questions, please feel free to give me a call.

WORK: 719-596-5795 ext. 262
FAX: 719-597-8225
This document examines the feasibility of using the old differential SCSI architecture for low power, high speed differential SCSI. The dominant concern with this method is power consumption. IC driver power should be limited to a total (driver, receiver, and misc. analog) of 1.5W. Another concern exists with what happens to an undriven bus. An unbiased, undriven bus can float to an undetermined state. It is better to have a slightly biased bus than a High-Z biased bus.

The first section of this document determines the power consumption of a single driver with a pulldown for BUS- and a pullup for BUS+. The pulldown current is called I1. The pulldown current is called I2. Ileak is the amount of current being injected into the bus by inactive drivers. Vass is the asserted voltage between BUS+ and BUS- measured at the active driver. Ra is half the value of the upper and lower bias resistors on the terminator networks. Rb is half the value of the center resistor in the terminator network. 'n' is the number of drivers on the bus (note: only one driver, in the middle of the bus is active). Vt_min is the minimum Vterm potential allowed. Vt is the terminator voltage (i.e. Vterm). Vc is the IC power supply voltage. Rc is the series line resistance in one line for one quarter of the bus length. Vclear is the minimum driver clearance between the driver output and the IC power rail.

This analysis looks at I2 limit different combinations of I2. NOTE: I1 is a function of Ra, Rb, Rc, I2, Vass, and Vt. It also looks at nine different values of Ra: from 150, to 350 ohms. NOTE: Rb is a function of Ra and Zterm. Zterm is the desired termination impedance and is fixed at 122 ohms. It has been previously determined that the worst case power consumption occurs when Vt is at its maximum value and Vc is at its maximum value. The values of I1 and I2 must be increased by K to overcome the worst case effects of bus leakage.

Calculate the value of Rc. 'ro' is the unit resistance (ohms/meter) of 28 guage copper wire at 70 degrees Celsius. L is the total length of the bus in meters.

\[
\begin{align*}
ro & := 0.2456 \\
L & := 25.0 \\
L \div Rc & := ro \div 4 \\
\text{j-limit} & := 8 \\
\text{i-limit} & := 100 \\
j & := 0 .. \text{j-limit} \\
i & := 0 .. \text{i-limit} \\
n & := 16 \\
Ileak & := .00005 \\
Zterm & := 122.0 \\
Ra_{\text{min}} & := 150.0 \\
Ra_{\text{inc}} & := 25 \\
Vt_{\text{min}} & := 4.00 \\
Vt & := 5.25 \\
Vc & := 5.5 \\
Vass & := 0.5 \\
Vclear & := 0.700
\end{align*}
\]

Determine conductance values from resistance values.

\[
Gc := \frac{1}{Rc}
\]
Define the standard leakage value:

\[ K := n \cdot I_{\text{leak}} \]

Determine the value of \( Ra \) for this iteration:

\[ Ra := Ra_{\text{min}} + Ra_{\text{inc}} \cdot j \]

\[ j \]

\[ G_a(ra) := \frac{1}{ra} \]

Determine the value of \( R_b \) from \( Ra \) and \( Z_{\text{term}} \):

\[ R_b(ra) := \frac{Z_{\text{term}} \cdot 2 \cdot ra}{4 \cdot ra - Z_{\text{term}}} \]

\[ G_b(ra) := \frac{1}{R_b(ra)} \]

Determine the point where \( I_1 = I_2 = I_{\text{sym}} \):

\[ I_{\text{sym}}(\text{vasst},ra,vt) := \frac{\text{vasst} \cdot (2 \cdot ra + R_b(ra)) + vt \cdot R_b(ra)}{4 \cdot ra \cdot R_c + 2 \cdot ra \cdot R_b(ra) + 2 \cdot R_b(ra) \cdot R_c} + K \]

Now solve the system equation using determinants.

Define some common factors.

\[ \text{FAC1}(ra,i2) := i_2 - \frac{\text{Vt}}{ra} \]

\[ \text{FAC2}(i2) := i_2 \cdot R_c - \text{Vasst} \]

\[ G_{\text{ab}}(ra) := G_a(ra) + G_b(ra) \]

\[ G_{\text{ac}}(ra) := G_a(ra) + G_c \]

\[ G_{\text{bc}}(ra) := G_b(ra) + G_c \]

\[ G_{\text{abc}}(ra) := G_a(ra) + G_b(ra) + G_c \]

\[ \text{SYS}(ra) := \begin{bmatrix} (-1) \cdot G_{\text{abc}}(ra) & G_b(ra) & G_c \\ 0 & (-1) \cdot G_{\text{abc}}(ra) & 0 \\ 0 & 0 & 1 \end{bmatrix} \]

\[ \text{VEC}(ra,i2) := \begin{bmatrix} 0 \\ \text{FAC1}(ra,i2) \\ \text{FAC2}(i2) \end{bmatrix} \]

\[ f(ra,i2) := \text{SYS}(ra) \cdot \text{VEC}(ra,i2) \]

\[ \text{VP}(ra,i2) := f(ra,i2) \]

\[ \text{VM}(ra,i2) := f(ra,i2) \]

\[ \text{V1}(ra,i2) := f(ra,i2) \]

\[ \text{VP} \text{ is the nodal potential with respect to ground on BUS+ at terminator:} \]

\[ \text{VM} \text{ is the nodal potential with respect to ground on BUS- at terminator:} \]

\[ \text{V1} \text{ is the nodal potential with respect to ground on BUS+ at the driver:} \]

Determine the value of \( I_1 \):

\[ I_1(ra,i2) := (\text{V1}(ra,i2) - \text{VP}(ra,i2)) \cdot G_c \]
Pp is the power dissipated by the BUS+ driver:

\[ Pp(ra,i2) := (Vc - V1(ra,i2)) \cdot (I1(ra,i2) + K) \]

Pm is the power dissipated by the BUS- driver:

\[ Pm(ra,i2) := (VM(ra,i2) - i2 \cdot Rc) \cdot (i2 + K) \]

Pchip is the amount of power dissipated by the IC:

\[ Pchip(ra,i2) := Pp(ra,i2) + Pm(ra,i2) \]

Define I2 to go from 0 to 0.06.

\[ I2 := 0.06 \cdot \frac{i}{i \text{ _limit}} \]

Monitor the deasserted potential across Rb at the terminator and in the middle of the bus. In this case the worst case bus leakage would be in the same direction as the asserting bus drivers.

\[ In(ra) := \frac{Vt_{min} + K \cdot Rb(ra)}{2 \cdot ra + Rb(ra)} \]

\[ Vdast(ra) := (K - In(ra)) \cdot Rb(ra) \]

\[ Vdasd(ra) := 2 \cdot K \cdot Rc + (K - In(ra)) \cdot Rb(ra) \]
Define the relationship between $I_1$ and $I_2$: 

[Graph showing the relationship between $I_1$ and $I_2$]
\[ V_{\text{assert}} = V_1 - V_2 \]

**Figure 1 - Circuit Used for Calculating IC Power Consumption**

**Figure 2 - Circuit Used for Calculating Minimum Deassertion Potential**