Date: November 5, 1990

To: X3T9.2 Membership
From: Erik Jessen, Larry Lamers, and John Lohmeyer

Subject: October 29, 1990 Low-Power Differential Working Group Meeting

John Lohmeyer called this meeting to order at 2:30 p.m., Monday, October 29, 1990. Chuck Micalizzi was unavailable to chair this meeting due to airline problems. Erik, Larry, and John agreed to keep the minutes.

The following people attended the meeting:

Name	Status	Organization
Mr. Robert C. Herron	A	3M Company
Mr. Doug Makishima	S	Adaptec, Inc.
Mr. Robert Otis	A	Apple Computer
Mr. Robert Liu	P	Fujitsu America, Inc.
Mr. Kurt Chan	P	Hewlett Packard Co.
Mr. Mike Peper	A	Hewlett Packard Co.
Mr. Howard Wang	O	Hitachi
Mr. Roger Dimmick	V	IBM Corp.
Mr. Lawrence J. Lamers	P	Maxtor Corp.
Mr. Ken Erickson	O	Micropolis Corp.
Mr. Gary Murdock	A	National Semiconductor
Mr. Don Chin	V	National Semiconductor
Mr. Thai Nguyen	V	National Semiconductor
Mr. John Lohmeyer	P	NCR Corp.
Mr. Luke A. Perkins	S	NCR Corp.
Mr. Thomas R. Marks	P	NEK/Helix Cable, Inc.
Mr. James McGrath	O	Quantum Corp.
Mr. Edward R. Schurig	O	Texas Instruments
Mr. Kevin Gingerich	V	Texas Instruments
Mr. Mike Bartlett	V	Texas Instruments
Mr. Arlan P. Stone	A	UNISYS
Mr. Erik Jessen	O	Western Digital

22 People Present

Status Key: P Principal
A Alternate
O Observer
S Special Interest (frequent visitor)
V Visitor

RESULTS OF MEETING

Plenary Guidance

John Lohmeyer started the meeting by presenting the foils from the Ft. Lauderdale X3T9.2 plenary meeting giving the plenary's opinion on the requirements and goals for the low-power differential working group. (Please refer to item 8.6 in 90-163 for this information.)

The key point was that the plenary group placed a higher value on interoperability with old devices than the low-power differential group had at its September meeting. John stated that his view of interoperability did not require new devices to drive the old terminator, but it was essential for old differential devices to operate on the new differential bus.

SPICE Results

Mike Bartlett presented his SPICE results:

	min	max	
TRANSMITTER			
Voc	2.0	3.0	V
Ios (Vo = 5V)	---	100	mA
Ios (Vo = 0V)	---	-100	mA
Tskew (LIM)	---	7.5	ns
Vod (RL = 60 ohms)	0.5	0.8	V
Voh	---	4.0	V
Vol	1.0	---	V
RECEIVER			
Vih	---	5.0	V
Vil	0.0	---	V
Ii	-50	+50	uA
Vth		200	mV
Vtl	-200		mV
Vhys	35		mV
Ri	12		k-ohm
Ci		25	pF
Tskew (LIM)		7.5	ns

Tskew is the skew between the fastest and slowest signals in the cable.

This provides 1V of common-mode shift on the cable. 8-bit power consumption was 1.25W, and 16-bit power was 1.75W. The cable was terminated with a single 120-ohm resistor; each input receiver had a built-in bias replacing the existing bias provided by the three resistor termination used currently. He stated it should be possible to add new transceivers to old systems but not vice-versa.

Termination

There was a discussion about changing the values of the existing termination resistors to reduce power consumption. Mike did think that changing the

resistors would help to reduce power consumption to 1.75W for 8-bit and 2.58W for 16-bit; however, the power is still too great for a single package. Luke Perkins believed that the resistors could be tuned further than Mike had gone, and power could be reduced to the level that one package could contain a complete controller (no more than 1.2W). He is going to model it and bring the results to the next meeting.

It was pointed out that low-power differential would have at least as much ESD and over-voltage protection as single-ended does today. Control of common-mode voltage shifts is a system design function, and a system designer must meet the requirements to be able to use low-power differential.

Gary Murdock stated that the leakage current should be 50 uamps maximum (this is reflected in the earlier table of results presented by Mike). He also asked about the pulse width distortion at 200mv when switching with fast transfer rates. Mike Bartlett responded that we are trading sensitivity for speed. If less than 200mv the receiver slows down. This is very tough in CMOS.

Common-Mode Noise

The question of what is the actual AC common-mode noise encountered in real systems was not answered. It was pointed out the the answer should be measured in power, not voltage or current. The working group is still looking for systems integrators that can provide a model and/or actual numbers on common-mode noise.

John Lohmeyer said a single-ended specification on the part that ties down common-mode tolerance is useful. Such a specification was lacking in RS-485 and it resulted in some problems for the SCSI usage of these parts. He also requested that the set of rules for mixing and matching new and old devices be developed. (This is reflected in the table.)

A comment was made to the effect that increasing signaling rate would not increase power consumption proportionally. Thus a fast signaling protocol would be superior to a wider bus for obtaining a given transfer rate.

Packaging

It was pointed out that higher power consumption in a single part was possible; however, air flow was required across the device, which is a function of system design. As a result, SCSI controller designers were forced to assume the worst-case (still air situation) when calculating power dissipation.

SPICE Results for Maximum Transfer Rates

Mike Bartlett said that he would bring his results for 20MT/s to the January meeting.

Hot Plugging

Roger Dimmick (IBM) presented his definitions and requirements for hot plugging, live plugging, and concurrent maintenance. This completed his

action item from the previous meeting. Larry Lamers re-keyed the information from Roger's foils in document 90-178.

Proposed New Differential Pin Outs

Gary Murdock proposed that the P, Q, and L cable pinouts be changed on differential for compatibility with single-ended devices (see 90-177). The proposal also added a DIFFSENS2 line to check for low-power differential. Smart transceivers could switch from single-ended to low-power differential based on DIFFSENS2. The purpose of this proposal is to provide an upgrade path to get low-power differential accepted, make it interoperable with single-ended implementations, and allow manufacturers to build one device for both signal types.

Assuming electrical compatibility with old differential devices is achieved, then devices following this proposal could interoperate with old differential devices by using a "gender-bender" device to map the pins.

Self-Adjusting Maximum Signaling Rates

Gary Murdock proposed that the design should not be based on an all worst-case scenario. Rather an automatic throttle should adjust transfer speed if the bus has a high error rate. He noted that many high-speed modems employ a similar "fall-back" technique. Since SCSI error rates must be significantly higher than the modem rates, the time to accurately measure the error rate is longer. No one was sure how to measure the error rate in a reasonable period, but it is an interesting idea.

Action Items

1. Power Analysis using three resistor approach - Luke Perkins
2. Look at higher speed options - Mike Bartlett
3. Compatible with existing differential - Mike Bartlett
4. Are bias resistors needed and what happens if they are not there - Mike Bartlett

Agenda for January 1991 Meeting

1. Spice of > 10 Megatransfers per second
2. Review proposals

Next Meeting

The next working group meeting is being hosted by Ken Post of Future Domain at (see document 90-158):

Red Lion Hotel
3050 Bristol Court
Costa Mesa, CA 92626-3098
TEL: 714-540-7000 FAX: 714-540-9176
THE RESERVATION CUTOFF DATE IS DECEMBER 27, 1990.

The Low-Power Differential Working Group Meeting will begin at 1:00 p.m. on Monday January 14, 1991.

TRANSCEIVER REQUIREMENTS

	Min.	Max.	units
RECEIVER			
VTH		200.0	mV
VTL	-200.0		mV
Vhys	35.0		mV
ri	12.0		k Ohms
ci		25.0	pF
t skew(LIM)		7.5	ns
DRIVER			
|VOD| (RL=60 Ohms)	0.5		V
VOC	2.0	3.0	V
Ios (Vo=5V)		100.0	mA
Ios (Vo=0V)		-100.0	mA
t skew(LIM)		7.5	ns
V_{OH} (max)		4.0	V
V_{OL}	1.0		V
I_I	-50	+50	μA

MBB 03-752 10/29/90

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POWER ANALYSIS
PRESENT SCSI TERMINATION

	POWER (mW)	8 BIT CHANNELS	8 BIT POWER (mW)	16 BIT CHANNELS	16 BIT POWER (mW)
DRIVER OUTPUT	85.0	14	1,197.0	23	1,966.5
DRIVER DC	0.5	14	7.7	23	12.6
DRIVER AC	5.5	9	49.5	18	99.0
RECEIVER	27.0	5	137.5	5	137.5
CONTROLLER DC	165.0	1	165.0	1	165.0
CONTROLLER AC	200.0	1	200.0	1	200.0
TOTAL			1,757.0		2,581.0

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POWER ANALYSIS
PROPOSED NEW TERMINATION

	POWER (mW)	8 BIT CHANNELS	8 BIT POWER (mW)	16 BIT CHANNELS	16 BIT POWER (mW)
DRIVER OUTPUT	49.0	14	695.8	23	1,143.1
DRIVER DC	0.5	14	7.7	23	12.6
DRIVER AC	5.5	9	49.5	18	99.0
RECEIVER	27.0	5	137.5	5	137.5
CONTROLLER DC	165.0	1	165.0	1	165.0
CONTROLLER AC	200.0	1	200.0	1	200.0
TOTAL			1,256.0		1,757.0

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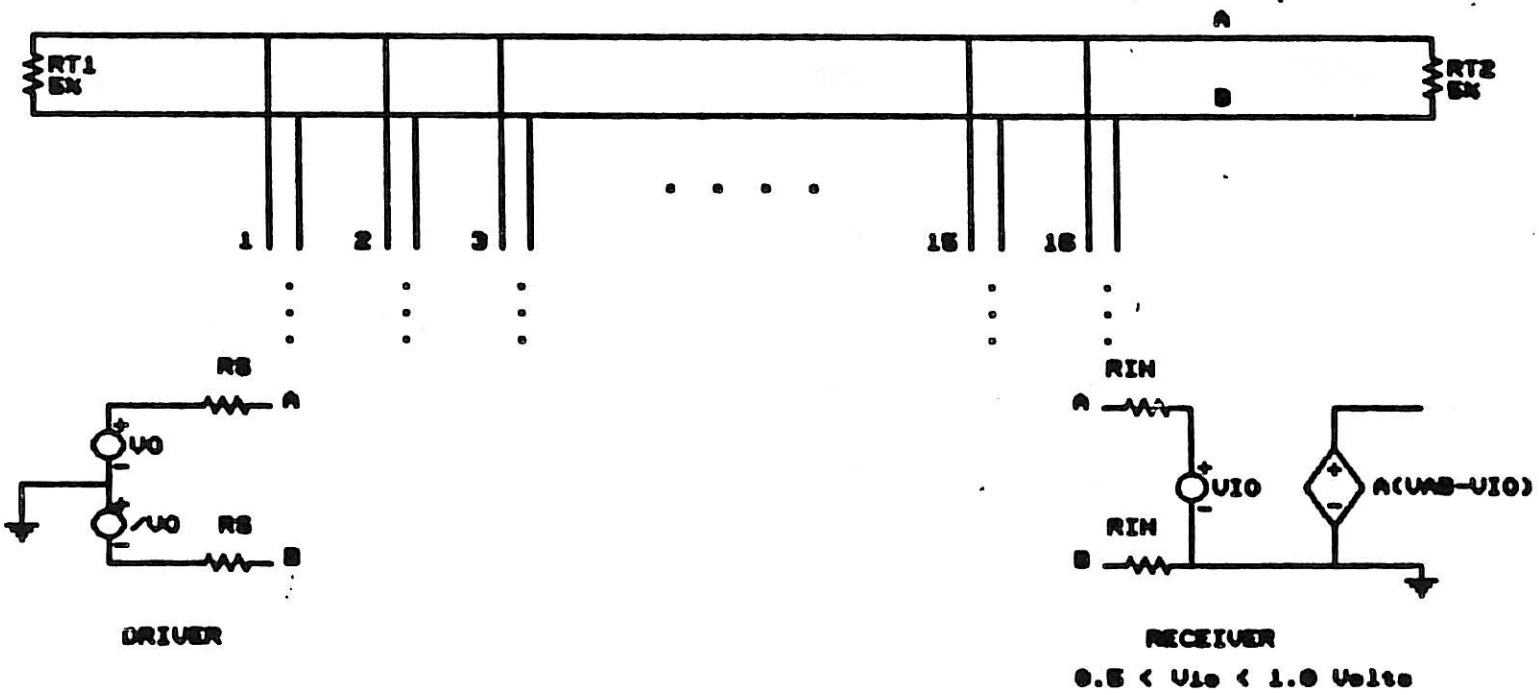
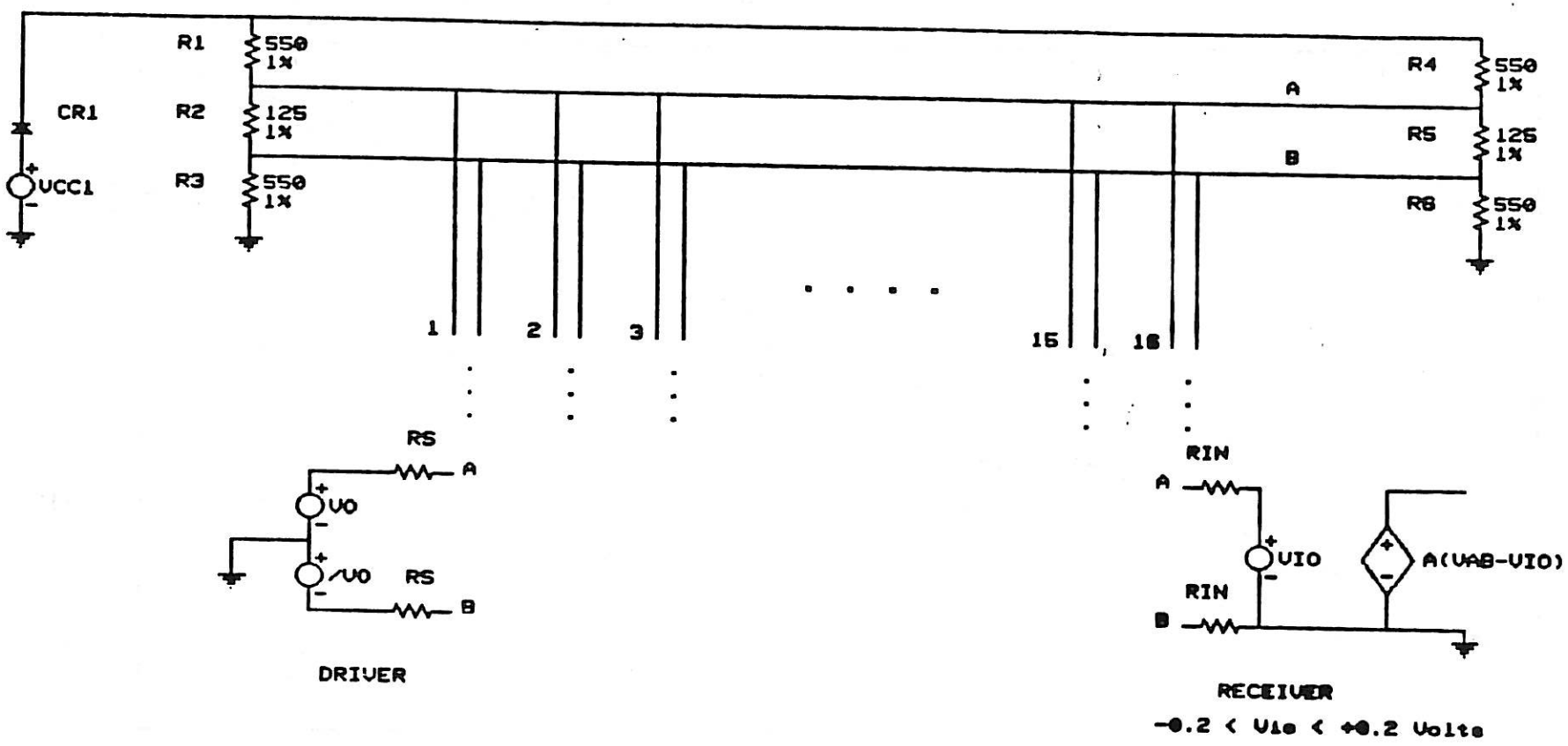


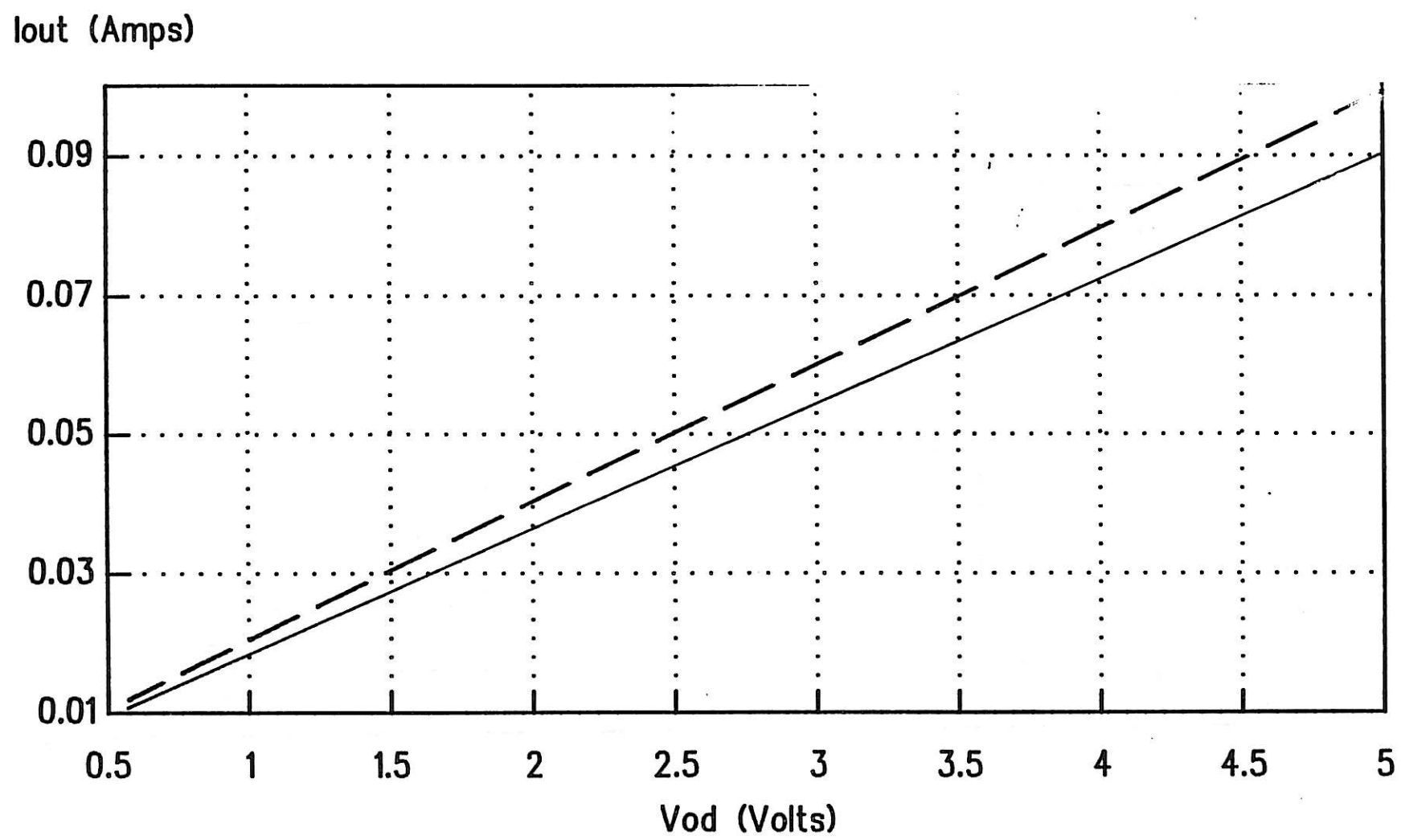
Internal Vio termination DC equivalent schematic.
(METHOD B)



External termination DC equivalent schematic.
(METHOD A)

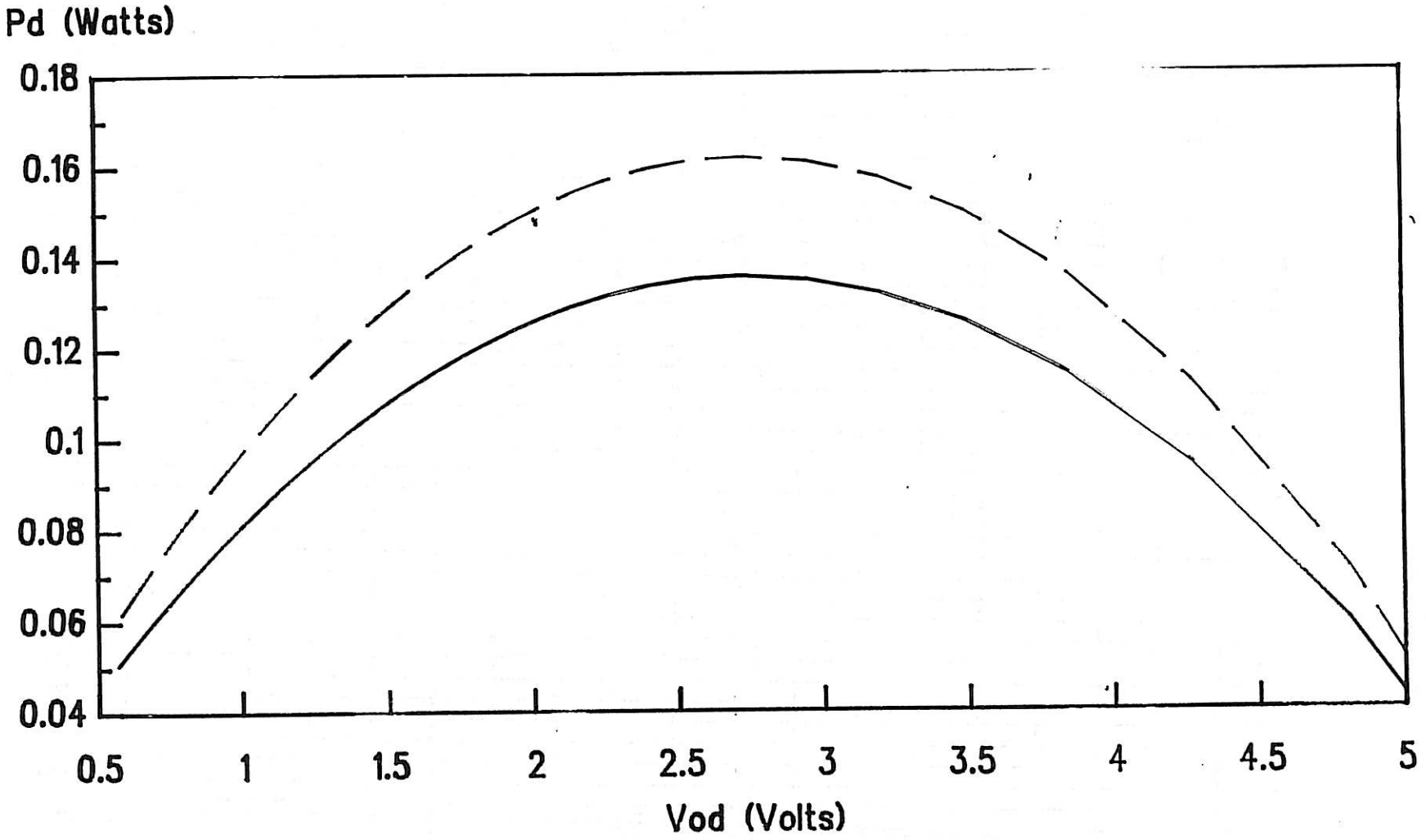
MAXIMUM Iout vs Vod

Internal Vio — "New" Old method - - -



MAXIMUM PER CHANNEL DC LOSSES vs Vod

Internal Vio "New" Old method



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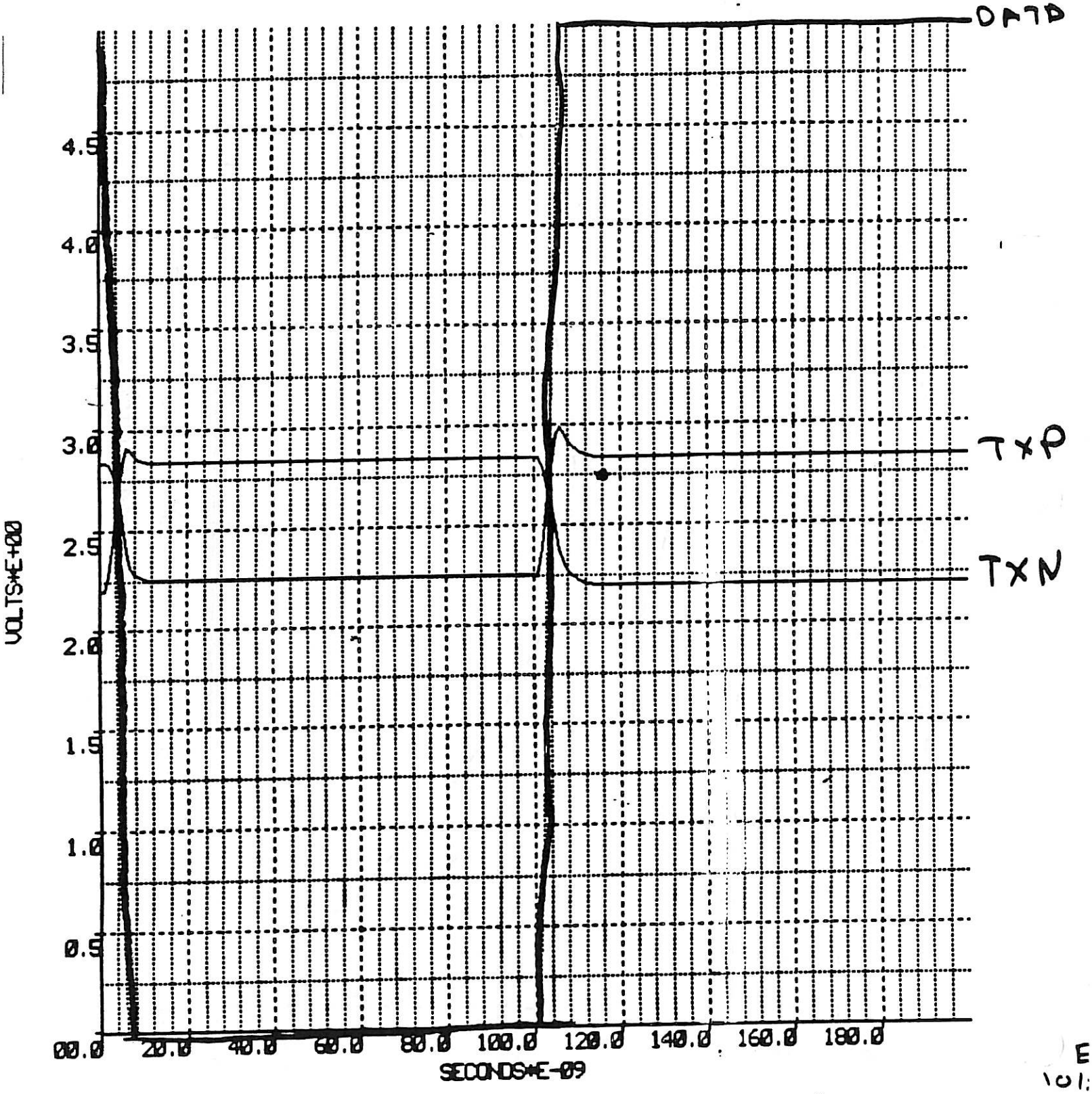
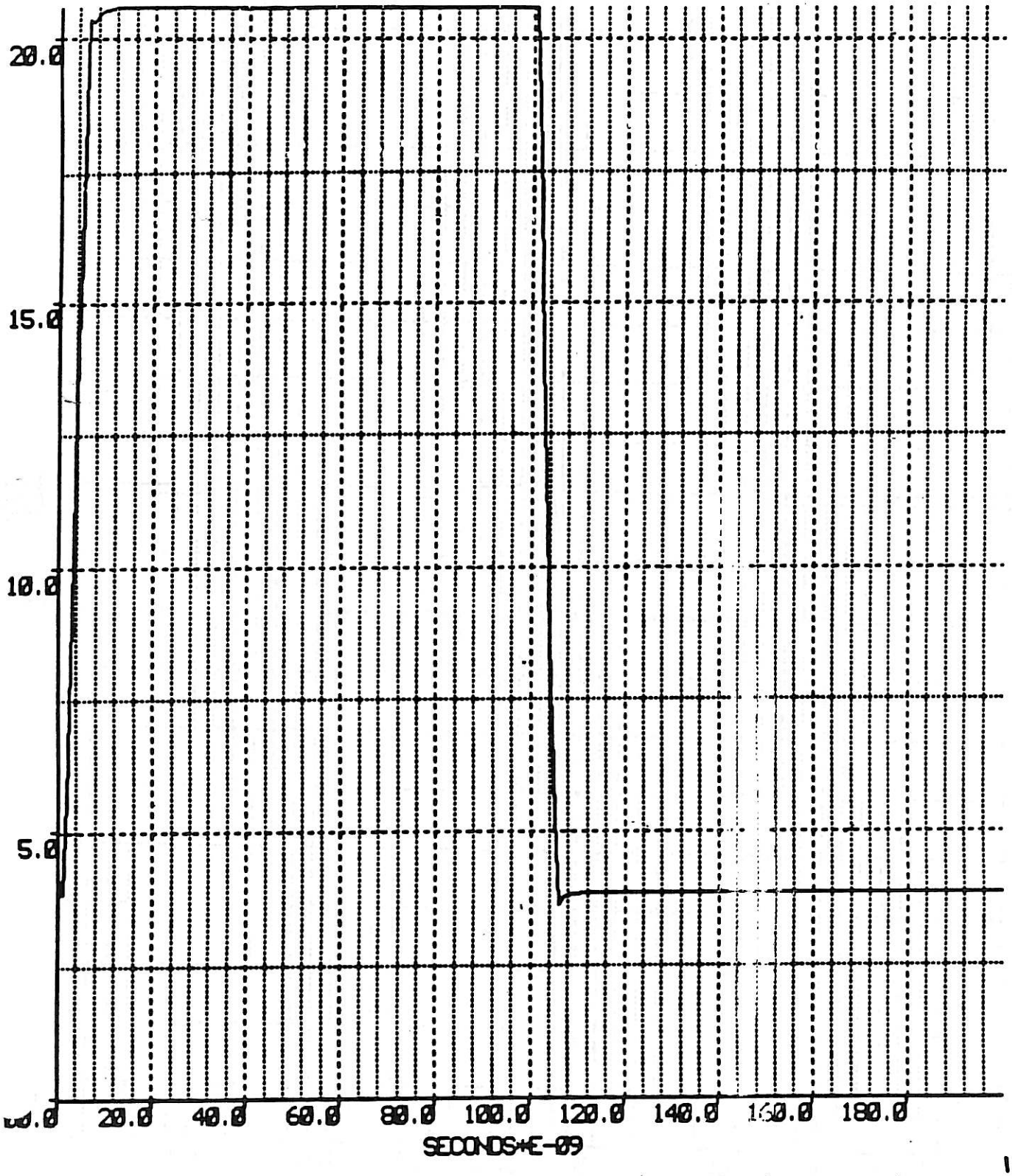
SCSI Driver
Config A



Worst case I_{cc}

Config A

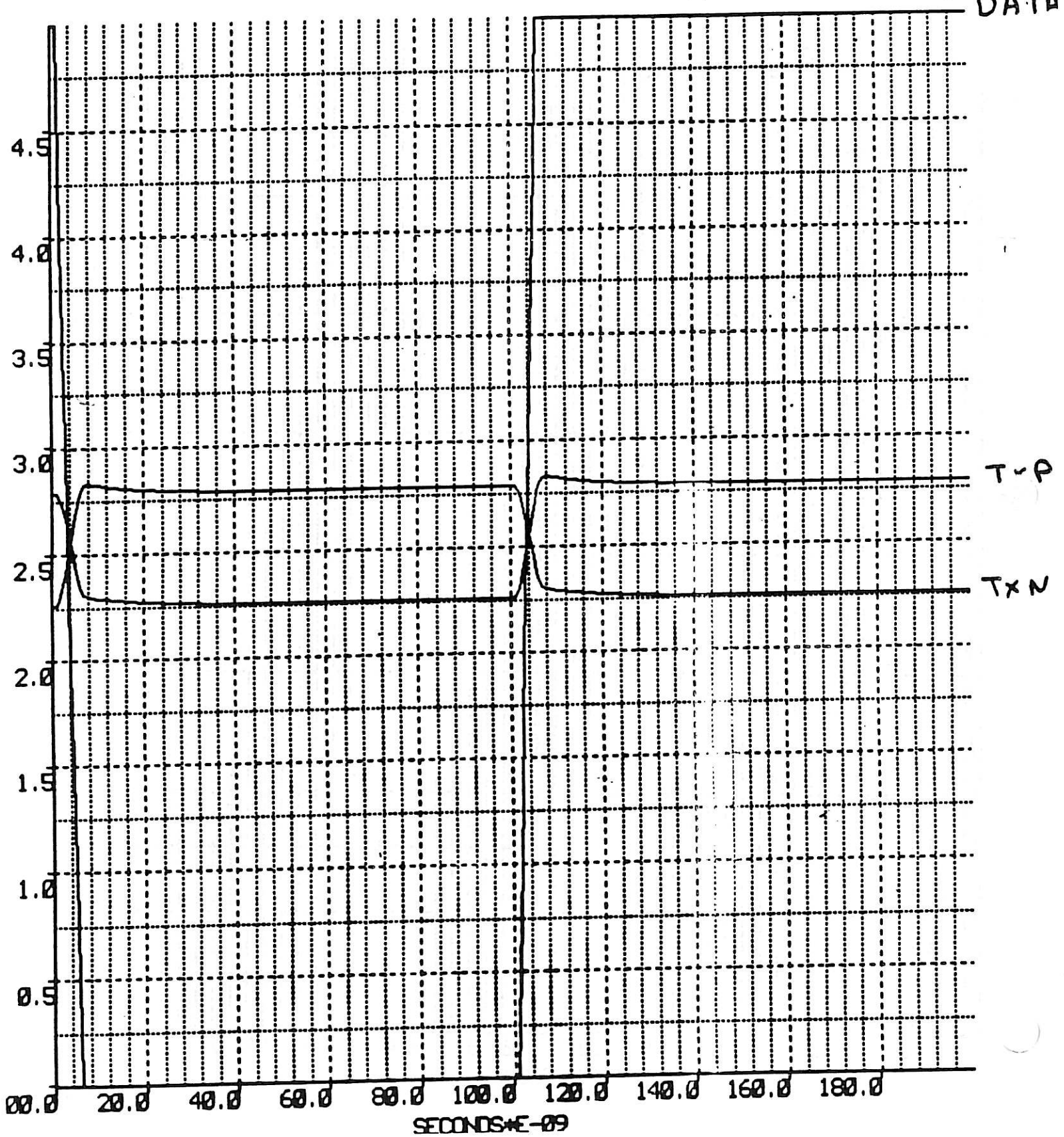


ECS
10/26/90

SCSI DRIVER

Configuration B

Nominal Conditions



worst case I_{CC}

Config B.