TEXAS INSTRUMENTS

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MEMORANDUM -- 31 Aug 1990

TO: John Lohmeyer, Chairman, X3T9.2

FROM: Bill Spence, TI

SUBJECT: S/E Cable Best-Case Analysis

Rev 0 presented the analysis for the first upward step which a signal on a single-ended (S/E) SCSI bus conductor makes after deassertion (release) of the signal. Rev 1 extends the analysis to the second step, which is the controlling step if one of a device pair is at the end of the SCSI bus.

THE BOTTOM LINE:

1. Compared to most practical implementations using the unregulated 132-ohm terminator, the use of the regulated 110-ohm terminator adds margin equivalent to an improvement in line impedance of 15 ohms or more.

2. In systems using the unregulated 132-ohm single-ended (S/E) terminator, only with a termpower voltage of 4.65 volts or more and a S/E cable impedance of 90 ohms or more is there any theoretical noise margin provided at the first step.

3. In systems with more than 1 device on the interior reach of the bus, improved noise margin results if the initiator(s) is at an end(s) of the bus.

Following up on our new insights into one of the most critical vulnerabilities of single-ended cable operation, I've made the following analysis of the best performance which can be expected in the signal steps which follow release of a single-ended (S/E) SCSI bus conductor. It is in the duration of these steps that a REQ or ACK line is most vulnerable to a false transition. Wave-front degredation, line losses, cross-talk, etc, can further REDUCE the margin of the signal above the receiver threshold; nothing can IMPROVE the margin above the limit set by the line current and the line impedance. In other words, the Vs figures shown below establish the best-case margins for various configurations; real-life cable performance will provide lower margins.

This analysis is similar to one which Kurt Chan didn't publish, but it is carried farther and the results are presented differently. NOTE: It has been pointed out to me that Kurt, along with Paul Boulay and Jim Schussler, did publish a lot of useful work in the May 10th issue of Electronic Design. It gives essentially the same formula for Vs1, does not quantitatively address Vs2. Their conclusions emphasize these same points: Keeping the line current and impedance, and thus the step voltages, high is essential to good operation.

The analysis is simple. Although the results are similar for any bus configuration, the simplest case to analyze is a bus conductor held low (asserted) in the center of the bus. Then, by symmetry, it is adequate to examine the behavior of one half of the bus only.

The following analysis presumes a bus conductor of S/E impedance R with a terminator network at one end and a driver/receiver at the other. The terminator network has an open circuit voltage of Voc and a source resistance of Ro and is powered from the TERMPWR conductor with a voltage of Vtp. It is assumed that with the driver holding the line down at Vol = 0.4 v, a current I is established in the line. Then the driver releases the line. In idealized analysis, the line at the driver/receiver will instantly experience a voltage increment of RI.* This increment added to the Vol produces what I call Vs1. Vs1 will persist for the time required for a signal roundtrip to the other end of the line and back, after which the voltage will proceed toward Voc in increasingly smaller steps, as illustrated in Kurt Chan's paper 90-93.

When the the signal wavefront reaches a terminator at a bus end which is of higher impedance than the line (almost always the case with shielded twisted-pair cables), the signal instantaneously increases by an additional increment to what I call Vs2, and a signal wavefront of this magnitude propagates back along the cable. This increment from Vs1 to Vs2 arises from the continuing infeed of current from the terminator at that end and is given by

$$\triangle Vs = (Voc - Vs1)R \;/\; (Ro + R).**$$

For the most general case--neither device in a data transfer at an end of the bus--the noise margin is only that provided by Vs1. If either device is at an end of the bus, then the noise margin available is that provided by Vs2. A signal received at an end of the bus instantaneously increments to the Vs2 level. A signal originating at an end of the bus, having the benefit of the continuing current infeed from the terminator there, starts out at Vs2.

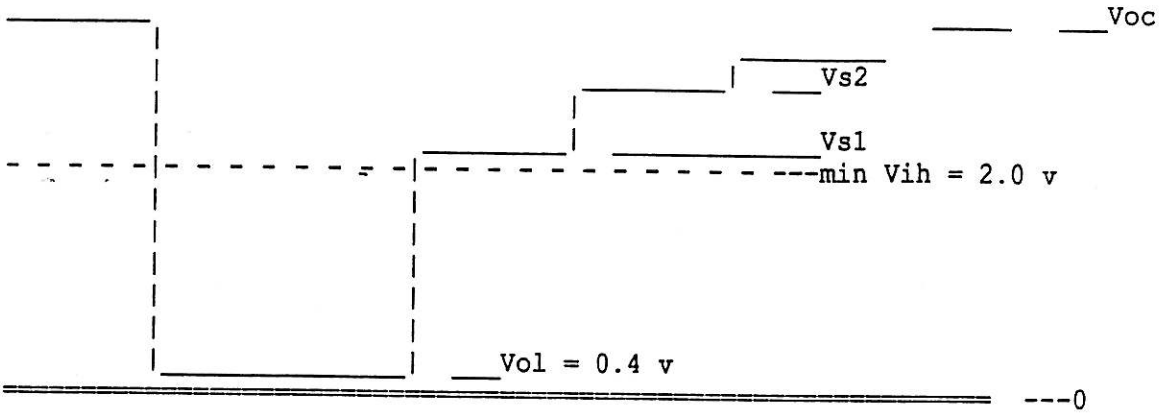
To be "legal," a Vs must be at or above the min Vih = 2.0 v prescribed in the standard. If a Vs is not above 2.0 v, there is zero "legal" or "theoretical" noise margin provided, and the system runs on the margin between the Vs and the actual upper threshold voltage of the particular chip doing the receiving. In any case, the higher a Vs is, the more noise margin is available. A design minimum of 2.4 volts would be desirable.

The width of a Vs can be calculated as (distance to the terminator) x (2 / V). With velocities (V) being about 0.2 m/ns (time delays being about 1.5 ns/ft), the maximum width Vs experienced is about as follows:

Total length:	1 m (3.3')	6 m (20')	20 m (66')
Vs width:	10 ns	60 ns	200 ns

The narrower the Vs, the less the exposure. Double-clocking of REQ- or ACK- becomes progressively less possible as exposure times fall below 100 ns, at least in the older SCSI chips. This may point to a key reason why the empirical limit of 6 m was set for S/E SCSI.

The following figure of voltage vs time at the driver illustrates the concepts involved.



The following table gives Vs1 & Vs2 for various cable S/E impedances and values of line current, as controlled by the terminator style and bus configuration. Three cable impedances are presented: our presently established simple-minded 90 ohms from SCSI-2, a kind of median 79 ohms for good S/E cables, and a 68 ohm figure close to the minimum values reported in all the testing to date.

					Vs1/Vs2		
Case	Vtp	Voc	Ro	I	R=90	R=79	R=68
A				22.4	2.42/2.61	2.17/2.45	#1.92/2.28
B		2.85	110	22.3	2.41/2.60	2.16/2.45	#1.91/2.27
C	4.7	2.82	132	18.3	2.05/2.40	#1.85/2.25	#1.65/2.10
D	4.25	2.55	132	16.3	#1.87/2.17	#1.69/2.05	#1.51/1.91#

- below the "legal" minimum of 2.0 v.

Case A: The legal best: the maximum legal current from the terminator is 22.4 ma, so this case represents the highest Vstep legally possible.

Case B: The regulated 110-ohm terminator, designed by Paul Boulay to establish essentially the maximum legal current and thus the maximum Vstep.

Case C: The nominal best with the 132-ohm terminator: A Vcc of 5.0 v is dropped to 4.7 v by the Schottky diode. The divider drops the Voc to 330/550 times the Vtp. The high source resistance of 132 ohms then holds the current down and thus lowers Vs by a major amount.

Case D: "Worst" best case with the 132-ohm terminator: Vtp is at the "legal" minimum of 4.25 v. No Vs1 reaches the "legally" required 2.0 v.

* The transmission line analysis I know of is based on presumptions about the physical system which are not satisfied by a bundle of twisted pairs, one conductor of each pair and an overall shield grounded, and the intervening space a jumble of air and some dielectric. Thus the concept of characteristic impedance may be only an approximation. Nonetheless, for the purpose of SCSI cable analysis, the instantaneous $\Delta v/\Delta i$ definition is in my opinion the most useful. NOTE: different cable constructions yield amazingly different performance as transmission lines, as illustrated in my submissions 89-148 and 90-124. Some bundled twisted-pair cables perform very well.

** The ΔVs between Vs1 and Vs2 is given by $R\Delta i$, where Δi is given by (Voc - Vs2)/Ro, or (Voc - (Vs1 + ΔVs))/Ro,
i.e., ΔVs = (Voc - Vs1 - ΔVs)/Ro. Solving for ΔVs gives the equation above.