SERIALIZED DATA COMM.

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Outline

- Serial Data Communication Background
- AMD's Serial Data Communication Solutions (TAXIchips)
- Serial SCSI Solutions
- Integrated Optical Components
- Futures
ADVANTAGES:

- Single Line vs. Multiple Lines for Parallel Transmission
- Small Connector Size
Issues/Requirements of the Serial Link

- Embedding and Recovering Clock → PLL Circuitry/Coding
- Bit and Byte (word) Alignment at Receiver → SYNC Symbols
- Filling Gaps Between Data → Idle Symbols
The TAXIchip Set

- Parallel, TTL Bus Interface, 4 to 17.5 Mbytes/sec
- Transparent Serial Link, 32 to 140 Mbits/sec (40 to 175 Mbaud)
- Simple STROBE/ACK Handshake at Transmitter
- Serial Side Easily Interfaces to Coaxial or Twisted Pair Cable, or Optical Components
TAXI Transmitter Block Diagram

- Strobe (STRB)
- Acknowledge (ACK)
- Clock (CLK)
- Data Mode Select (DMS)
- Data Command
- Input Latch
- Encoder Latch
- Data Encoder
- Shifter
- Media Interface

(SEROUT+) Serial Out +
(SEROUT−) Serial Out −
TAXI Receiver Block Diagram

Serial In + (SERIN+)
Serial In - (SERIN-)

Media Interface

Shifter

Decoder Latch

Data Decoder

Output Latch

Oscillator and Clock Gen.

PLL Clock Gen.

Byte Sync Logic

Data Mode Select (DMS)

Clock (CLK)

Data Strobe (DSTRB)

Command Strobe (CSTRB)

Note: N can be 8, 9, or 10 bits
Total of N + M = 12

(VLTN) Violation

Data

Command

N

M

AMD
Serial SCSI

SCSI Bus Interface

SCSI Bus Interface

TAXI TX

TAXI RX

TAXI TX

TAXI RX

SCSI Bus

SCSI Bus
Passive Bridge Circuit

- Allows for Full-Duplex Transmission over Single COAX
Linear Bus, Logical Ring Topology
Linear Bus, Logical Ring Orientations

- Connector choice determines Logical Orientation
TAXI COAX LIMIT

DATA RATE (Mbaud)

MAXIMUM COAX LENGTH (ft)
(UNCOMPENSATED, JITTER BOUNDED LIMIT)

RG 58/U

RG 174/U

AMD
FOX1 Components

- Contains TAXI and Optical Components Packaged Together
FOXI Open Assembly
- Plastic, Injection Molded Package

- LOW COST !!
ADM IN MOLDED PACKAGE