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X3T9.2/90-93

Date: 18 Jun 90
From: Kurt Chan, X3T9.2 Principal, Hewlett-Packard
To: X3T9.2 Membership
Subject: Single-ended crosstalk measurement results

I tested 14 SCSI cables for single-ended crosstalk. The purpose of this exercise was:

1. To determine the effects of crosstalk on SCSI data integrity,
2. To characterize the worst-case crosstalk for some commercially available cables, and
3. To begin an investigation into a termination algorithm for SCSI cables which minimizes crosstalk without sacrificing signal quality in other areas.

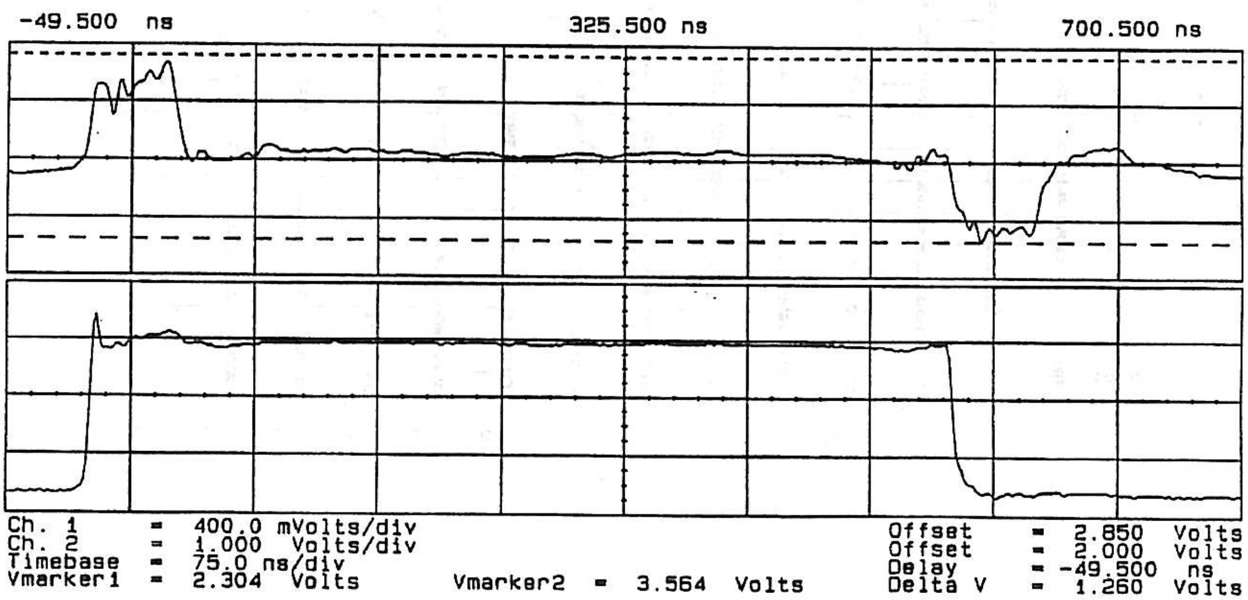
The following cable assemblies were tested using SCSI Alt-2 single-ended termination:

A: C&M 63281	B: Madison 4084	C: Montrose SCSI-2	D: Astro 28/30AWG	E: Hitachi 8212
F: Berktek 270288	G: Nek/Helix	H: Hitachi 8213	I: Furukawa 882814	J: Belden P1309
K: Madison 4099	L: Furukawa 891055	M: C&M 62327	N: Ribbon Cable	

Each of the cables was approximately 18 feet in length, terminated in SCSI-1 shielded connectors.

METHODOLOGY

25 open collector drivers, toggling at a 1 MHz, 50% duty cycle frequency were applied to a cable through 25 switches. One by one, each of the 25 pairs was left open while the other 24 were driven. The crosstalk on the undriven signal was measured. The classic "near-end" or "backward" crosstalk waveform on the quiescent signal appears below:



A pulse appears on the 2.85VDC quiescent signal coincident with each edge of the driving waveform. The widths of the crosstalk pulses are equal to two cable propagation delays, while the amplitudes are a function of:

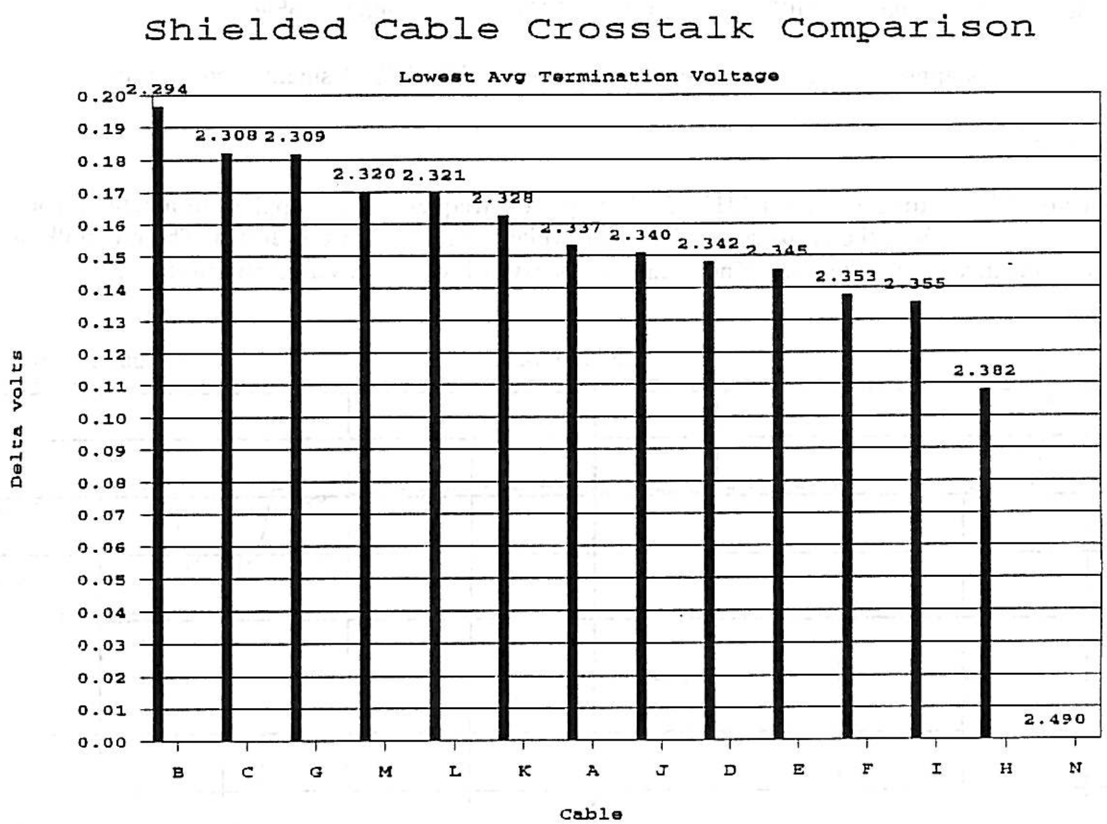
1. the mutual capacitances and inductances between the driving wires and the affected wire
2. the intrinsic capacitances and inductances of the wires
3. the amplitude of the driving signals.

TEST RESULTS

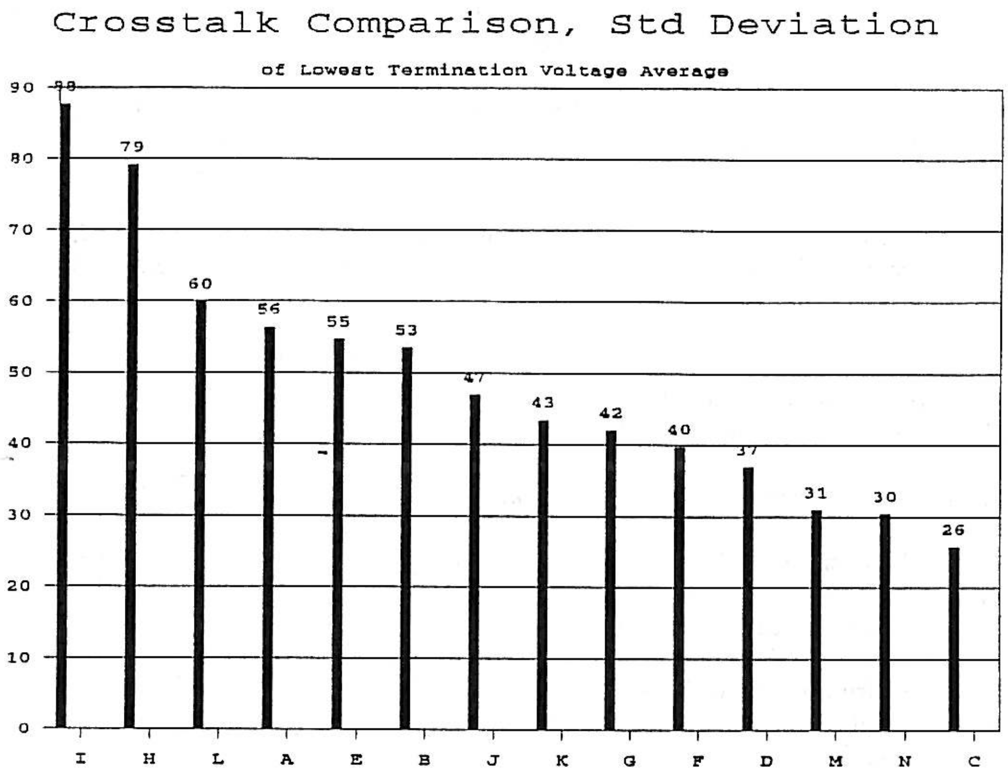
The voltages recorded in the following graph correspond to the lowest voltage measured on the negative-going crosstalk pulse when the quiescent signal is biased at 2.85 volts. The larger the voltage, the smaller the negative crosstalk pulse. The average low voltage due to crosstalk across all 13 shielded cable samples was 2.33V, indicating that worst case crosstalk can be responsible for half-volt "spikes" in the negative direction on deasserted (or rising) signals.

Scattergrams for each individual cable are attached to the end of this document. In some cases, the data was bifurcated, indicating perhaps that a buffer layer separated the cable pairs into two distinct layers.

The Y axis below is labeled to show the differences between the best cable (unshielded ribbon, cable N) and the cables under test. The greater the differences, the more susceptible the cable pairs are to crosstalk from one another.



The standard deviations for the cables are shown below in millilvolts. The higher values indicate a broader distribution of crosstalk susceptibility within each cable.



BACKGROUND and ANALYSIS

A few observations and conclusions can be made from this data:

1. The data here is extremely conservative - we don't really toggle 24 lines at a time (more like 8 or 9). Also, we have a few ground/TERMPWR lines interspersed in the cable which reduce crosstalk between the signal pairs.

2. The biggest difference in cable crosstalk performance occurs between shielded cables in general and unshielded ribbon cable. Ribbon cable differed from the **best** shielded cable by 108mV, whereas the best and worst shielded cables only differed by 88mV.

3. The differences between pairs within the cable (198mV) was greater than the average differences between the best and worst cables (88mV). All shielded cables tested are capable of equivalent crosstalk performance given suboptimal pair placement. Another way to state this is that **the differences between the cables were not significant compared to the differences that could be observed by selective placement of the pairs within the cable.** Gains are more likely to be realized by defining and avoiding worst-case pair placement rather than developing exotic cable technology.

4. Crosstalk can cause quiescent lines to fall up to .6V below the termination voltage. With proper Alt-2 termination, this shouldn't pose a problem (2.85-.6=2.25V, still above 2.0V) except in a scenario described below where REQ/ACK is transitioning at the same time as data. Crosstalk is more likely to have an effect

in systems where SCSI-2 signal quality recommendations are ignored.

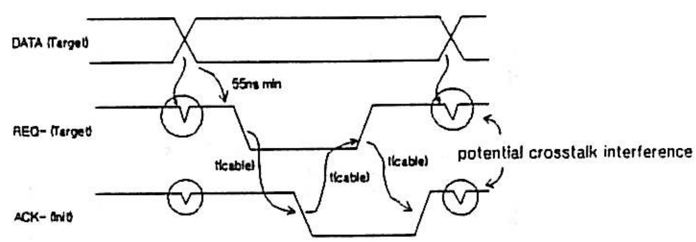
5. The two cables with the lowest average crosstalk had the highest standard deviations. These cables also had clearly bifurcated data patterns (see scattergrams).

One of the ideas presented at the last meeting was that the worst-case real life crosstalk scenario occurs when several data lines switch simultaneously and influence the edge-sensitive REQ and ACK lines. This is probably true, since:

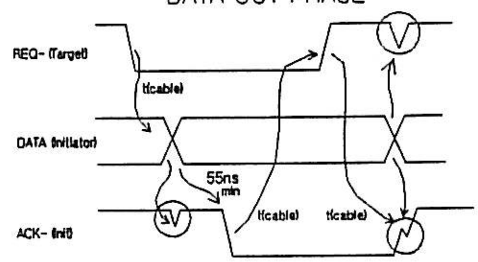
1. The receiver circuitry for REQ and ACK is generally of high speed and sensitive to edges.
2. The data lines change when REQ and ACK are deasserting or already deasserted - their most susceptible states.

Consider the following asynchronous timing. Circles show the areas where REQ and ACK are susceptible to crosstalk from adjacent data lines. On Data Out, ACK is susceptible at the beginning of the cycle and as it changes from low to high, or shortly thereafter. Crosstalk is especially dangerous if data is changing at the same time ACK is deasserting, since there is a greater liklihood that ACK will be near a receiver threshold point as it transitions from low to high. Any additional noise is therefore more likely to be misinterpreted as multiple edges. This is another argument for high-impedance cables; the cleaner we can make the deassertions, the less time will be spent in the transition region, and the lower the exposure to crosstalk susceptibility.

DATA IN PHASE



DATA OUT PHASE

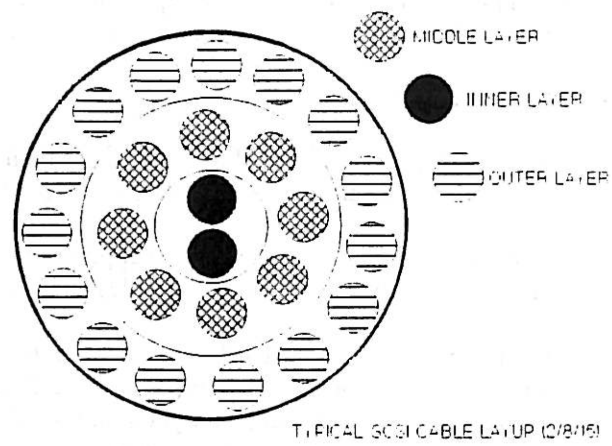


Traditional reasoning holds that the REQ and ACK lines should be placed on high-impedance pairs in the cable (near the center). However, in a cable with 2/8/15 or 3/9/13 contruction, putting the data lines around the REQ/ACK lines in the center may actually create worst-case crosstalk. Some layup schemes that have been proposed (see also diagram on next page):

	Inner Layer	Middle Layer	Outer Layer
Option 1	REQ, ACK	GND/TERMPWR (7 pairs) Parity (1 pair)	Data (8 pairs) Control (7 pairs)
Option 2	REQ, ACK	Control (7 pairs) Parity (1 pair)	Data (8 pairs), TERMPWR/GND (7 pairs)

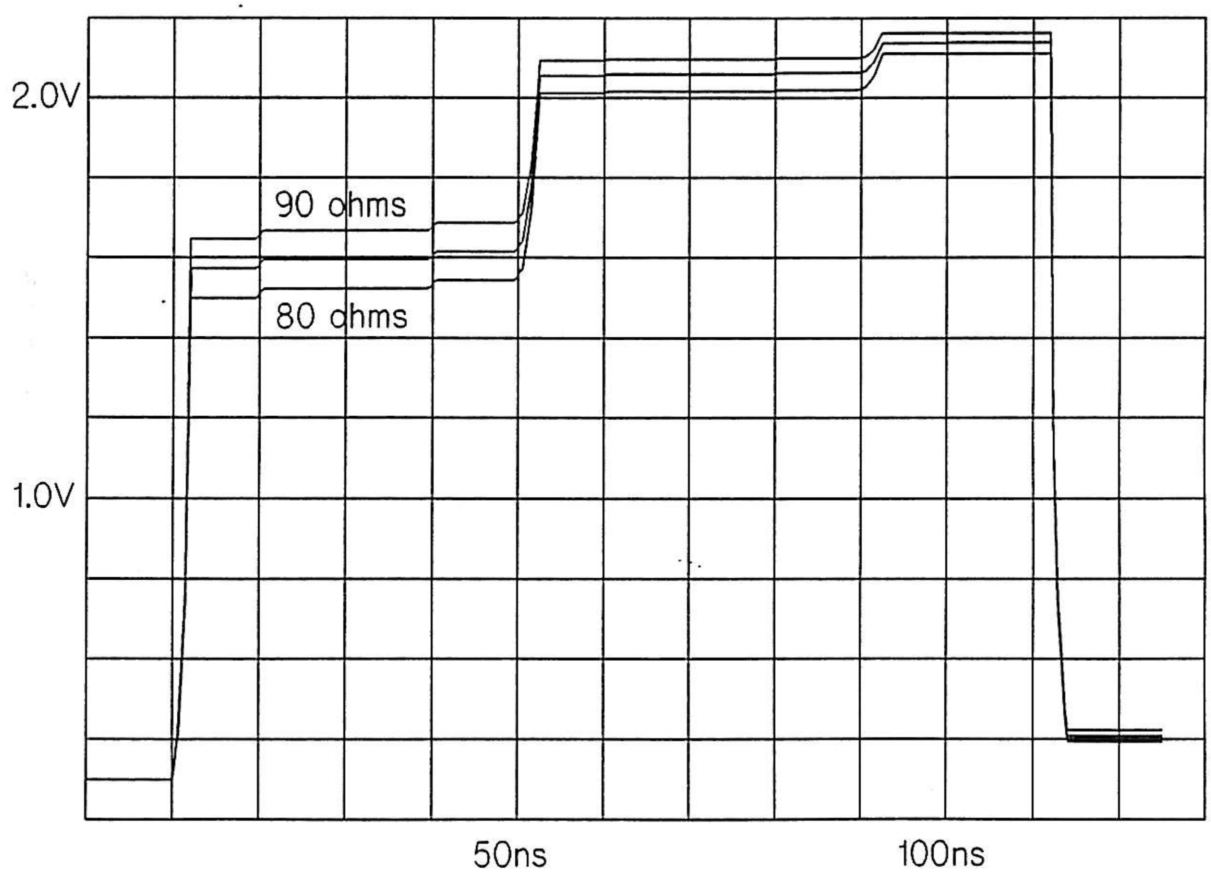
The problem with putting data on the outer layer is that we know that having high-speed lines on the low impedance pairs will reduce the likelihood that they will deassert cleanly and quickly. The question then is, what are the timing requirements for data on a single-ended bus, and is it worth trading off 5-10 ohms of impedance for what we think will be better crosstalk performance? The answer can be arrived at with some experimentation and analysis. But first, consider the effect of low impedance on SCSI timing.

In the previous asynchronous Data In timing, data must be valid 55ns plus a cable delay following a change (cable skew + deskew + recognition of REQ by initiator). The "cable delay" varies: it is whatever delay is necessary to get REQ from the target to the initiator, including any necessary reflections. If the transmission line delay of the REQ line versus the data lines differ by more than 55ns, the data won't be valid when the intiator asserts ACK and samples the data. 55ns is not quite two full propagation delays on an unloaded 6 meter SCSI cable. The problem is that in some cases slightly less than two cable delays is the MINIMUM time that will be incurred if a signal is not deasserted on it's first pass down the bus.



For example, if the initiator is 12" away from the target on a 6 meter bus and the target generates a strong deassertion, the signal will reach the initiator in about 1.7ns. If the deassertion is weak, the signal will have to propagate to the far end of the cable (about 35ns) and all the way back to the initiator (about 35ns minus 1.7ns). This means the difference between a weak (under the Vih threshold) and strong signal is a 60-70ns delay. This is the reason is it imperative to achieve signal transitions in a single cable delay, without requiring addititive reflections from the terminations to achieve valid signal levels. So our first focus should be getting the impedance of **all** pairs within the cable as high as possible.

80,85, and 90 ohm center driven lines, at center



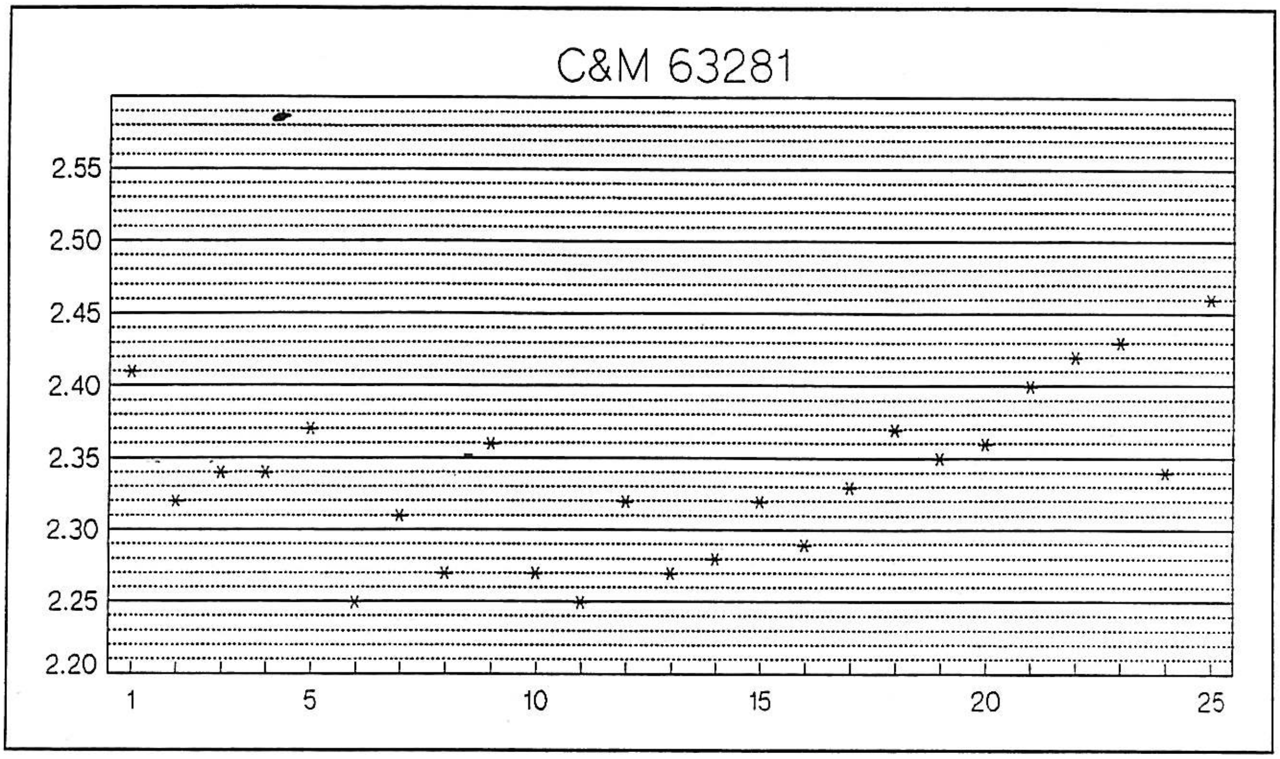
The effect of losing 5 ohms in impedance is shown in the SPICE plots. The initial step voltage decreases by about 100mV for each 5 ohms lost in impedance, given Alt2 termination. Note that this can be enough to cause the signal to violate the 2.0V V(ih) specification on it's first excursion down the cable.

FUTURE INVESTIGATION

1. Curious cable vendors should arrange to get their cables back from me for dissection, in order to confirm our hypothesis about lower-crosstalk pairs begin toward the perimeter of the cable.

2. Given that even the outer pairs can support single-delay deassertion, minimizing crosstalk by putting data pairs on the outer layer of shielded cables and REQ/ACK on the inner layers deserves more consideration.

   Over the next few weeks I will be evaulating the relative performance of cables terminated in "best" and "worst" configurations. If the differences in REQ/ACK crosstalk susceptibility is close to the 100mV advantage gained by putting data pairs on the middle layer versus the outer layer (assuming the difference in Z0 is about 5 ohms between these layers), it may benefit us to adopt one of these "best case" configurations.



C&M 63281
2.55
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2.35
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2.20
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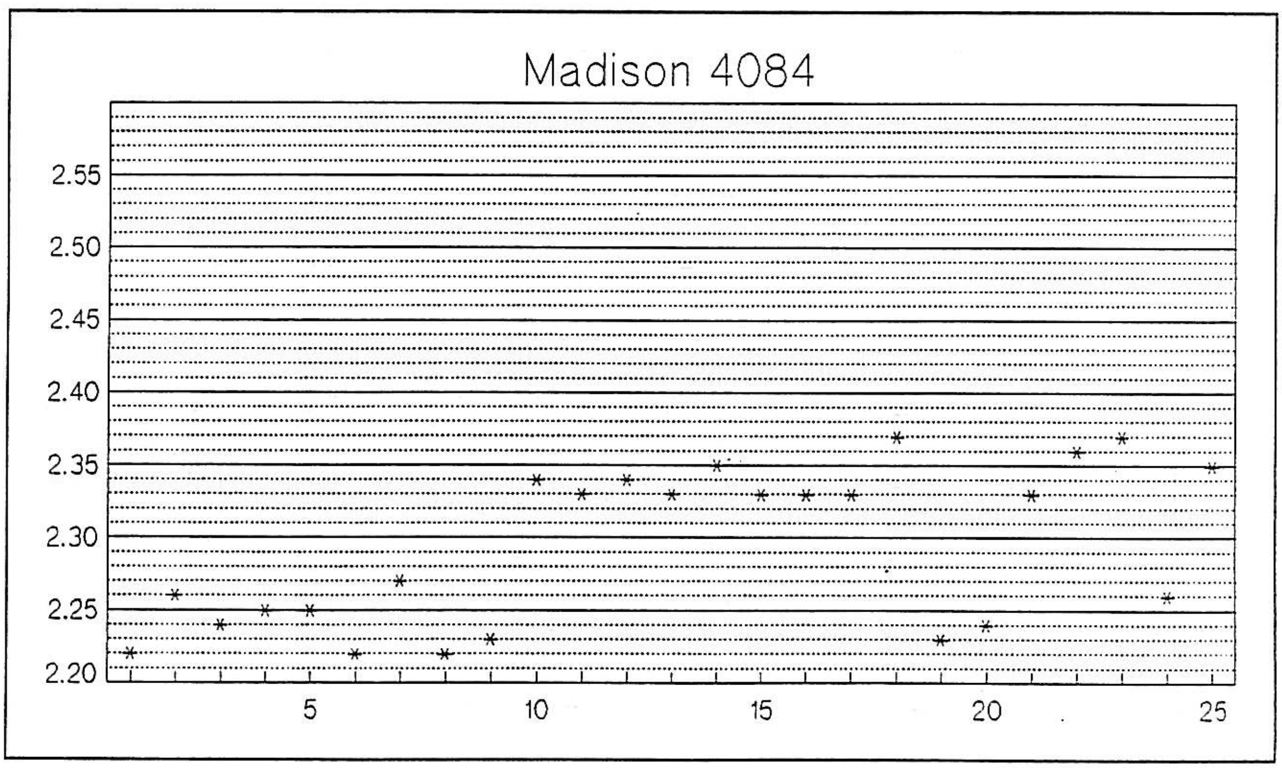
25



Madison 4084
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2.50
2.45
2.40
2.35
2.30
2.25
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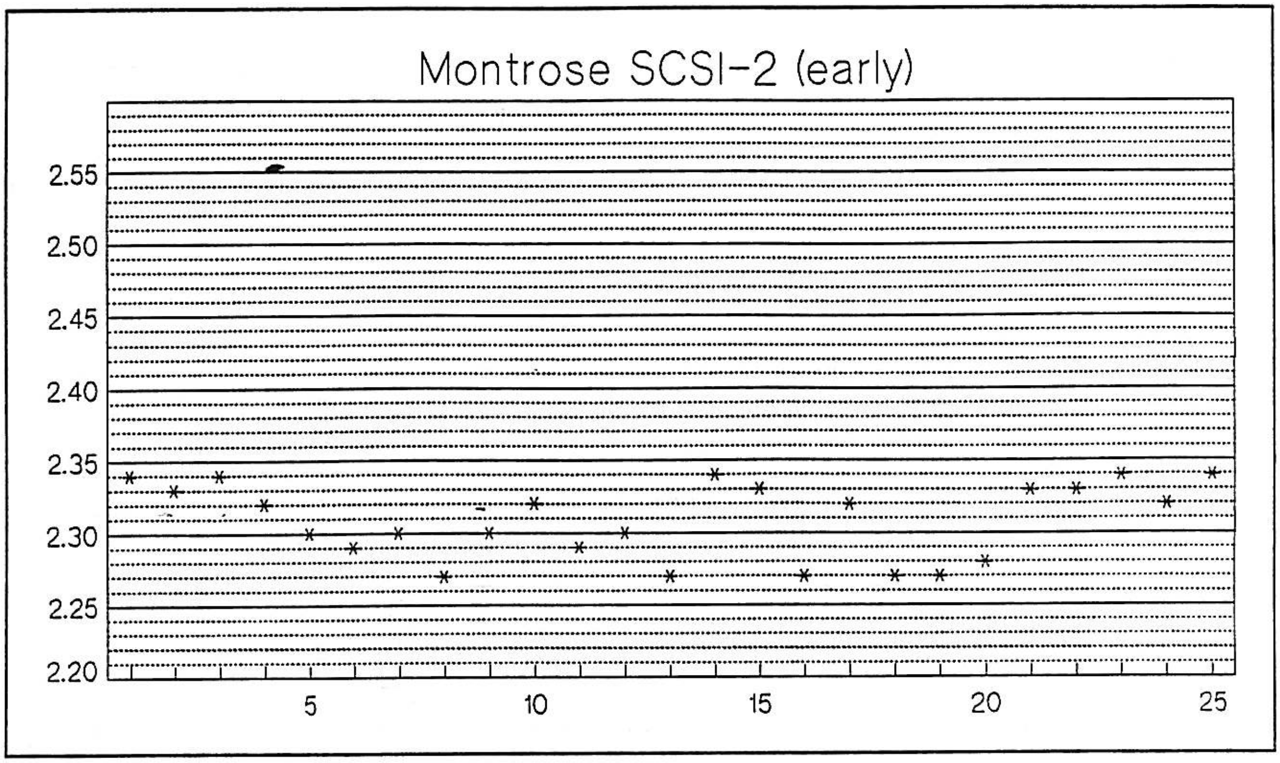
Montrose SCSI-2 (early)
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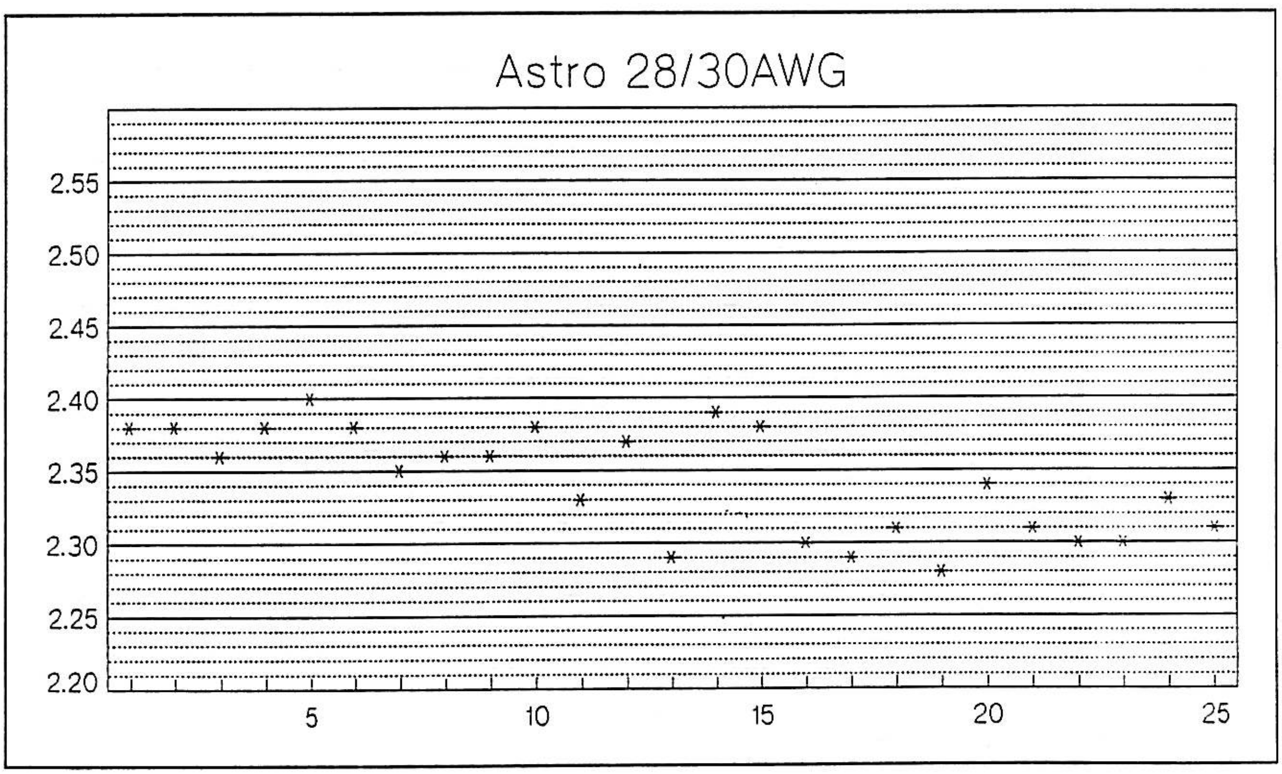
Astro 28/30AWG
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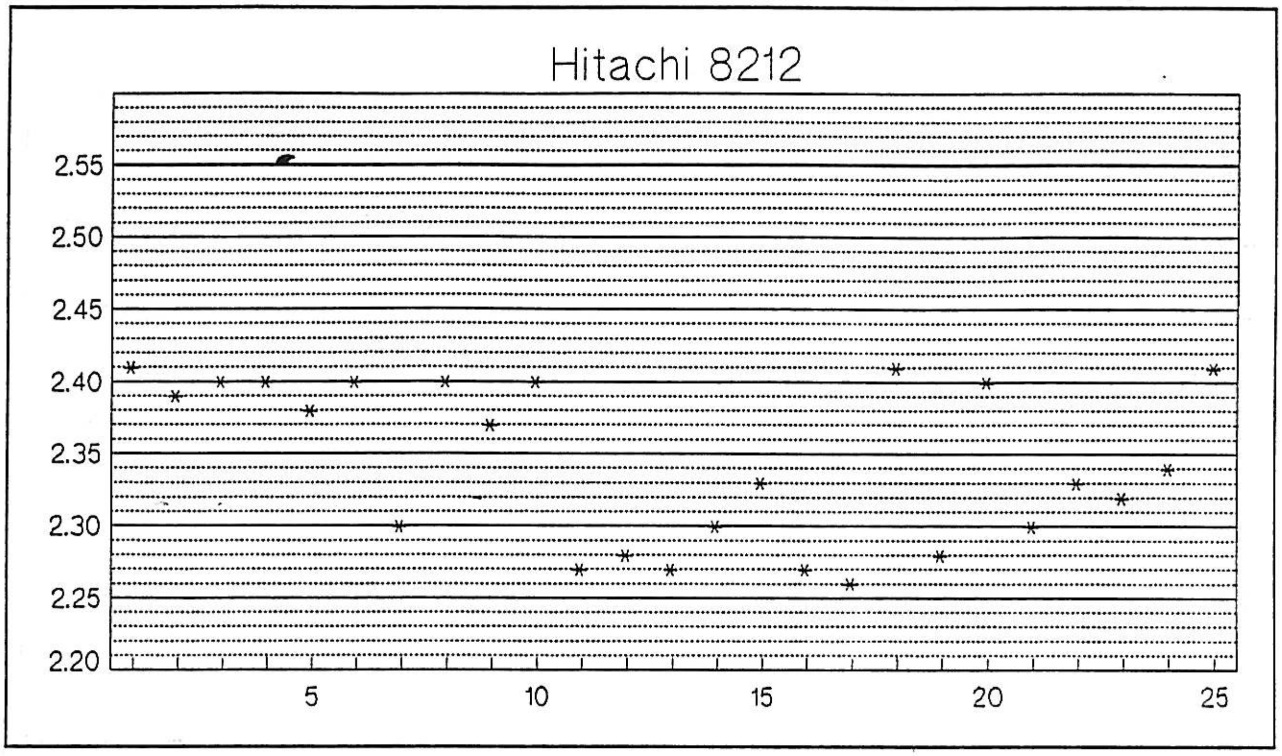
Hitachi 8212
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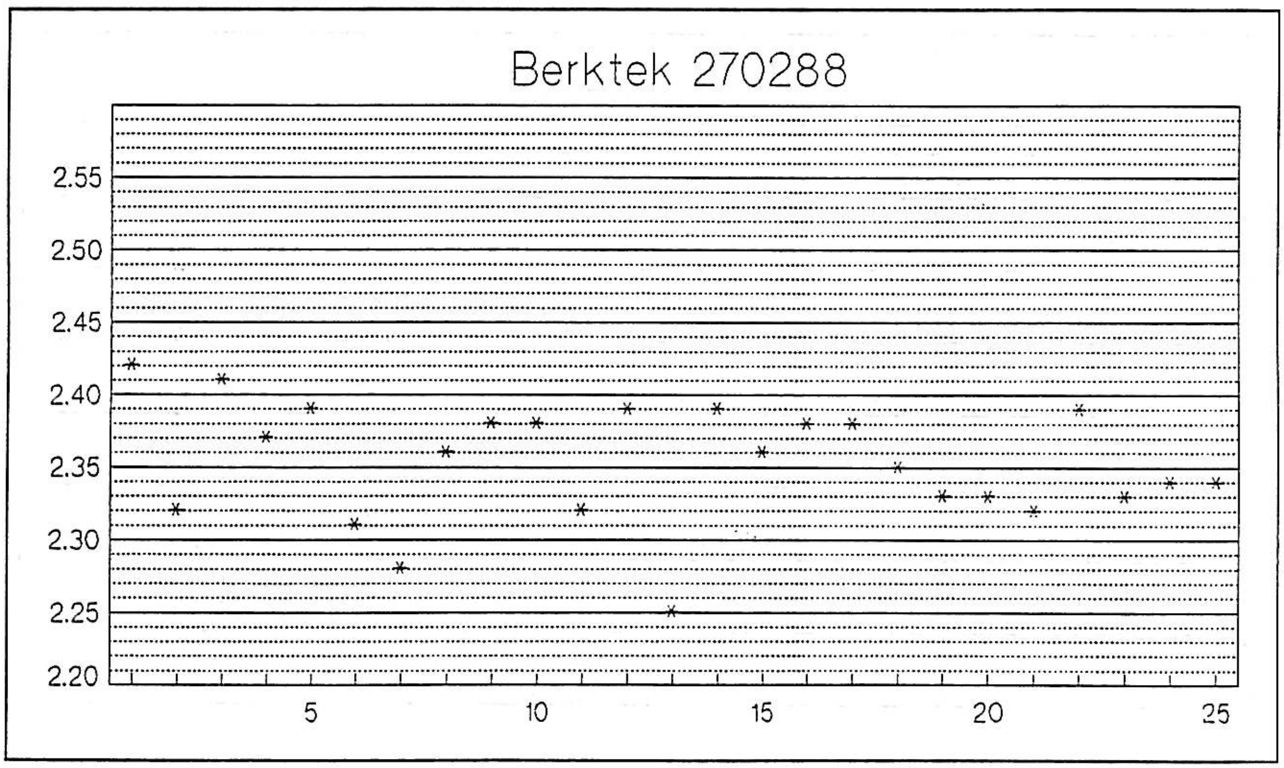
Berktek 270288
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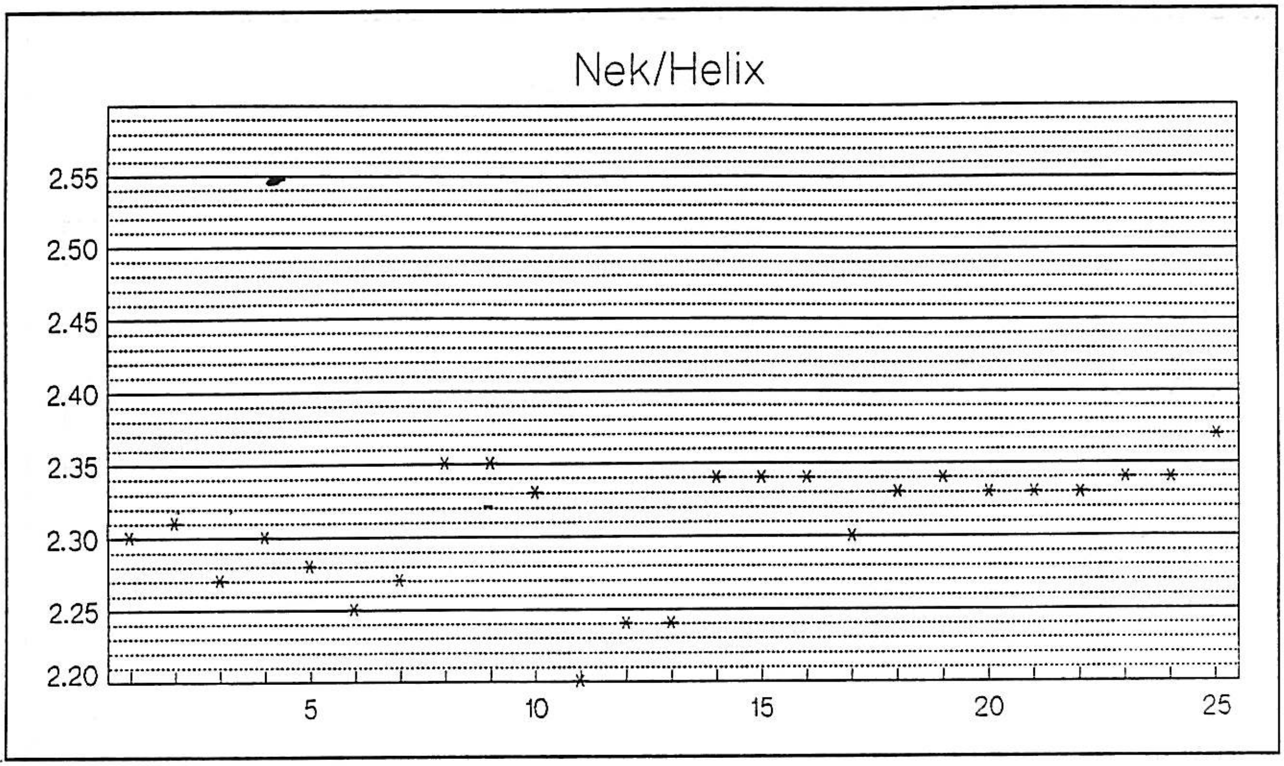
Nek/Helix
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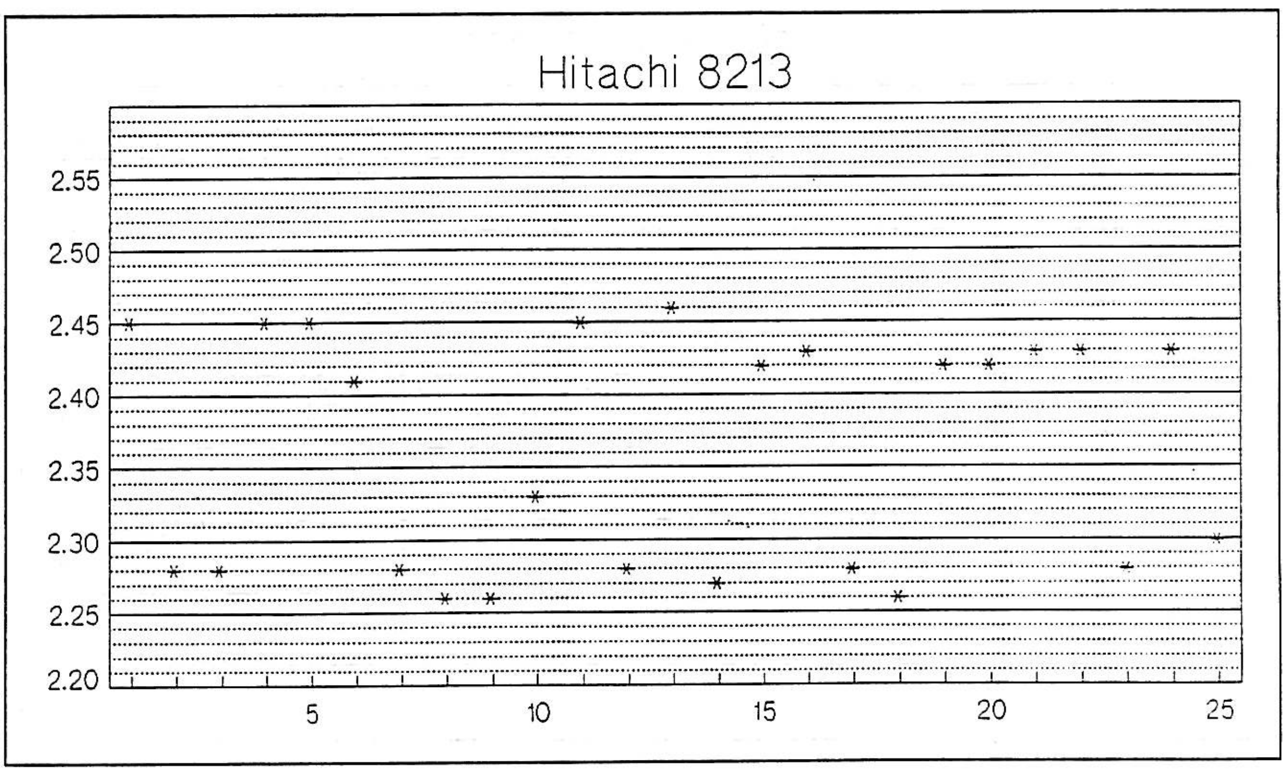
Hitachi 8213
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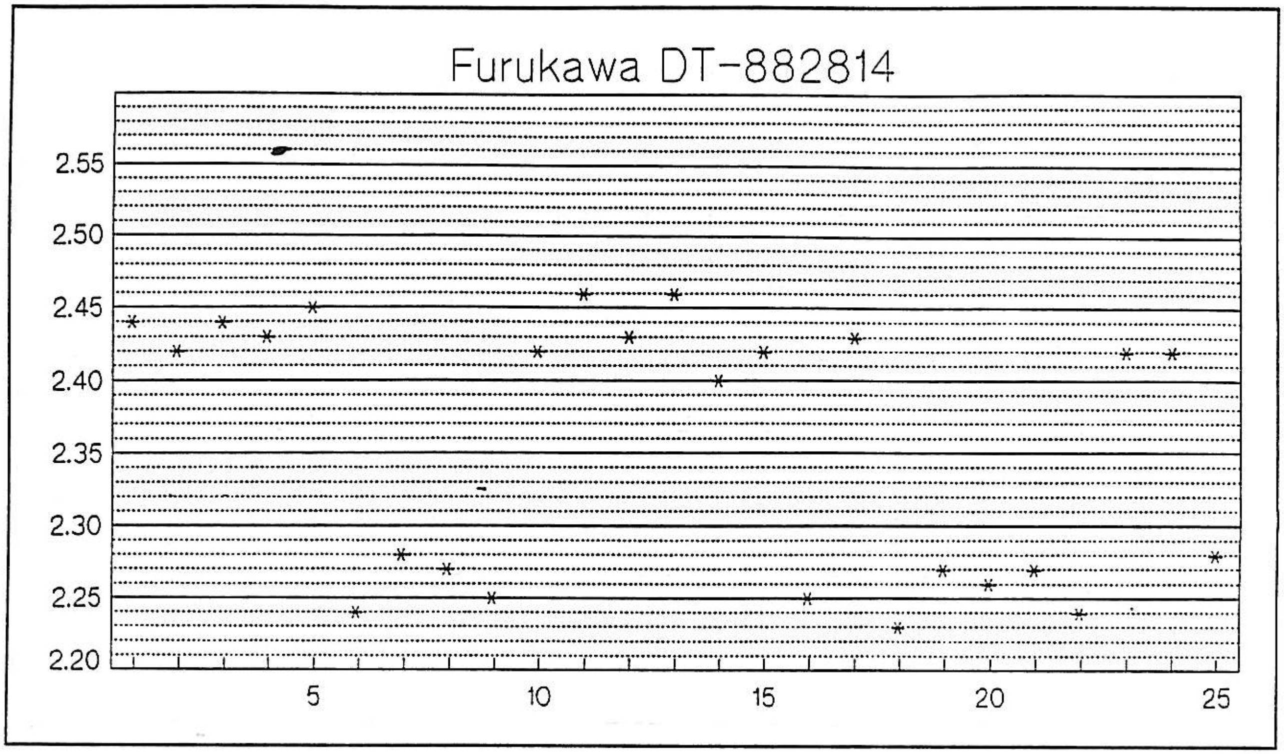
Furukawa DT-882814
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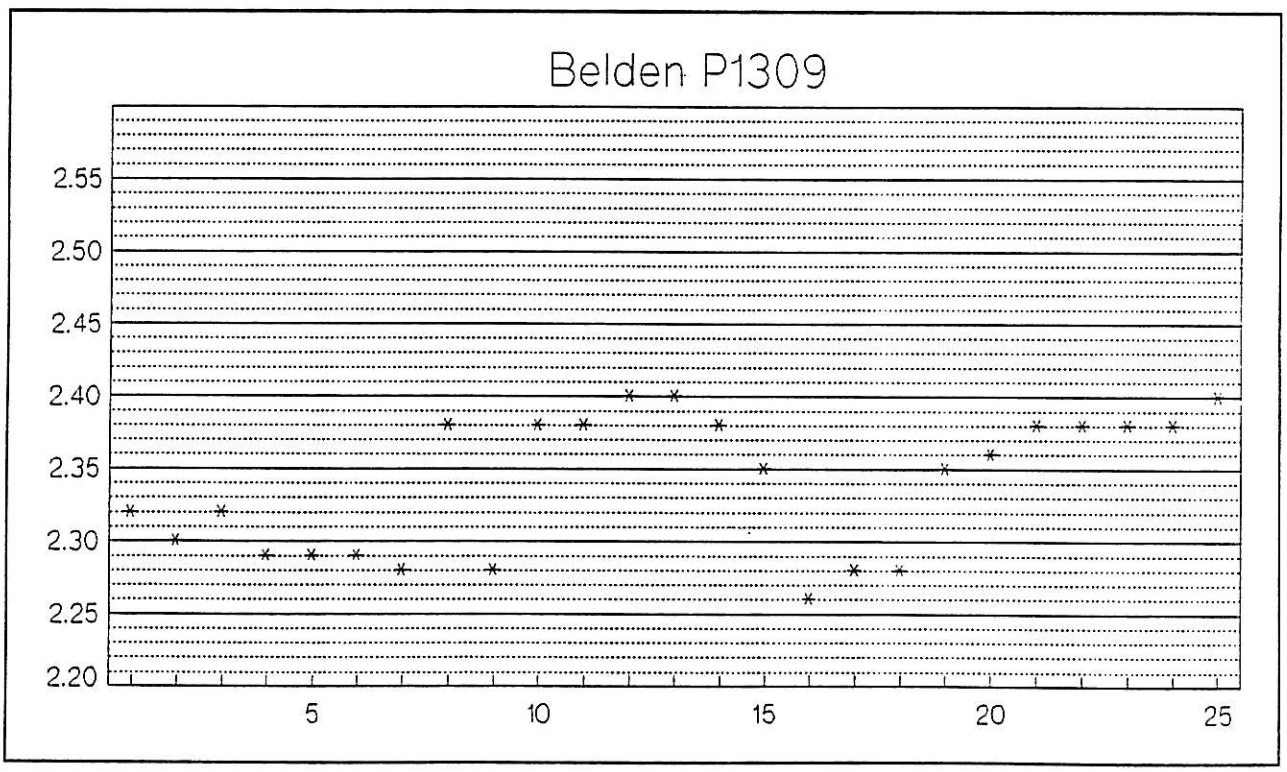
Belden P1309
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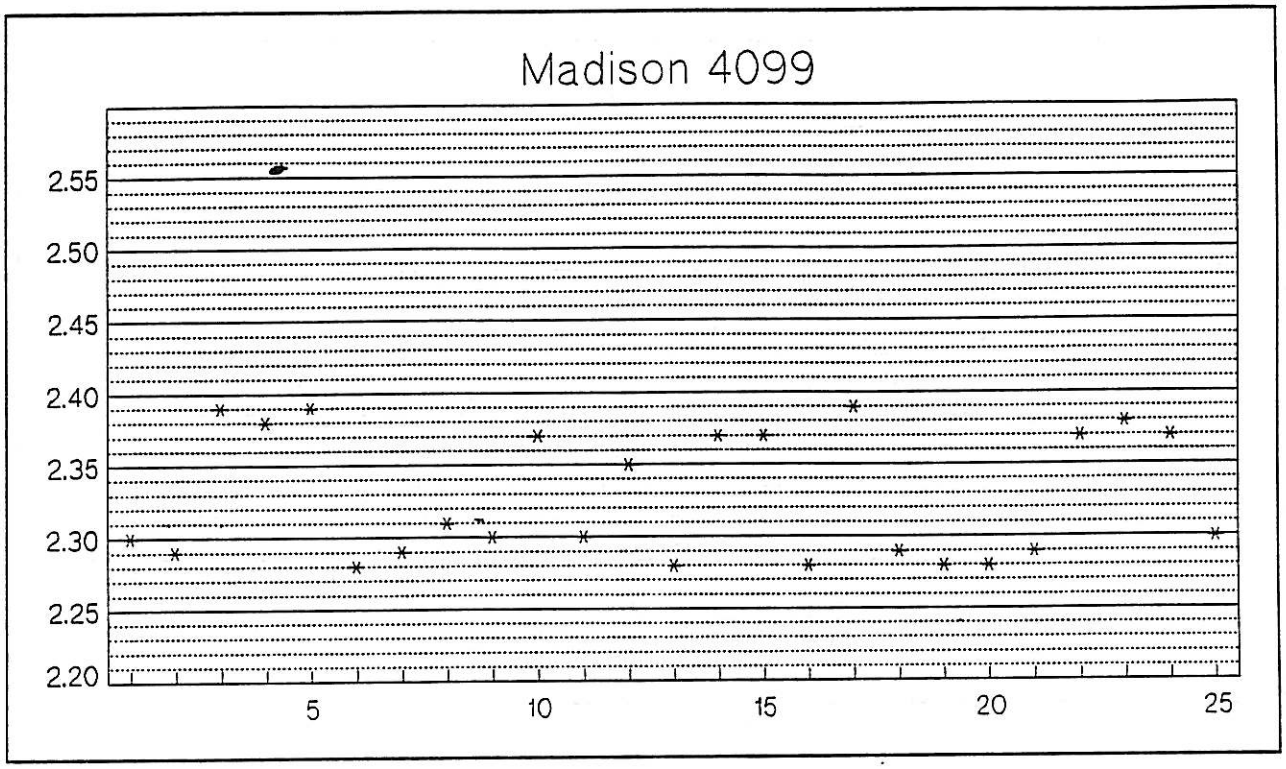
Madison 4099
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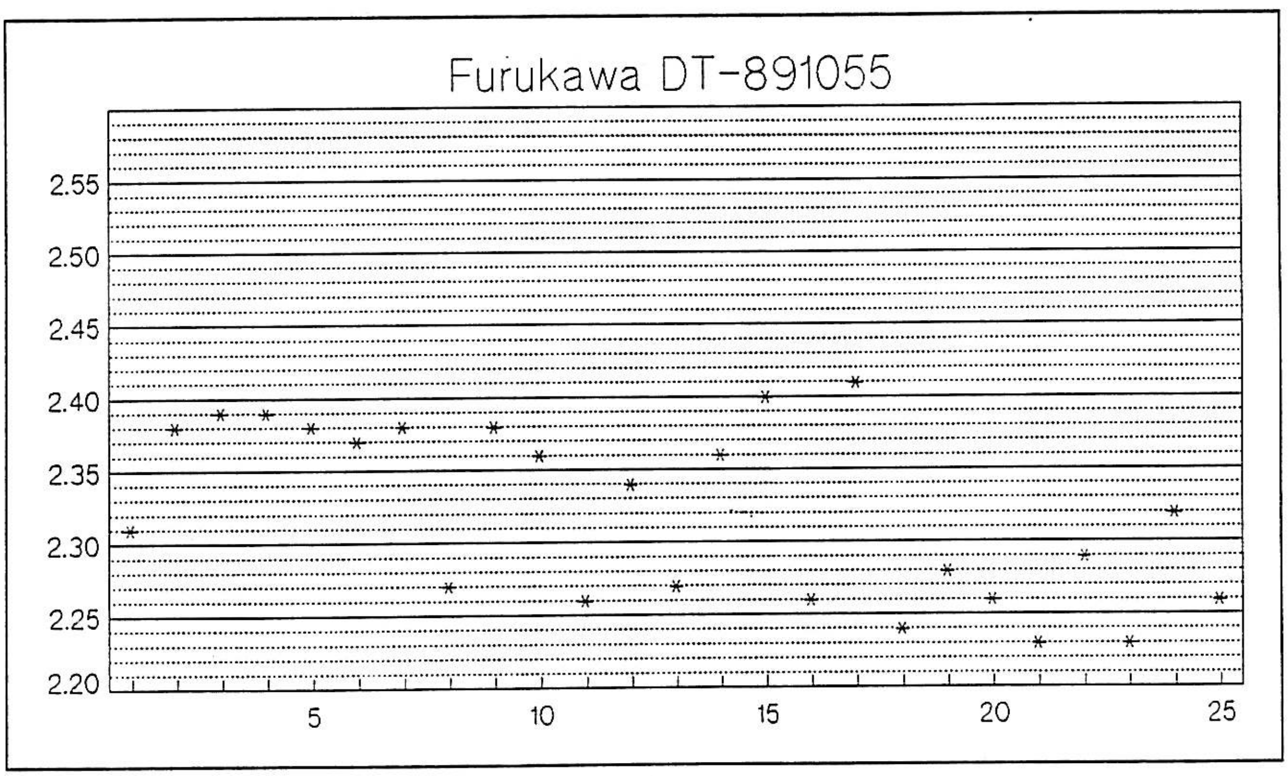
Furukawa DT-891055
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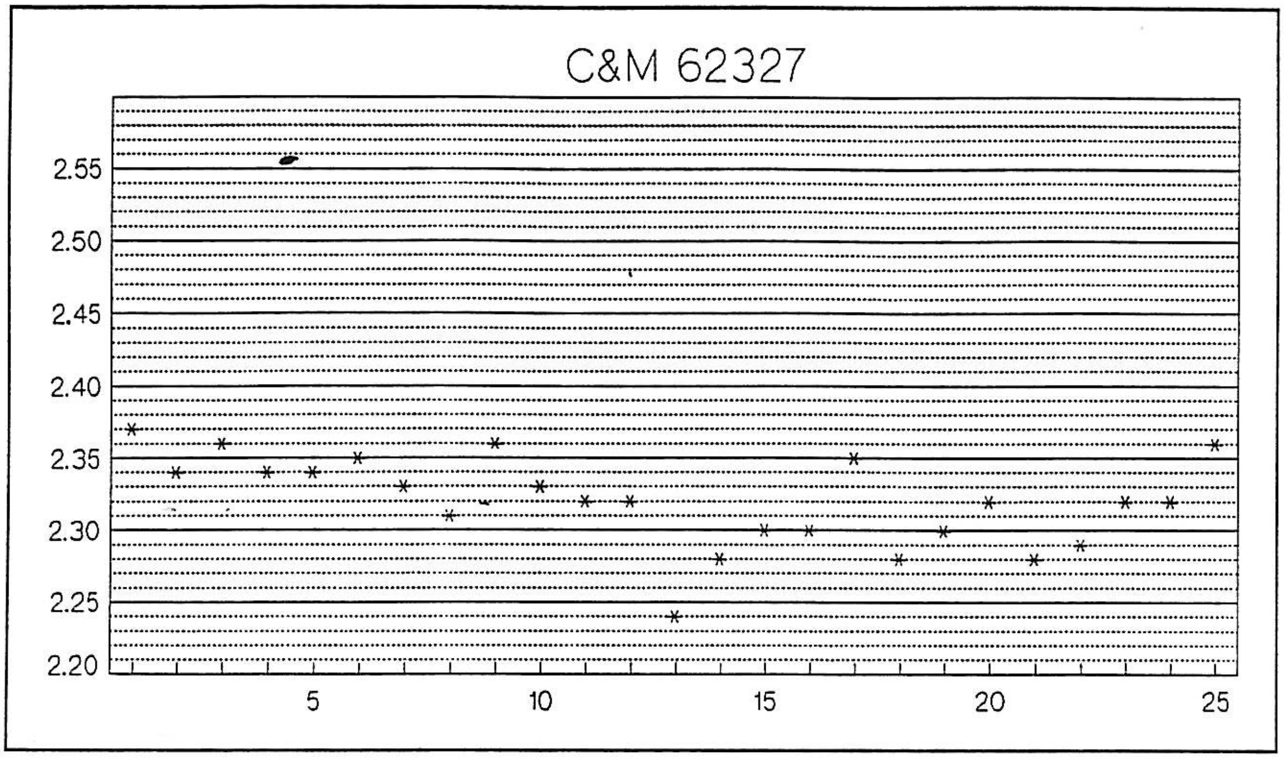

C&M 62327
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2.45
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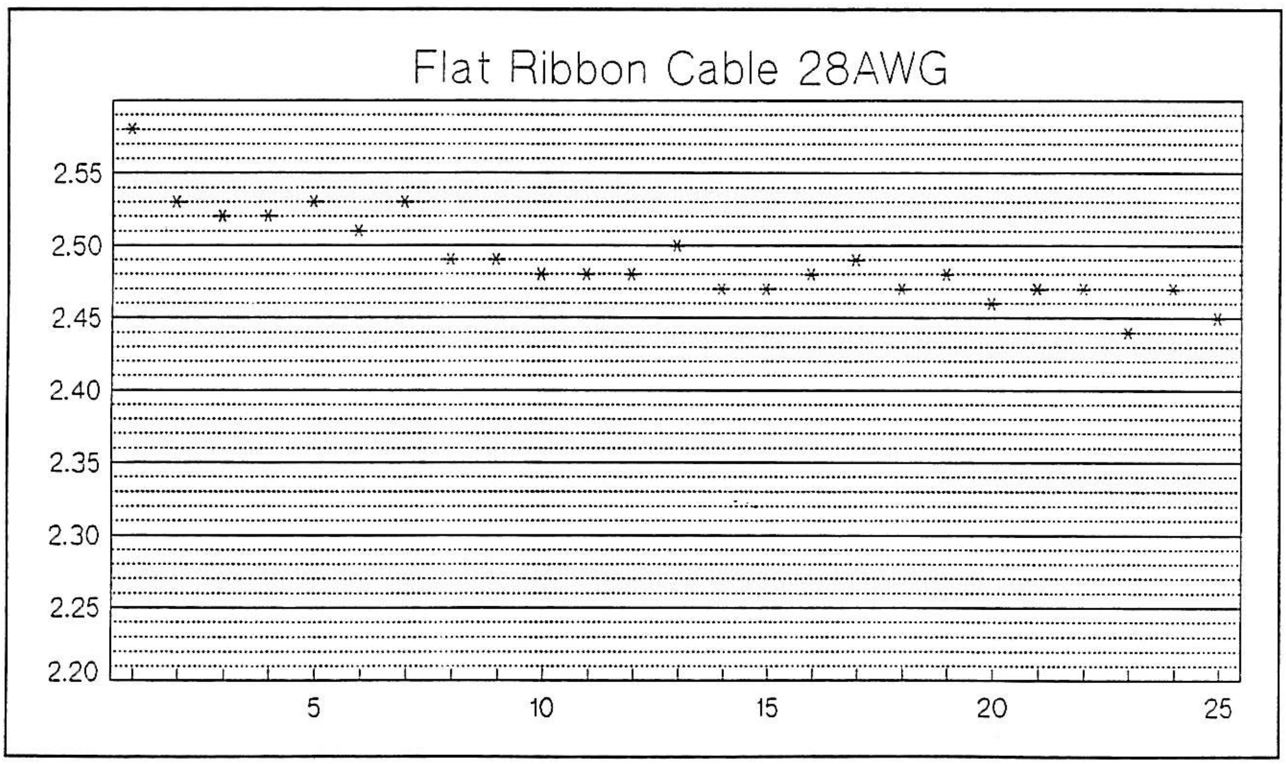

Flat Ribbon Cable 28AWG
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