AN

INTRODUCTION TO/UPDATE ON

THE

FIBER CHANNEL

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WHAT IS FIBER CHANNEL?

New Physical Layer (i.e. conductors, connectors, transceivers and low-level protocol) for:

SCSI Cmds/Messages	IPI Level 3 Protocol
HSC Data Link Layer	Other vendor protocols

All of the above to coexist on the same physical plant (perhaps to different equipments)

Faster and/or Longer and/or Better RFI/EMI than present copper interfaces

Smaller plant than copper at equivalent performance level

FIBER CHANNEL IS NOT A SIMPLE EXTENDER

WHY NEW LOW-LEVEL PROTOCOL?

Excessive overhead with current protocol due to long turnaround delays (over 10 microseconds @ 1KM)

Poor bandwidth utilization of "brute force" serialization approach

Different error mechanisms due to serial nature

Different architecture because separate fiber for each direction (i.e. each fiber is true simplex link)

Security an issue over these distances

SYSTEMS PRESENTED TO WORKING GROUP

ICL MACROLAN	Processor-peripheral s/s interface 50 Mb/s, 500m, compact token ring, led 20,000 nodes in field
HP-FL	Connection to remote disk cabinet 40 Mb/s, 500m, 820 nm frequency Serial copper intra-cabinet (low cost)
PARALAN/OPTIVISION	Fiber extenders for SCSI and DR-11W
CANSTAR/HUBNET	Expandable, broadcast hub system 100 Mb/s, collision arbitration

X3T9.2/89-118

SYSTEMS PRESENTED TO WORKING GROUP (CONTD)

DG FIBER ICB	I/O Subsystem i/f, 160 Mb/s, 2KM Serial copper short distance
GRUMMAN HS LAN	Expandable up to 200 KM Up to 800 Mb/s, fault tolerant Complex ring/star topology
ANCOR FASTNET	Expandable transparent circuit switch Up to 1Gb/s/chan Excellent cost/performance

MULTIPLE CLASSES

As in IPI and SCSI today

Plastic Class	5 - 10	Mbits/s @	20 meters
Multimode LED Class	200	Mbits/s @	2 Kilometers
Multimode Laser Class	200	Mbits/s @	5 Kilometers
	OR 1000	Mbits/s @	750 meters
Single Mode Class	1250	Mbits/s @	25 Kilometers

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ARCHITECTURE

Separate high speed and low speed functions

ECL or GaAs transceiver chip contains:

- transmitter and receiver
- electrical/optical conversion and vice versa
- clock source and recovery
- serial/parallel conversion and vice versa
- framing

CMOS interface chip acts on parallel data and contains:

- encoding and decoding
- error detection
- buffering

Intent is to standardize parallel interface between chips

WHY CODING?

Enable worst-case link parms: dc balance (rcvr sens)
run length (clock recover)

Provide control characters for framing and protocol use

Provide error detection

Four schemes presented to Group:

4B/5B	(AMD TAXI chips, FDDI)
8B/10B	(IBM, Hitachi channal)
8B/10B + FEC	(DEC)
"Naked"	(Ancor, Livermore and others)