

X3T9.2/88-001

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To: X3T9.2 Membership

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Subject: Update block modifications

This proposal is the result of a working group held during the San Diego meeting on Update Block command. The group felt that the Update Block and Read Update Block should be modified to allow only single block transfers. The reasons were:

1. Single block operation simplifies the implementation of an already difficult function.
2. Single block operation discourages the use of these commands in file system applications. These commands were originally intended for defect management use.
3. There was no compelling reason to include multiple block operation.

This proposal effects the commands defined in section 15. The group 5 versions are to be deleted, since they were included to increase the transfer length possible.

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UPDATE BLOCK Command

Peripheral Device Type: Optical Memory and Write-Once Read-Multiple  
Operation Code Type: Optional

UPDATE BLOCK Command

Bit	7	6	5	4	3	2	1	0
0	Operation Code (30h)							
1	Logical Unit Number			Reserved			RelAdr	
2	(MSB)							
3								
4	Logical Block Address							
5	(LSB)							
6	Reserved							
7	Reserved							
8	Reserved							
9	Control Byte							

[this concept of update operation as well as several others in the optical section need a theory or model to provide a framework for consistent implementation. a glossary of terms with definitions is also needed. to be done by L. Lamers ...ed.]

The UPDATE BLOCK command requests that the target logically replace data on the medium with the data sent during the DATA OUT phase.

The logical block address specifies the logical block address at which the update operation shall begin occur.

The transfer length specifies the number of contiguous logical blocks of data to transfer. A transfer length of zero indicates that no logical blocks shall be transferred. This condition shall not be considered as an error. Any other value indicates the number of logical blocks that shall be transferred. Support of transfer lengths greater than one is optional. If the target does not support the requested transfer length, it shall terminate the command with a CHECK CONDITION status. The sense key shall be set to ILLEGAL REQUEST.

This standard does not define the result of a WRITE command issued to a block previously updated by an UPDATE BLOCK command when blank checking is disabled.

[Note: The behavior of this command relative to the Enable Blank Check bit in MODE SELECT is defined there...ed.]

A logical block may be updated until the alternate block area is exhausted. The alternate blocks used for the update operation shall not be reported in the READ CAPACITY data. If the alternate block area is exhausted the command shall be terminated with CHECK CONDITION and the sense key shall be set to MEDIUM ERROR.

[the following still needs work relative to the device models...ed.]

If the error recovery parameter specifies posting of recovered errors and if a read operation of a logical block that has had a successful update operation performed occurs the command shall terminate with a CHECK CONDITION status. The sense key shall be set to RECOVERED ERROR and the additional sense code set to [\_\_\_\_\_].

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READ UPDATED BLOCK Command

Peripheral Device Type: Optical Memory  
Operation Code Type: Optional

READ UPDATED BLOCK Command

Bit	7	6	5	4	3	2	1	0	
0	Operation Code (2Dh)								
1	Logical Unit Number		DPO	FUA	Reserved	RUBB	RelAdr		
2	(MSB)								
3	Logical Block Address								
4									
5	(LSB)								
6	Latest (MSB)		Generation Address					(LSB)	
7									
8	Reserved								
9	Control Byte								

The READ UPDATED BLOCK command (Table 15-\_\_) requests that the target transfer data to the initiator from the specified generation(s) and logical block(s).

The logical block address specifies the logical block at which the read operation shall begin occur.

The transfer length specifies the number of contiguous logical blocks of data that shall be transferred. A transfer length of zero indicates that no data shall be transferred. This condition shall not be considered as an error. Any other value indicates the number of logical blocks that shall be transferred. If the transfer length and generation address specified results in exceeding the number of existing generations for the logical block specified, the command shall be terminated with a CHECK CONDITION status. The sense key shall be set to ILLEGAL REQUEST.

The Latest bit determines the meaning of the generation address field. A Latest bit of zero indicates that the generation address is specified relative to the first generation of the block; generation address zero specifies the first generation. Increasing generation addresses specify later generations.

A Latest bit of one indicates that the generation address is specified relative to the latest generation of the block; generation address zero

specifies the most recent generation. Increasing generation addresses specify earlier generations.

A Read Updated Blocks Data (RUBB) bit of 0 requests the target to transfer the data from multiple generations of the single logical block specified. The transfer begins at the generation address of the logical block address specified and continues transferring increasing generation addresses of the logical block address specified, as defined by the Latest bit.

A RUBB bit of 1 requests the target to transfer the data from each logical block of the single generation specified. The transfer begins at the logical block address of the generation address specified and continues transferring increasing logical block addresses of the generation address specified.

If any the requested generation does not exist, the command shall be terminated with a CHECK CONDITION status and the sense key shall be set to BLANK CHECK, with an additional sense code of Generation Does Not Exist.

This command shall be terminated with a status of RESERVATION CONFLICT if any reservation access conflict (see 8.1.8) exists and no data shall be transferred.

See section 6.2.4 for a description of the cache control bits (DPO and FUA).  
See section 6.2.5 for a description of the relative address bit (RelAdr).

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