X3T9.2/87-216

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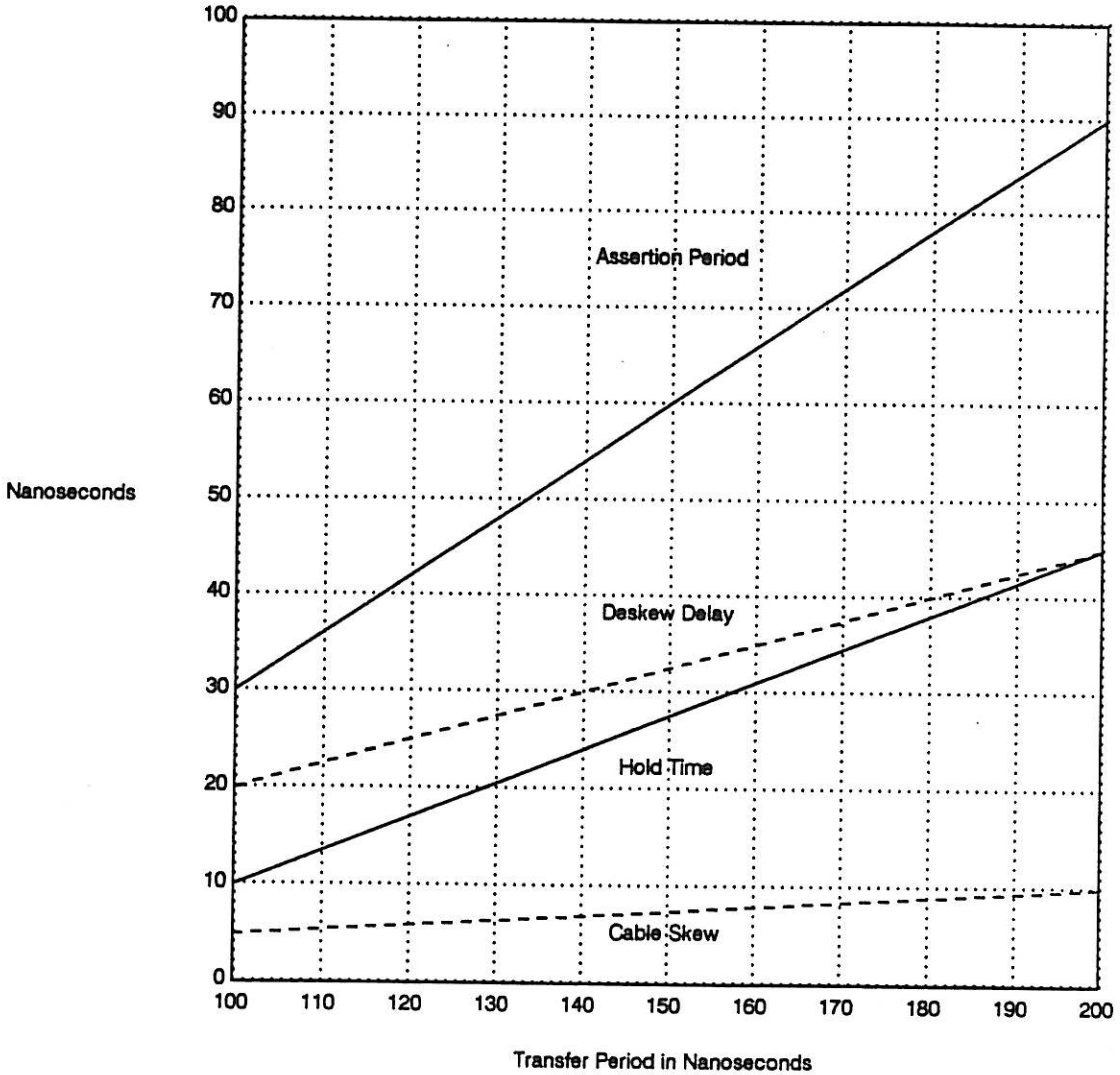
To: San Jose Working Group

This is only a "temporary" working group document; I don't propose it have an X3T9.2 document number.

I have taken a second look at Assertion/Negation times as suggested by NCR. After talking with National's engineers, we believe reducing this value from 45nS to 30nS would make designing future protocol chip easier and not degrade performance at all. I am negotiable on reducing it 5nS further to 25nS, although we prefer 30nS.

Document #195 stands now as Rev. 1 with the ammendments shown. I still recomend the linear transition between old and new parameters as the best way to squeeze the most performance out of future chips. Below is a graph which could be used to look up needed timing parameters for fast synchronous mode.

Synchronous Timing Parameters
Linear Transition from SCSI-1 to Fast SCSI



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