X3T9.2/87-123

To: X3T9 working Group

From: Dal Allan and Jayshree Ullal 6/8/87

The next working group meeting will be held by Fairchild on July 16 and July 17 at 10400 Ridgeview Ct, Cupertino. For further information, please contact Gary Murdock at (415)864 6200. Please see attached map for dirctions. The most convenient hotel is still the Sunnyvale Hilton (408-738-4888). No arrangements have been made so you are on your own.

The agenda for the meeting is as follows;

July 16th 9 AM - 12 NOQN: Joint IPI/HSC Meeting

July 16 afternoon and July 17 morning: the IPI and HSC groups will break up to hold independent meetings.

Faster IPI will devote their time to discussing the Lower physics laws and study proposed drivers and receivers, cable constraints etc.

High Speed Channel will continue working on the definition of the Functional requirements and study different proposals.

July 17th 1 PM onwards: Joint meeting for IPI and HSC.

Attached is a draft of the minutes of the last working group meeting held on May 14th and 15th, at National Semiconductor. The draft consists of two sections: minutes of the faster/faster and wider/wider IPI working group and minutes of the High Speed Channel (HSC) working group.

We look forward to seeing you at the meeting.

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THIS IS A DRAFT OF THE MINUTES FOR THE FIRST SECTION OF THE FFWW MEETING HELD ON MAY 14 AND 15, 1987, AT NATIONAL SEMICONDUCTOR IN SANTA CLARA, CALIFORNIA.

The meeting of the faster/faster wider/wider working group of ANSI X3T9.2 and ANSI X3T9.3 was held on May 14 and 15, 1987 at National Semiconductor in Santa Clara, California. Bob Morris of Simulex opened the meeting. Attendees included:

Adaptec	Robert Snively	IBM	Henry Brandt
Amdahl	Ed Cardinal	IBM	Ken Moe
Amdahl	Masanori Motegi	IBM	Horst Truestedt
AMD	Jayshree Ullal	JVNC/ZeroOne	Pete Paluzzi
CDC/Canada	Roger Cummings	Los Alamos	Gene Dornhoff
CDC/MPI	Tom Leland	Los Alamos	Don Tolmie
CDC/MPI	Rick Mansfield	Martin Marietta	Dennis Bowman
CDC/Systems	Wayne Sanderson	Miltope	Dan Klang
Convex	Alan Gant	MMI	Kenneth Won
Convex	Tom McClendon	Multiflow	Lynn D'Amico
ELXSI	Robert Thomas	National Semi	Randy Davis
ELXSI	Doug Zumbiel	National Semi	Kumar Sivesothy
ENDL	Dal Allan	National Semi	Jim Schuessler
Fairchild	Gary Murdock	Texas Inst	Rene Clabaugh
Fujitsu America	Bob Driscal	Ultra	Newt Perdue
Fujitsu America	Jim Luttrull		
Gould	Ed Balogh		
GP Associates	Bob Grow		
GP Associates	Ron Perloff		
Hitachi Micro	Sam Karunarithi		
HP	Del Hanson		
IBIS	Ed Dacey		

Kumar Sivasothy of National Semiconductor presented the results of his studies on the performance characteristics of the DS3695 operating in a restricted IPI/SCSI environment. After careful consideration of the capabilities of the drivers, cables, and receivers, he concluded that a clock rate of approximately 12.5 Megatransfers per second could be achieved over a 50 meter cable. The study has not yet included the effects of cross talk or injected noise.

Ken Moe of IBM presented the results of an earlier study of the current mode drivers operating on a 200 foot cable. His study demonstrated that IPI could operate safely at 10 Megatransfers per second for a net data rate of 20 Megabytes. At higher frequencies, significant pattern dependent jitter began to be visible.

During these two presentations, there was considerable discussion about the actual meaning of the information presented. Statistical slight of hand was required to actually achieve the required operational speeds. The proposed changes in the National specification and slightly improved screening of chips would probably suffice to make the magic real.

Don Tolmie indicated that their studies were not yet complete. He brought in information about FASTBUS (IEEE 960) and the Cray HSX channel as samples of machines that reach very high data rates. He indicated that Cray did not seem to have any interest in offering their channel as a standard. Don Tolmie's early results indicate that the 25 Megatransfer rate they hope to achieve could not be supported for long cables. The length limit may be around 15 meters.

Bob Morris of Simulex presented results that indicated that very high efficiencies could be achieved during the data transfer portion of IPI operation. Overheads of under 5 microseconds per burst could be expected with the proposed chip implementation. Efficiencies of 30 to 99 percent could be achieved, depending on the block length and actual data rate. Two K transfers at 20 Megabytes would have 87% efficiency.

Roger Cummings of CDC generated a new skew budget based on the new information presented during the morning. The skew budget demonstrated that a carefully designed system could operate at better than 10 Megatransfers per second.

Wayne Sanderson of CDC presented a graphic version of Bob Morris's efficiency analysis.

Dal Allan presented an overview of the IPI architecture. The overview brought all members of the meeting up to full understanding of the IPI characteristics which would be helpful in high bandwidth environments. It was noted that SCSI could also provide significant performance capabilities.

Ed Dacey of IBIS presented an overview of the original goals of the FF/WW working group. He then introduced a proposed parallel control protocol for IPI-2 that he felt would be important to the implementation of high performance IBIS drives.

Bob Morris of Simulex indicated that device level interfaces were required to achieve the ultimate in performance. Bob Snively of Adaptec indicated that the same performance levels could be achieved with higher level interfaces with appropriate design choices.

After some introductory remarks, the choice of goals and organizational changes necessary to achieve the goals for both very high performance IPI and SCSI and for the High Speed Channel were deferred to the second day. (See the rest of the minutes from the second day secretary).

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THIS IS A DRAFT OF THE MINUTES FOR THE SECOND SECTION OF THE MAY14TH,15TH HELD AT NATIONAL SEMICONDUCTOR FOR HIGH SPEED CHANNEL WORKING GROUP.

The meeting was chaired by Dal Allan. Dal opened the meeting by describing the X3T9 structure and emphasized the need for a technical document editor for any new working group. He also stated the need to divide the goals of the working group into three classifications:

Faster/Faster:
1. Study IPI performance with existing drivers
2. Study IPI performance with new (currently available) drivers with a goal of 12/87
3. Study and define high speed channel requirements. This may be a two year effort.

Wider/Wider
Needs documentation
Study connector issues

Master/Master
Need to define functional requirements.

FF/WW/MM are all enhancements to the current IPI which will be studied by the working group as expansion efforts.

HSC Functional Requirements

Global Goals: FAST

Generic Goals: Media - Fiber?

Specific Goals: Modularity - n X 50 MB/s

Global Goals:

Interconnectablity

Data Rate: 200 Mbytes with stepping increments starting at 50 Mbytes/s

Distance: 25 meters for proximity - depends on lower physics.
1 km for long distances.

Data Integrity: 10e-15 raw error rate for fiber.
Implicit error recovery at transport layer.
May need encoding/decoding

Other Globals: Undetected error rate 10e-9
Does not exclude networking, but OSI compliance is not necessary.
Does not prevent time-critical applications

Generic Goals:

- Hybrid versus dedicated control/data
- Protocoal commonality to differnt transmission.
- Common data transfer mechanisms.
- Duplex control of simplex data transfer.
- Three media options:
  - Parallel Copper
  - Parallel Fiber
  - Serial Fiber

Functional Block Diagram of Options:

64 bits?

PHY 1 PROTOCOL & ELECTRICAL INTERFACE

(Determines direction, and controls method of data management)

PHY 0 TRAMINSMISSION CHARACTERISTICS

(Media, Parallel or Serial, Connectors, Drivers and Receivers)

Definitions: (To be refined)

Interconnectability: Two machines can communicated with each other within the same options.

Modularity: To be defined.

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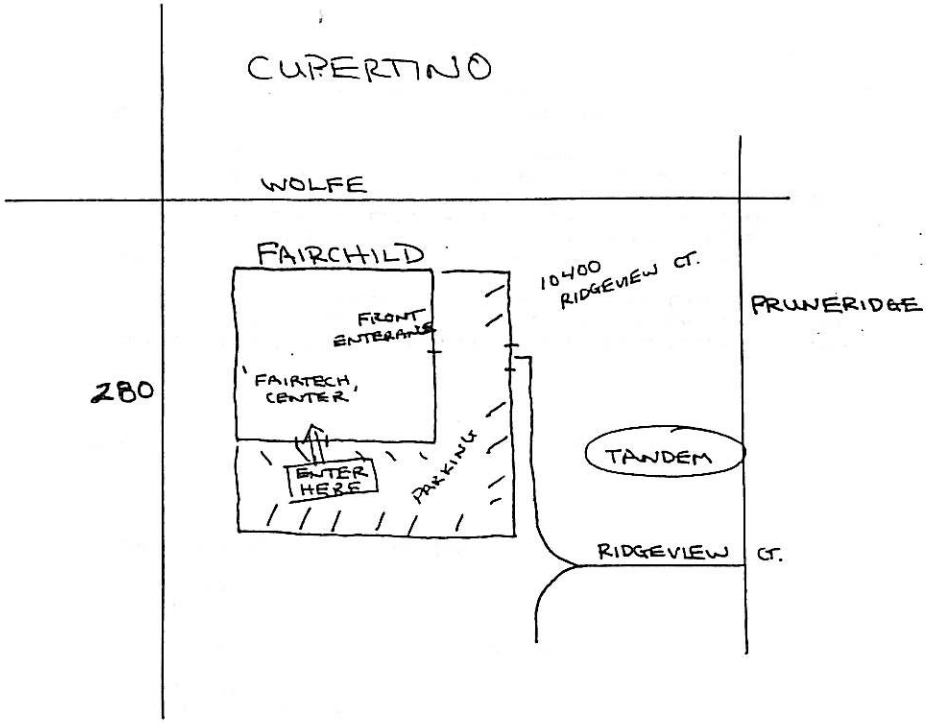
FAIRCHILD
A Schlumberger Company

FAIRTECH

NORTH

Next X3T9 WG Meeting
July 16 & 17



FAIRCHILD CUPERTINO:
408 - 864 - 6200

GARY MURDOCK
415 - 962 - 4027

TRANSMISSION PARAMETERS

#	GROUP	DESCRIPTION		AVG	MIN	MAX	DIFF
0	Config	Transmitting Logic Skew					
1	Config	Foll Delay					
2	Xcvr	Transmitter Prop Delay					
3	Xcvr	Transmitter Asymmetry					
4	Xcvr	Transmitter Rise/Fall Time					
5	Xcvr	Charge Cable Time					
6	Xcvr	Bias Asymmetry					
7	Config	Foll Delay					
8	Config	Drop Cable Prop Delay					
		CONNECTOR (To be spec value)					
10	Cable	External Cable Prop Delay					
11	Cable	Jitter					
12	Cable	Intersymbol Interference					
		CONNECTOR (IPI spec value)					
13	Config	Drop Cable Prop Delay					
14	Config	Foll Delay					
15	Xcvr	Receiver Prop Delay					
16	Xcvr	Receiver Jitter					
17	Xcvr	Receiver o/p Rise and Fall Time					
18	Config	Foll Delay					
19	Logic	Logic Setup/Hold					
		TOTALS					

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RJC – 5/13/87

IPI - SCSI

CLOCKING LIMIT OF IPI CURRENT MODE HARDWARE UNDER TEST

		3 sigma deviation	
cbl skew	0.15 ns/foot	36.9 ns	
driver		6 ns	
receiver		10 ns	
logic at driving end		10 ns	
logic at receiving end		10 ns	
sq. root of sum of sqs. of indep. var.			41.2 (A)
offset (note 2)		5 ns	
pattern dependent (note 2)		5 ns	
open collector (notes 1, 2)		5 ns	
inability to center clock		10 ns	
mean of logic clocking data		4 ns	
unallocated (note 3)		10 ns	
arithmetic sum of non-indep. variables			39 (B)
latch setup		30 ns	
metastability protection		10 ns	
sum of factors needed for data latching			40 (C)

MAX. (projected) DATA RATE- 10 MB/sec
1/(A+B+(C/2))

Note 1: This factor is associated with the difference in the receiver output rise and fall times due to the open collector design of the device under test (DUT).

Note 2: The magnitude of these factors assumes the clock to data alignment is adjusted to minimize these effects. The clock to data relationship for factors which are cable length dependent are optimized for the longest cable. Since the cable skew is less with short cables this technique will not present a problem in that case.

Note 3: This factor is included since the reliability of a three sigma link is not believed to be sufficient.

26 April 85 K. Moe

IPI - SCSI FF/...

May 14 1987

TO : Rick Henderson
FROM : Kumar Sivasothy

SUBJECT : Further charaterisation of the National Semiconductor DS3695 Transceiver and Madison 26AWG Cable for IPI/SCSI

We presented Driver and Receiver propagation skew numbers at the March 31 1987 working group meeting. These numbers were extremely conservative - I had allowed 3Sigma margins for individual worst case propagation delays; this implies a better than 3×10^{-12} probability for the total skew (see Footnote 1). I have re-calculated the numbers allowing 3Sigma margins for the driver skew and the receiver skew. This implies a probability better than 2×10^{-06} for the total skew. I have also taken jitter measurements for a length of 50M assuming a clock rate of 12.5Mhz (25Mbytes/s Data Transfer). We are very close to the desired transfer rate - just one or two nanoseconds above the total distortion budget. With a little adjustment to the budgets allocated to the various contributors to skew, we should meet the 12.5MHz clock rate. 25 Mytes/s over 50M seems to be what the committee is looking for. The jitter measurements are quite tedious to make and the jitter worsens rapidly for longer distances. I would prefer to leave the measurements at the longer cable distances until we sort out the 50M length.

Driver Skew (Note2)	6.0	nS
Receiver Skew (Note2)	9.0	nS
Data Dependent Jitter (Note3)	4.0	nS
Duty Cycle Distortion (Note4)	< 1.0	nS
Skew - Cable Rise Time and Receiver Offset (Note5)	3.0	nS

Other cable characteristics(50M)

Propagation Delay	263	nS
Rise Time (10%-50%)	7.0	nS
Rise Time (10%-60%)	11.8	nS
Skew between wires of the same pair	< 1.0	nS
Prop.Skew (Worst Case) between any two pairs (Note6)	8.0	nS

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Footnotes

Note 1

One-tailed 3Sigma probability = 1.35E-03
Probability(Driver Skew > 9nS) = $P(t_{PLH}<12nS)\&P(t_{PHL}>21nS)$
= 1.35E-03 x 1.35E-03
= 1.82E-06

Similarly,
Probability(Receiver Skew > 14nS) = 1.82E-06
Probability(Total Skew > 23 nS = 1.82E-06 x 1.82E-06
< 3E-12

Note 2

These numbers are based on worst case measured propagation delays. The measurements assumed a temperature difference of no more than 25 Deg.C and a supply voltage difference of no more than 200mV between any two devices on the same PC card. The numbers do not vary significantly with cable length driven or with type of load (SCSI,vs. IPI) used.

Note 3

This was measured for 50M using an isolated pulse of width. 40nS (clock) and its complement. Load was IPI 560-150-560 termination at the far end of the cable.
With the SCSI 330-150-330 termination at both ends the jitter is 6nS

Note 4

This was done with a balanced load of 150 ohm.

Note 5

This is the sum of the worst case times taken for the differential signal at the far end of the cable to swing beween 0mV and -200mV and between 0mV and +200mV. The load is the IPI load. Cable length is 50M.
With the SCSI load the skew is 4.0nS

Note 6

The sample size was 1. The worst skew measured between any two pairs was 7.6nS. The three pairs situated in the core gave the worst propagation delay skews when measured with respect to the outer pairs. The propagation delay skew between any two of the outer pairs was considerably less.

EL1

SKELETON OF FASTER SCHEME

# GROUP	DESCRIPTION	MIN	MAX	CUM
CONFIG	FOIL DELAY		1	
XCVR	TRANSMITTER PROP DELAY SKEW		6	
XCVR	FOIL AND DROP CABLE DELAY SKEW		1	
CABLE	EXTERNAL CABLE PROP DELAY SKEW		10	
CABLE	PATTERN DEPENDENT JITTER (IPI)		4	
CABLE	CABLE BALANCE		1	
CABLE/XCVR	RISETIME/VTH DEPENDENT DISTORTION		3	
CONFIG	DROP CABLE AND FOIL DELAY SKEW		1	
XCVR	RECEIVER PROP DELAY SKEW		9	
CONFIG	SET UP TIME		5	

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4.5 Electrical Requirements

4.5.1 Logic Levels

All signals on the interconnecting cables are at ECL 10K voltage levels relative to signal ground at the transmitting end.

Negative logic signal levels are used for all external signals. A logical one is defined as the more negative of the two signal levels (nominally -1.65 volts); a logical zero is defined as the more positive of the two signal levels (nominally -0.85 volts).

4.5.2 Drivers and Receivers

Differential transmission is used for all signals on the interconnecting cables. Figure 4-6 shows suggested transmitter and receiver arrangements. All signals from CRAY equipment are transmitted using a circuit equivalent to ECL type 10109. All signals to CRAY equipment are received by ECL type 10116 differential line receivers.

4.5.3 Line Termination

All lines should be terminated with 60 ohms to -2.0 volts or its Thevenin equivalent. Two acceptable termination schemes are shown in Figure 4-6.

4.5.4 Grounding

No signal ground wire nor separate ground wire is provided in the interconnecting cables. It is desirable that the devices be grounded to the same grid ground.

4.6 Cabling Requirements

One HSX Channel requires eight cables, each cable consisting of 24 twisted-pairs (four cables for input and four cables for output). Connection to each device is by means of 10-foot drop cables (connectors on one end only). Interconnection between devices is achieved using a set of eight interconnect cables. Maximum cable length is 75 feet including drop cables and miscellaneous wiring between driver/receiver circuits and cabling.

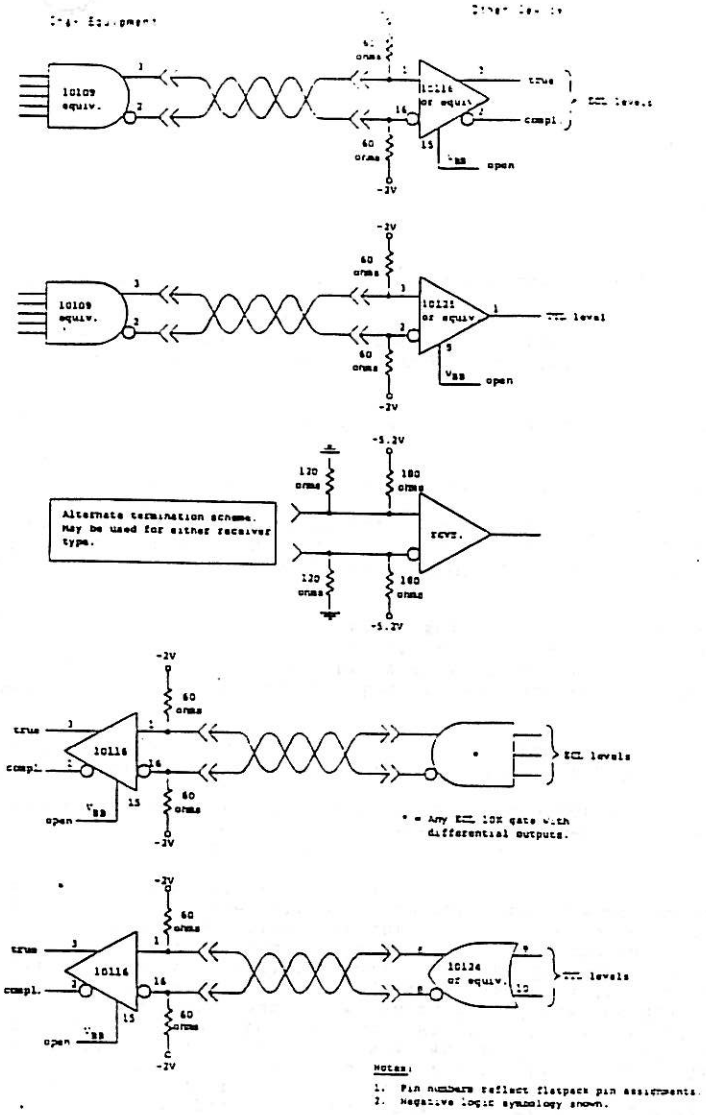

Figure 4-6. Transmitter/Receiver Circuits.

4.4.1 Cable Construction

Cables are constructed using 26 gauge wire with a characteristic impedance of 115 +/- 10 ohms (Cray Research, Inc. P/N 01109700, Brand Rex P/N 10434400 or equivalent). This cable limits signal skew to less than 3.0 nanoseconds per 100 feet.

4.4.5 Abnormal Conditions

4.4.5.1 Power Off

The voltage on both wires of a twisted pair carrying a signal to the device will be approximately zero volts. The output of a differential line receiver under these conditions is undefined.

4.4.5.2 Cable Disconnected

The voltage on both wires of a twisted pair carrying a signal to the device will assume nearly equal low logic levels determined by the line's termination network. The output of a differential line receiver under these conditions undefined.

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C CABLE SEGMENT IMPLEMENTATION

Specifications for the FASTBUS Cable Segment are given in Section 16. The following information is expected to be amplified and modified as Cable Segment implementations are developed.

Circuits which attach to the FASTBUS Cable Segment are differential current drivers. The driver circuits are designed such that in their quiescent state no current is flowing to either of the wires of a pair. A compensation circuit at one terminator sinks a current of I to bias the cable such that the '0' line is more positive than the '1' line. When a circuit drives the signal pair to the '1' state it sinks I current from the '0' line and sources a current I into the '1' line. This results in the differential voltage across the signal line changing from -0.5IRt to +0.5IRt. Rt is the value of the terminating resistor for each line, which is 0.5 the impedance of the signal pair. The voltage change is sensed by a differential amplifier attached to the signal pair. The amplifier is designed such that its output changes from a logical 0 to a logical 1 when the '1' line is more positive than the '0' line. The signal pair is biased to a voltage, Vterm, which optimizes the common mode range for the driver-receiver circuits.

Cable Segment logic states are shown in Figure C.

All drivers which attach to the FASTBUS Cable Segment shall:

a. When driving the cable to a logical zero, supply zero current ±0.01I to either side of a signal pair.

b. When driving the cable to a logical one, source a current I±0.05I to the '1' leg of the signal pair, and sink a current I±0.05I from the '0' leg of the signal pair. The difference between these currents shall not exceed 0.01I.

All receivers which attach to the FASTBUS Cable Segment shall be designed such that they develop at their output a logical one when the '1' line is more positive than the '0' line and a logical 0 when the '0' line is more positive than the '1' line. The input current shall be less than 0.3% of I on both inputs.

The common mode range for the drivers and receivers shall be as stated in Appendix C.2.

One end of the Cable Segment shall be terminated by a resistor of the characteristic impedance of the cable, Zo, across each signal line pair.

The terminator at the other end of each signal line pair of the Cable Segment shall provide a resistor of Zo/2 from each line of the signal line pair to the terminating voltage. It shall also provide a bias current through the '1' leg terminating resistor such that, when no driver on the line is active, the '1' line has a voltage equal to -0.5IZo relative to the '0' line.

The bias voltage on the signal line pairs shall be such that the drivers and receivers are operating in the middle of their common mode range.

C.1 Electrical Specification for Cable Segment

The Cable Segment shall have a characteristic impedence, Zo, between 100 and 150 ohms. The characteristic impedance of all Cables forming a given FASTBUS Cable Segment shall be the same within ±10%.

The drivers that attach to the Cable Segment shall have the following specifications:

I	= 4.0 ± 0.2 milliamperes
Driver common mode range	= ± 3.0 volts min.
Zero state current	= 40 microamperes max.
Current source sink match	= better than 1%

The receivers that attach to the Cable Segment shall have the following specifications:

Receiver input current	= 100 microamperes max.
Receiver current imbalance	= 10 microamperes max.

Figures C.1(a) and C.1(b) show suggested implementations of the circuits that may be used to drive the bus.

C.2 ECL Cable Segment Implementation

For an ECL implementation, the receivers that attach to the Cable Segment shall have the following specifications:

Common mode range	= +0.1 volt to -2.0 volts min.
Terminating voltage	= -0.9 volts

Note that the 10114 meets these receiver specifications.

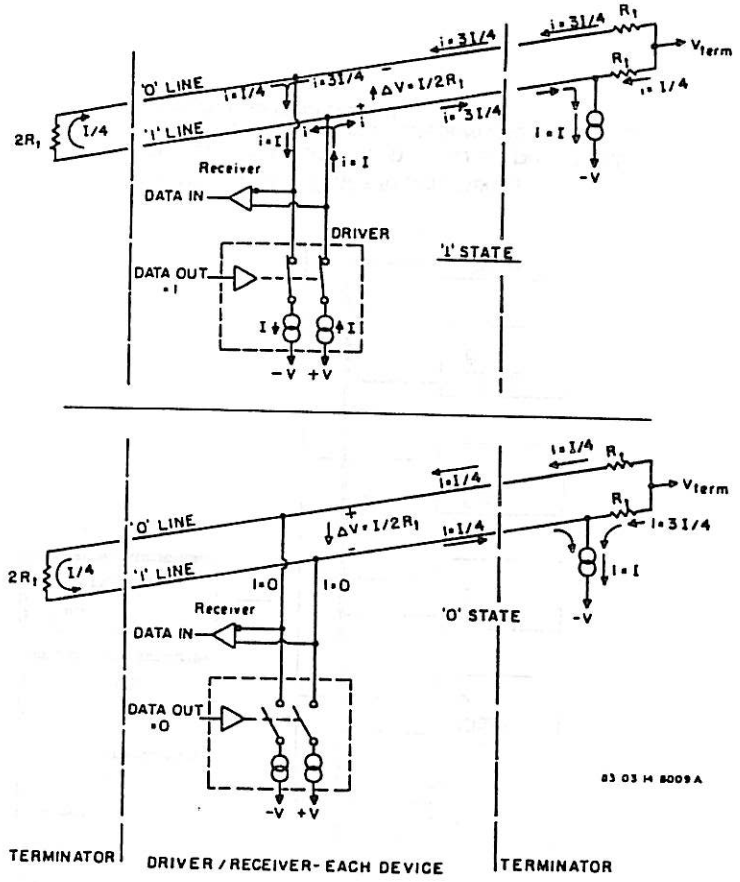


Figure C. CABLE SEGMENT LOGIC STATES
(Values of currents shown are based on zero wire resistance.)

TABLE A.I.2 CHARACTERISTIC TIMES FOR ECL IMPLEMENTATION

SEGMENT TYPE	SKEW (t_s) (MIN)	MASTER or SLAVE RESPONSE TIME OUT ** ADDRESS (MIN)	MASTER or SLAVE RESPONSE TIME OUT ** DATA (MIN)	SLAVE RESPONSE TIME ADDRESS (MAX)	SLAVE RESPONSE TIME DATA (MAX)	BROADCAST RESPONSE TIME + ADDRESS	BROADCAST RESPONSE TIME + DATA	BUS DELAY (MAX)	RB•1 (MIN)	EG DELAY TIME # (MAX)	RESPONSE DELAY TO RB•1	ARBITRATION TIME (AG•1) MIN.	ARBITRATION LOGIC DELAY (MAX.)	MIN PULSE DOWN TIME	
482.6 mm (19") CHASSIS	4 ns	900 ns	1600 ns	500 ns	1000 ns	500 ns MIN 700 ns MAX	1000 ns MIN 1400 ns MAX	15 ns	500 ns	60 ns	100 ns MIN 150 ns MAX.	150 ns**	20 ns NOTE 4	40 ns	
609.6 mm (24") CHASSIS	4 ns	900 ns	1600 ns	500 ns	1000 ns	500 ns MIN 700 ns MAX	1000 ns MIN 1400 ns MAX	20 ns	500 ns	60 ns	100 ns MIN 150 ns MAX	180 ns**	20 ns NOTE 4	50 ns	
CABLE SEGMENT	4 ns + (0.3 ns x CL) x CL) NOTES 1, 3	900 ns + (12 ns x CL) x CL) NOTES 2, 3	1600 ns + (12 ns x CL) x CL) NOTES 2, 3	500 ns	1000 ns	500 ns MIN 700 ns MAX [+(12 ns x CL)] NOTES 2, 3	1000 ns MIN 1400 ns MAX	6 ns x CL NOTES 2, 3	500 ns + (12 ns x CL) NOTES 2, 3	60 ns	200 ns MIN 300 ns MAX	100 ns** + (24 ns x CL) NOTES 2, 3	30 ns NOTE 4	40 ns + (0.6 ns x CL) NOTES 2, 3	
REF. SECTIONS		5.1.1, 5.2.3, 6 3.5	5.2.1, 5.2.3	5.1.2, 5.3.2	5.2.2	7.3				7.2	5.5.2	6.3.4 7.1.2		5.1.1 5.2.1 7.1.2 7.4	

NOTES:-
1. CABLE SKEW BASED ON 5% OF CABLE PROPAGATION DELAY.
2. BASED ON AVERAGE TWISTED PAIR WITH 5.9 ns/m; MAY BE FASTER OR SLOWER DEPENDING ON CABLE TYPE.
3. CL = CABLE LENGTH IN METERS.
4. WORST CASE DELAY AL LINE INPUT TO AL LINE OUTPUT.

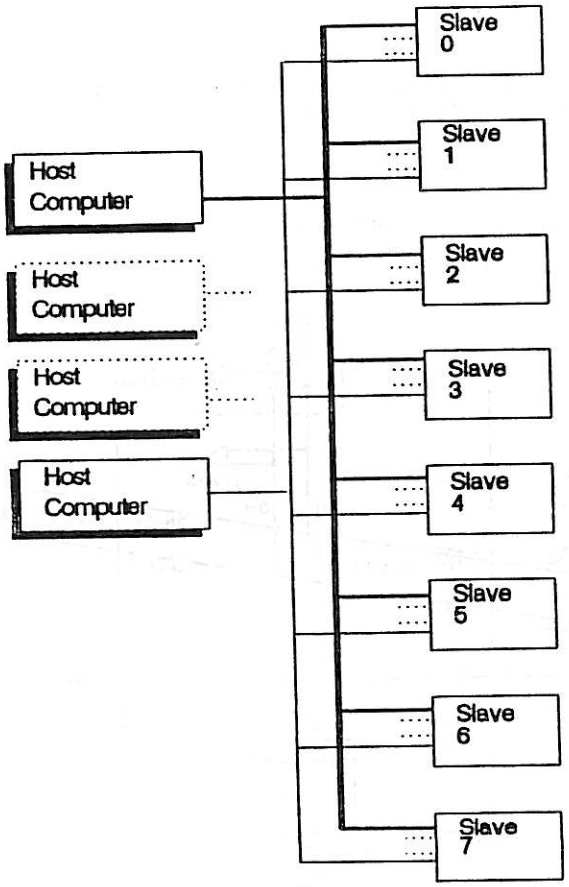
+ FOR ANCILLARY LOGIC. APPLIES FOR BOTH 0 TO 1 AND 1 TO 0 TRANSITIONS.

APPLIES FOR 0 TO 1 AND, WHERE APPLICABLE, 1 TO 0 TRANSITIONS.

FOR SPECIAL APPLICATIONS IT MAY BE POSSIBLE TO DECREASE THESE AG•1 Min TIMES.

IPI MULTIPORT INTERCONNECT

N – Port Shared Slaves



Redundent Data Paths to peripherals
Multiple Host Connection to shared peripherals
Defined as N – Port, current slave Impementations single and dual ported

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TRANSMISSION PARAMETERS

NO allowance for Stub, Crosstalk

	#	GROUP	DESCRIPTION		AVG	MIN	MAX	DIFF	
	.		Clock offset		5			5	
*	0	Config	Transmitting Logic Skew		0	0	3	3	
	1	Config	Foll Delay		1	0	1	1	
	2	Xcvr	Transmitter Prop Delay						
	3	Xcvr	Transmitter Asymmetry		16			6	
*	4	Xcvr	Transmitter Rise/Fall Time						
	5	Xcvr	~~Charge Cable Time~~						
	6	Xcvr	Bias Asymmetry						
	7	Config	Foll Delay		1	0	1	1	
	8	Config	Drop Cable Prop Delay		10	9	10	1	17
			CONNECTOR (To be spec value)						
*	10	Cable	External Cable Prop Delay		253			10	
	11	Cable	Duty Cycle ~~Jitter~~ Distortion		0			1	
	12	Cable	Intersymbol Interference Bias Distortion		0			4/3	18
			CONNECTOR (IPI spec value)						
	13	Config	Drop Cable Prop Delay		10			1	
	14	Config	Foll Delay					1	
	15	Xcvr	Receiver Prop Delay						
*	16	Xcvr	Receiver Jitter		25			9	
	17	Xcvr	Receiver o/p Rise and Fall Time						
	18	Config	Foll Delay		1			1	
	19	Logic	Logic Setup/Hold		0			5	
			TOTALS					52	17

* Items that are statistically independent

Taking square root of sum of squares saves 11 ns giving 39 ns total

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0.	Bus Control octet out delay	50	
1.	SLAVACK to BUSCTL state change	100	
2.	Transmitter delay	50	
3.	Cable delay (6.0ns/m * 25 m)	150	
4.	Receiver delay	50	
5.	Synchronization uncertainty	50	
6.	Synchronization delay	50	STTL 800ns
7.	BUSACK octet out delay	50	
8.	BUSCTL to BUSACK state change delay	100	
9.	Transmitter delay	50	
10.	Cable delay (6.0ns/m * 25 m)	150	
11.	Receiver delay	50	
12.	Synchronization uncertainty	50	
13.	Synchronization delay	50	STTL 500ns
14.	BUSACK to MASTEND state change delay	50	
15.	Transmitter delay	50	
16.	Cable delay (6.0ns/m * 25 m)	150	
17.	Receiver delay	50	
18.	Synchronization uncertainty	50	
19.	Synchronization delay	50	STTL 400ns
20.	MASTEND to SLAVACK state change delay	50	
21.	Transmitter delay	50	
22.	Cable delay (6.0ns/m * 25 m)	150	
23.	Receiver delay	50	
24.	Synchronization uncertainty	50	
25.	Synchronization delay	50	STTL 400ns
26.	DATA out delay	50	
27.	SLAVACK to TFRRDY state change delay	100	
28.	Transmitter delay	50	
29.	Cable delay (6.0ns/m * 25 m)	150	
30.	Receiver delay	50	
31.	Synchronization uncertainty	50	
32.	Synchronization delay	50	STTL 500ns
33.	TFRRDY to SLAVEND state change delay	50	
34.	Transmitter delay	50	
35.	Cable delay (6.0ns/m * 25 m)	150	
36.	Receiver delay	50	
37.	Synchronization uncertainty	50	
38.	Synchronization delay	50	STTL 400ns
39.	Master Status octet out delay	50	
40.	SLAVEND to SELECT state change delay	100	
41.	Transmitter delay	50	
42.	Cable delay (6.0ns/m * 25 m)	150	
43.	Receiver delay	50	
44.	Synchronization uncertainty	50	
45.	Synchronization delay	50	STTL 800ns
46.	Slave Status octet out delay	50	
47.	SELECT to SLAVACK state change delay	100	
48.	Transmitter delay	50	
49.	Cable delay (6.0ns/m * 25 m)	150	
50.	Receiver delay	50	
51.	Synchronization uncertainty	50	
52.	Synchronization delay	50	STTL 500ns

TTL 3.7us

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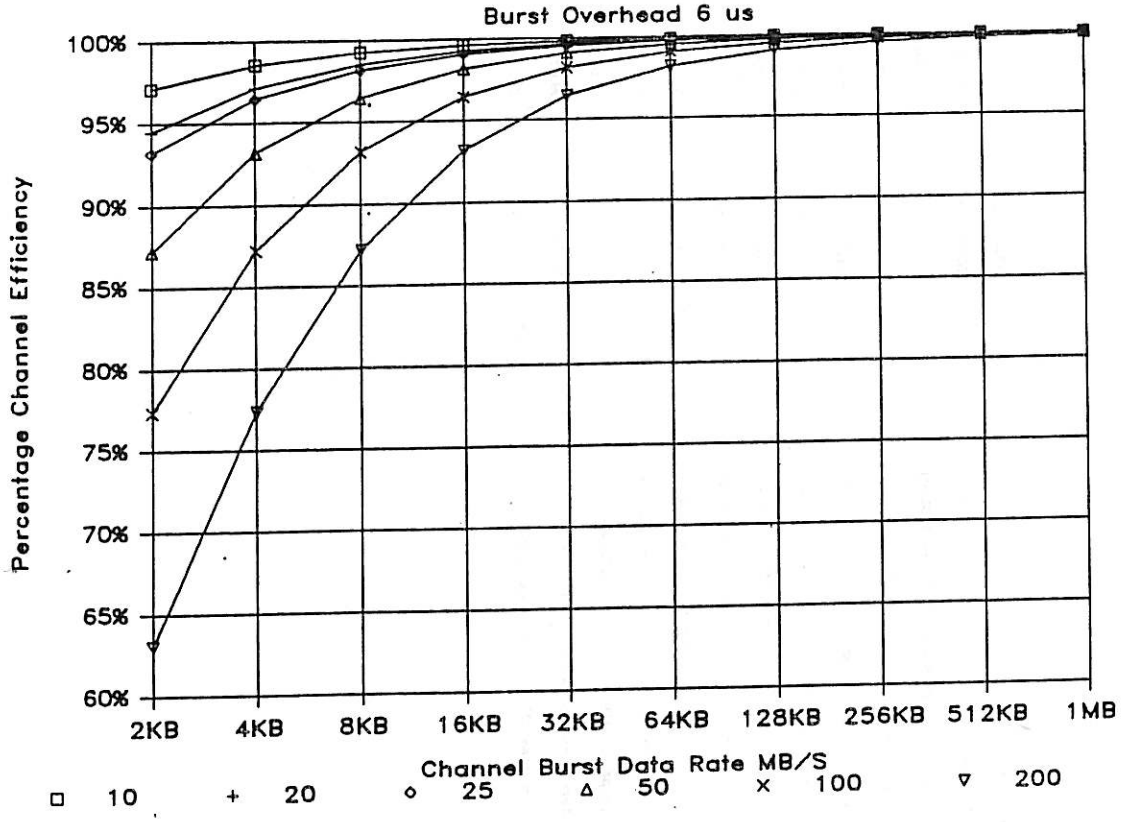
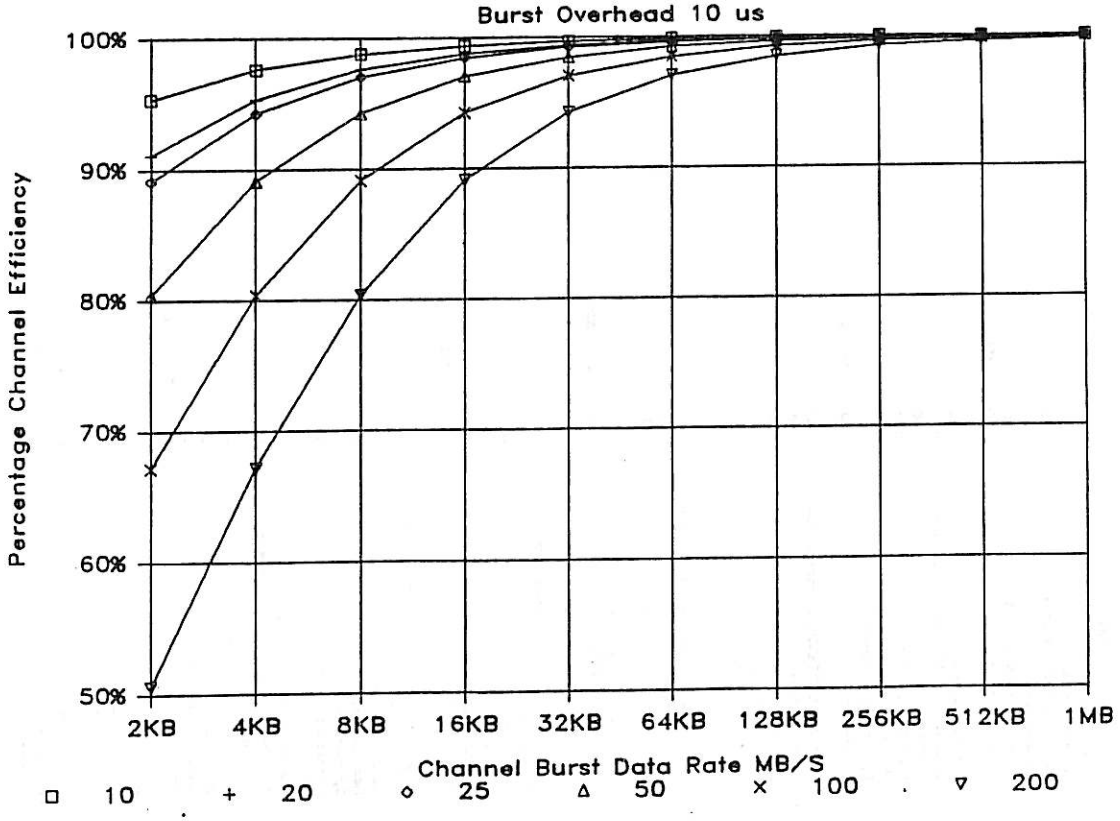
Packet size	Total Transfer Time	eff.
128 byte packet (16 quad words * 100 ns + 3700ns)	1600+3700ns	30.2%
256 byte packet (32 quad words * 100 ns + 3700 ns)	3200+3700ns	46.4%
512 byte packet (64 quad words * 100 ns + 3700ns)	6400+3700ns	63.3%
1024 byte packet (128 quad words * 100 ns + 3700ns)	12,800+3700ns	77.6%
2048 byte packet (256 quad words * 100 ns + 3700ns)	25,600+3700ns	87.4%
4096 byte packet (512 quad words * 100 ns + 3700ns)	51,200+3700ns	93.3%
8192 byte packet (1024 quad words * 100 ns + 3700ns)	102,400+3700ns	96.5%
16K byte packet (2048 quad words * 100 ns + 3700ns)	204,800+3700ns	98.2%
32K byte packet (4096 quad words * 100 ns + 3700ns)	409,600+3700ns	99.1%
64K byte packet (8192 words * 100 ns + 3700ns)	819,200+3700ns	99.6%
128K byte packet (16K words * 100 ns + 3700ns)	1,638,400+3700ns	99.8%
256K byte packet (32K words * 100 ns + 3700ns)	3,276,800+3700ns	99.9%

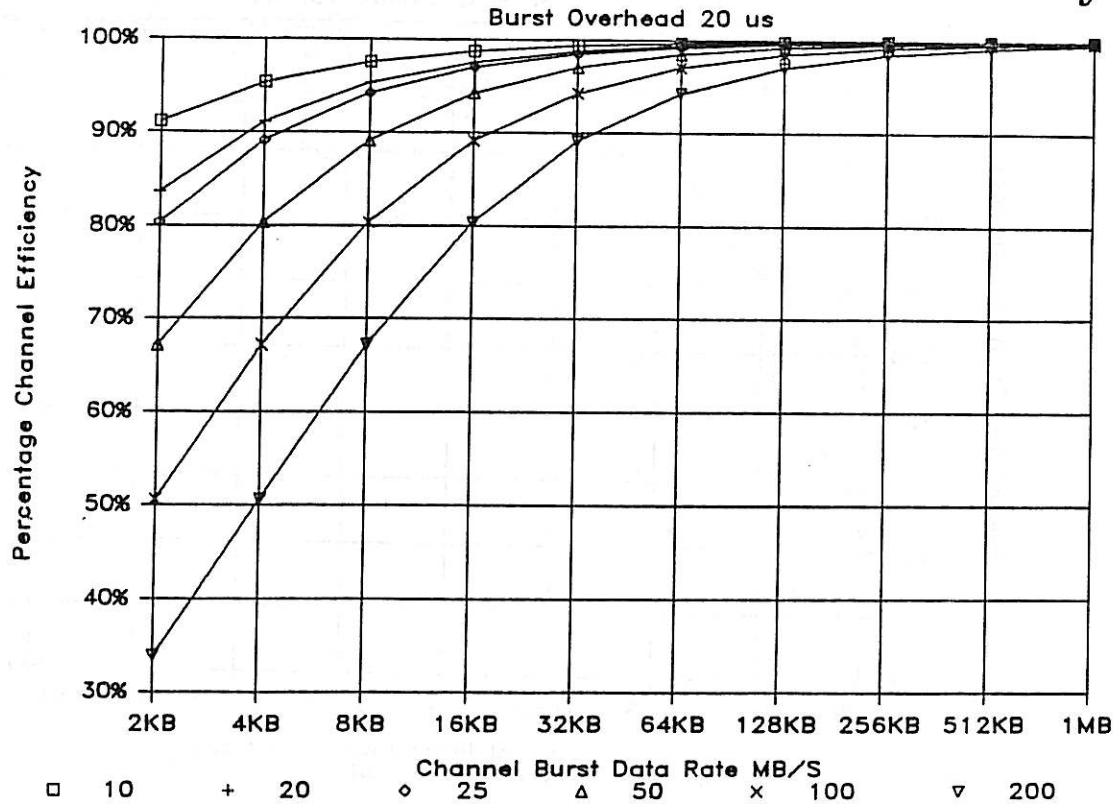
IPI Channel Data Transfer Efficiency



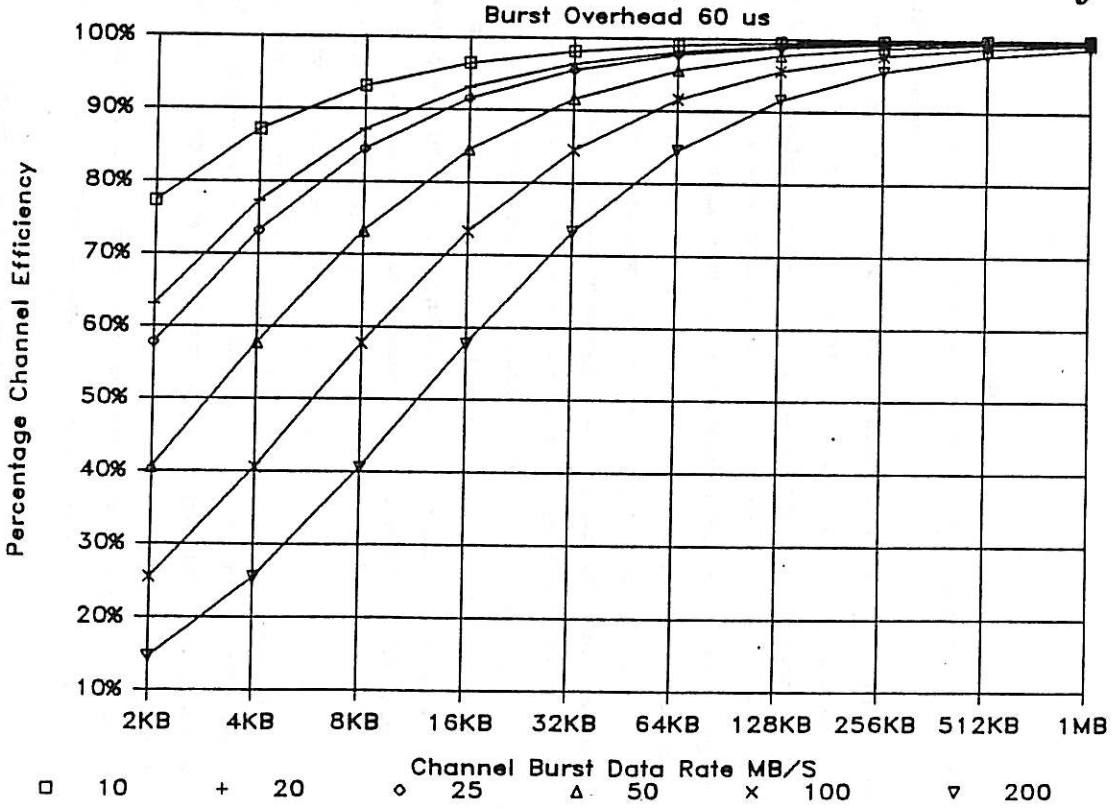
IPI Channel Data Transfer Efficiency



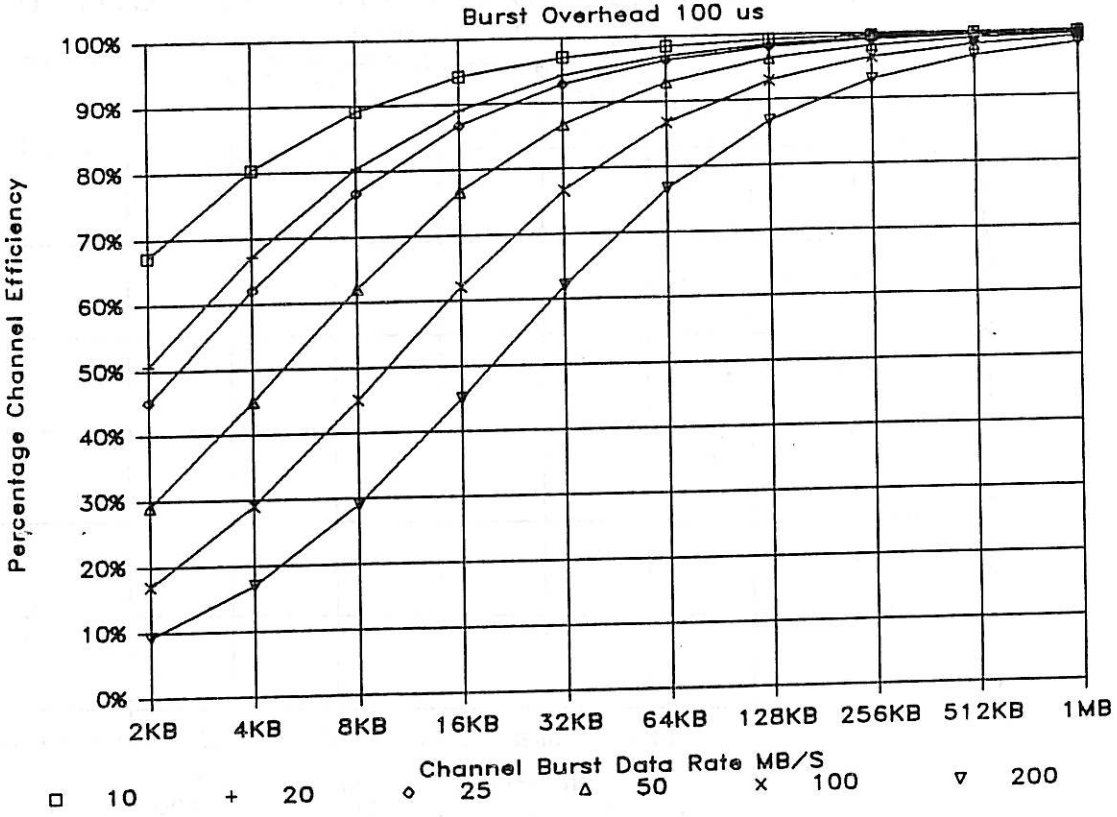
IPI Channel Data Transfer Efficiency



IPI Channel Data Transfer Efficiency



IPI Channel Data Transfer Efficiency



NEWSRELEASE

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Latest TAXI update FYI, Gryphon

FOR IMMEDIATE RELEASE

CHIP SET OFFERS BREAKTHROUGH IN HIGH-SPEED DATA TRANSMISSION

SUNNYVALE, California...May 18, 1987... A new chip set from Advanced Micro Devices offers a performance breakthrough for point-to-point data transmission applications. AMD's Am7968 TAXI Transmitter and Am7969 TAXI Receiver provide a high-speed interface at 56 megabits per second data throughput, or a 70MHz clock rate, for use over fiber optic or coaxial media. By the fourth calendar quarter, this performance will be enhanced to 100Mbps, or a 125MHz clock rate. These devices have a significant speed improvement over today's standard serial interfaces, which peak at a 10MHz clock rate.

This transparent bus interface scheme allows replacement of cumbersome ribbon cable or bundles with a single coaxial or fiber optic cable. Thus, the TAXI chip set significantly reduces wiring interconnections for point-to-point communications, essentially replacing copper with silicon. TAXI is AMD's designation for Transparent Asynchronous Transmitter-Receiver Interface.

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The Am7968 TAXI Transmitter serializes parallel data and asynchronously transfers the data stream over the media link. On the other end of this link, the Am7969 TAXI Receiver converts the serial data stream back into a parallel flow. All this is accomplished without the need for complex hardware or software protocols, easing design-in of the devices. The highly flexible TAXI chip set features 12 parallel interface pins, allowing operation with data that is 8, 9, or 10 bits wide. For very wide parallel paths, the TAXI devices can be cascaded in increments of 8, 9, or 10 bits to allow many parallel inputs to share a single serial interface.

The TAXI chip set achieves its high performance as a result of its unique

-more-

125MHz analog phase-locked-loop receiver. This allows high-speed decoding of the serial data back into a parallel flow.

The TAXI chip set is suited for use in both office and factory point-to-point communication schemes. Primary applications include point-to-point, high-speed links between computer CPUs and disk and peripheral controllers, such as printers. Other applications include links between distributed processors, as well as in communication systems, robotics, military avionics, industrial, and factory communication systems.

AMD is now sampling the Am7968/7969 TAXI chip set at a 70MHz clock rate, or 56 megabits per second data throughput rate. These devices will be available in production quantities next quarter. Higher speed versions of the devices at 100 megabits per second, or 125MHz clock rate, will be available in the fourth calendar quarter. In 28-pin cerdip packages, the 70MHz Am7968/7969 chip set is priced at $58.00 for the pair, in 100-piece quantities. The devices will be offered in plastic DIP and plastic leaded chip carrier (PLCC) packages in the fourth calendar quarter.

Advanced Micro Devices, one of the five largest U.S. manufacturers of integrated circuits, produces microprocessors, memories, telecommunications, graphics, networking, and programmable logic devices. AMD has sales offices worldwide, and has manufacturing facilities in Sunnyvale and Santa Clara, California; Austin and San Antonio, Texas; Penang, Malaysia; Manila, the Philippines; Bangkok, Thailand; and Singapore.

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For more information, please call: John Hamburger, Sunnyvale, California (408) 982-7445 or Jayshree Ullal @ 982-7138