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o: ANSI Committee X3T9.2

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ubject: Wide SCSI

In response to the action item given to us at the March working group meeting in Phoenix, we would like to submit the following text to be added to the drawings submitted at the working group, for inclusion into the SCSI II spec as an appendix.

These diagrams are intended as an architecture guide for device designers who wish to support the Wide SCSI protocol. For simplicity, only the control paths are shown. The SCSI Protocol Controller (SPC) which may be any one of several currently available chips, transfers 8 bits of data plus parity over the "A" cable. The FIFO transfers either 8 or 24 additional data bits plus parity over the "B" cable. Data is transferred via DMA to the SPC and FIFO in parallel from the memory of the controlling device. Data transfers over the "A" and "B" SCSI cables need not be simultaneous.

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INITIATOR - DATA IN

REQ(A) and ACK(A) control the transfer of bytes to the SCSI protocol controller (SPC) chip across the A cable as in 8-bit wide transfers. REQ(B) causes the data present on the B cable to be latched by the FIFO. When the SPC asserts DMA REQ and the FIFO deasserts EMPTY, indicating that both the SPC and FIFO have data, a DMA REQ is generated for the Initiator memory logic. The Initiator memory logic then asserts DMA ACK and reads one data byte from the SPC and either one or three data bytes from the FIFO in parallel. DMA ACK is sent to the Target as ACK(B) indicating that one word of data has been received across the B cable. The FIFO depth determines the maximum synchronous offset supported by the Initiator.

TARGET - DATA OUT

REQ(A) and ACK(A) control the transfer of bytes to the SCSI protocol controller (SPC) chip across the A cable as in 8-bit wide transfers. REQ(B) pulses are sent by the Target at a rate determined by CLOCK until the count limit is reached. The count limit is set to the synchronous offset value determined by the Target. ACK(B) causes the data present on the B cable to be latched by the FIFO. When the SPC asserts DMA REQ and the FIFO deasserts EMPTY, indicating that both the SPC and FIFO have data, a DMA REQ is generated for the Target memory logic. The Target memory logic then asserts DMA ACK and reads one data byte from the SPC and either one or three data bytes from the FIFO in parallel. DMA ACK causes the control counter to decrement by one, thus allowing one more REQ(B) pulse to be sent by the Target.

NITIATOR - DATA OUT

REQ(A) and ACK(A) control the transfer of bytes to the SCSI protocol controller (SPC) chip across the A cable as in 8-bit wide transfers. When the SPC asserts DMA REQ and the FIFO deasserts FULL indicating that both the SPC and FIFO are ready to receive data, a DMA REQ is generated for the Initiator memory logic. The Initiator memory logic then asserts DMA ACK and writes one data byte to the SPC and either one or three data bytes to the FIFO in parallel. FIFO NOT EMPTY allows ACK(B) pulses to be sent by the Initiator at a rate determined by CLOCK. The CONTROL COUNTER assures that the number of ACK(B) pulses sent by the Initiator will not exceed the number of REQ(B) pulses received from the Target. When the number of REQ(B) pulses received exceeds the number of ACK(B) pulses sent, COUNT=ZERO will be deasserted, allowing ACK(B) pulses to be generated. The leading edge of ACK(B), after one skew delay, causes the FIFO READ signal to be clocked, thus removing the current FIFO data from the B cable and presenting the next FIFO data.

ARGET - DATA IN

REQ(A) and ACK(A) control the transfer of bytes to the SCSI protocol controller (SPC) chip across the A cable as in 8-bit wide transfers. When the SPC asserts DMA REQ and the FIFO deasserts FULL indicating that both the SPC and FIFO are ready to receive data, a DMA REQ is generated for the Target memory logic. The Target memory logic then asserts DMA ACK and writes one data byte to the SPC and either one or three data bytes to the FIFO in parallel. FIFO NOT EMPTY allows REQ(B) pulses to be sent by the Target at a rate determined by CLOCK. The CONTROL COUNTER assures that the number of REQ(B) pulses sent by the Target less the number of ACK(B) pulses received from the Initiator will not exceed the synchronous offset limit. When the number of REQ(B) pulses sent less the number of ACK(B) pulses received equals the synchronous offset, COUNT=LIMIT will be asserted, disabling REQ(B) pulses from being generated. The leading edge of REQ(B), after one skew delay, causes the FIFO READ signal to be clocked, thus removing the current FIFO data from the B cable and presenting the next FIFO data.