X3T9.2/87-36

March 10, 1987

To: ANSI Committee X3T9.2

From: Steve Goldman
Distributed Processing Technology
132 Candace Drive
Maitland, Fl 32751
(305) 830-5522

Subject: Wide SCSI

In response to the action item given to us at the January working group meeting in Irvine, we would like to submit the following drawings for inclusion into the SCSI II spec as an appendix.

These diagrams are intended as an architecture guide for device designers who wish to support the Wide SCSI protocol. For simplicity, only the control paths are shown. The SCSI Protocol Controller (SPC) which may be any one of several currently available chips, transfers 8 bits of data plus parity over the "A" cable. The FIFO transfers either 8 or 24 additional data bits plus parity over the "B" cable. Data is transferred via DMA to the SPC and FIFO in parallel from the memory of the controlling device. Data transfers over the "A" and "B" SCSI cables need not be simultaneous.

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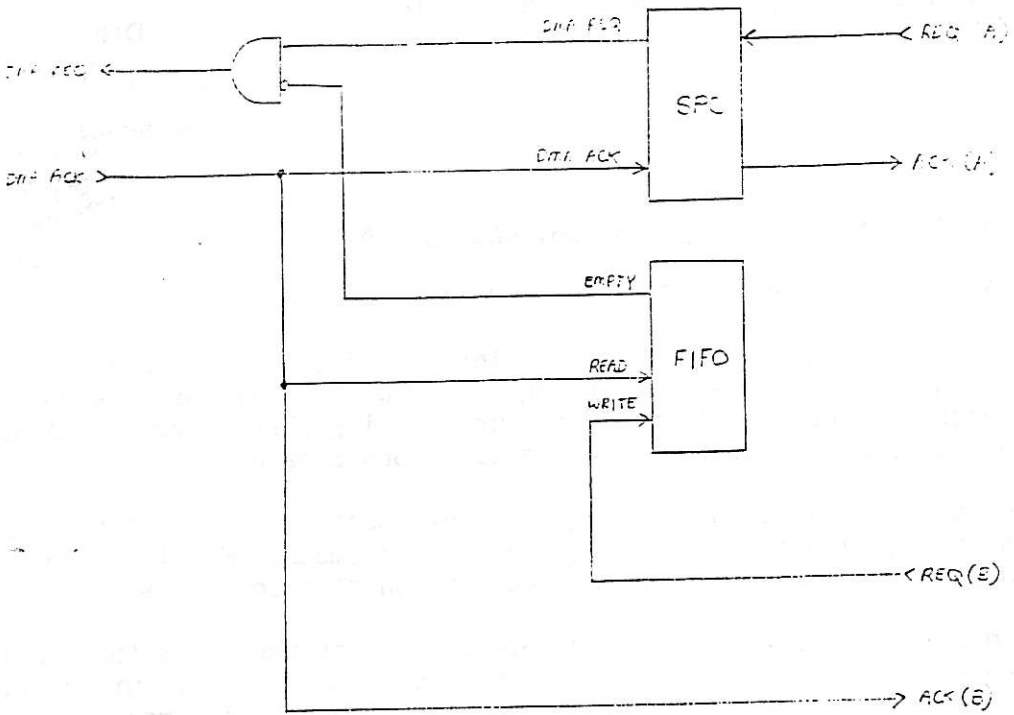

DPT Distributed Processing Technology
131 Candace Dr. • P.O. Box 1864 • Maitland, FL 32751 • Phone (305) 830-9522

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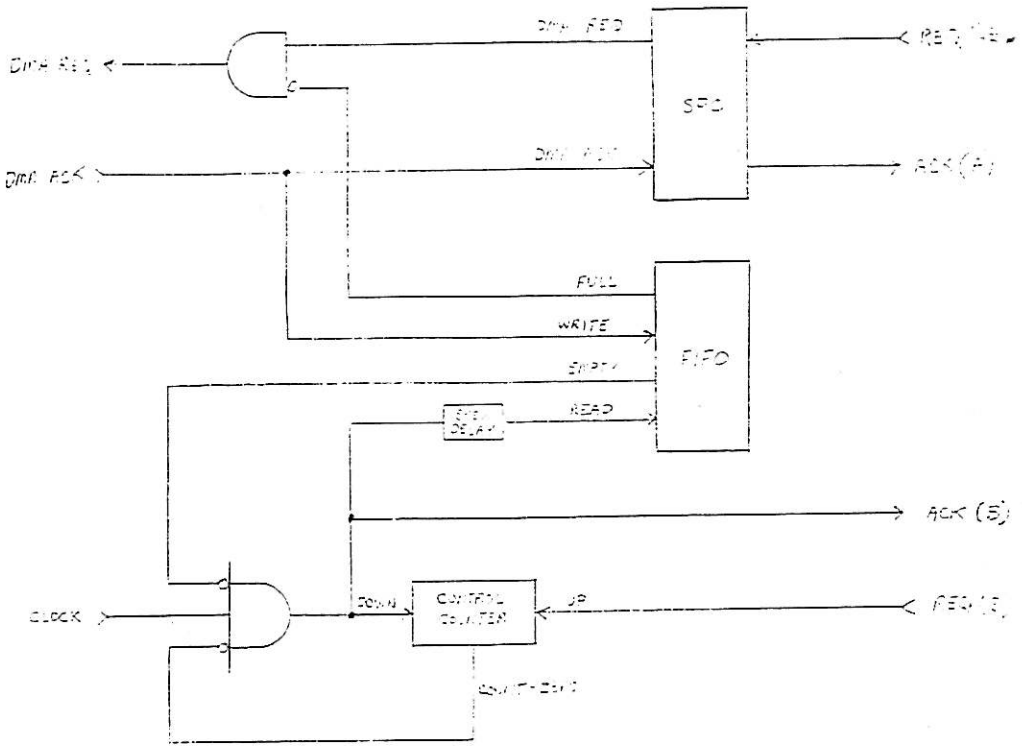

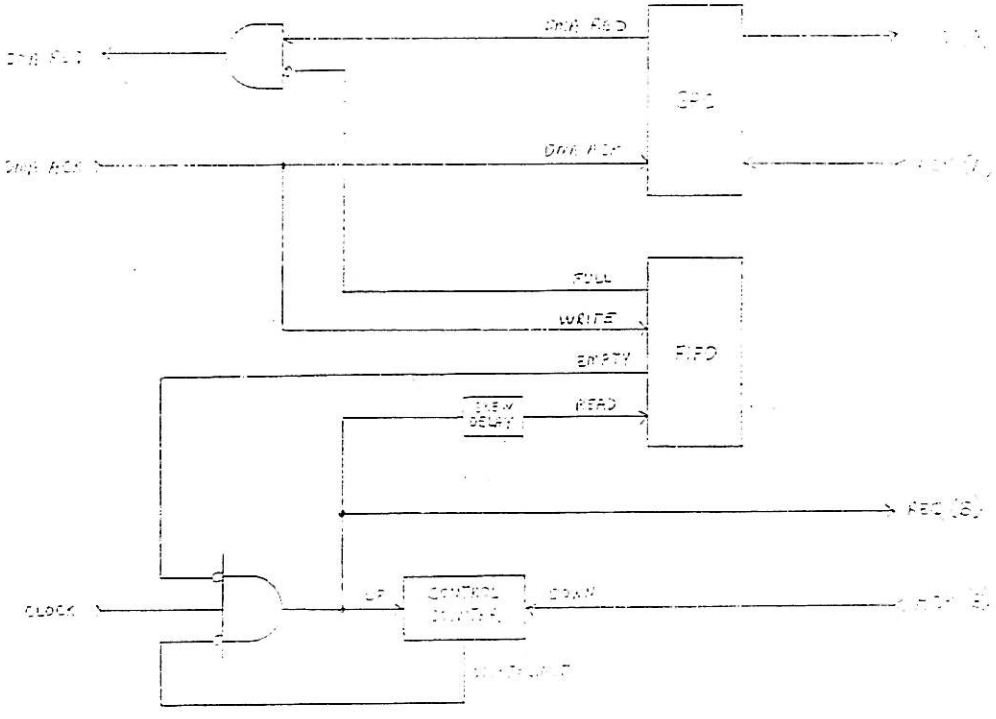

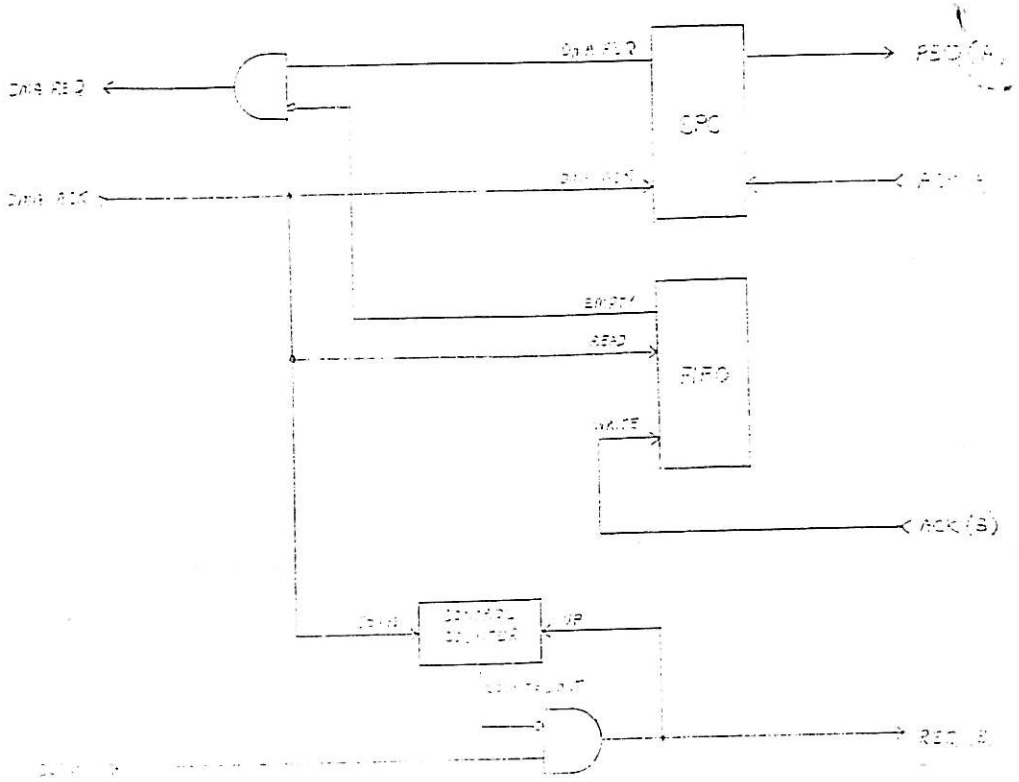
DPC
FIFO
READ
WRITE
ACK (B)