ADDRESS

X379.2/87-9 APPS -16-bit SCSI Example **Block Diagram*** Possible SCSI DMA DMA Protocol Controller Existing CONTRO Synch.SCSI Protocol SCSI Cable A Chip req(A) **FIFO** ack(A) Possible SCSI Protocol ADDRESS Controller ack(B) SCSI Cable B FIFO 8-bit Slave Data Chip By feeding back the REQ/ACK lines on the A cable the ASIC can slave itself to the intelligent controller. Due to this feedback there is no problem in achieving RAM RAM the proposed required timing.

Only immediate SCSI data paths are shown. Other elements are needed for a complete system.

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an Acknowledge on either cable.

can be asserted on either cable.

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16bit.scsi.example

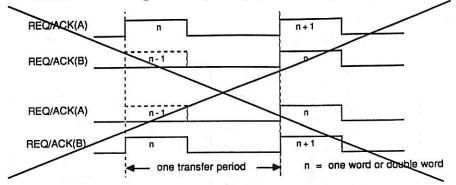
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In asynchronous mode, both Requests must be asserted before asserting

Likewise, both Acknowledges must be deasserted before another Request



16/32-bit Sync. Handshake Relative Timing of Req/Ack(A) and Req/Ack(B)



Proposed Wording to Sec. 5.1.5.3 (add to last paragraph)

In synchrenous mode both Requests for the same word or double word must be asserted within one transfer period of each other.

Likewise, both Acknowledges for the same word or double werd must be asserted within on transfer period of each other.

After considering this a bit more, I would recommend no restrictions on the timing of REQ and ACK in Synchronous mode. No significant savings in circuitry is realized by the above wording and in fact, complexity is increased.



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