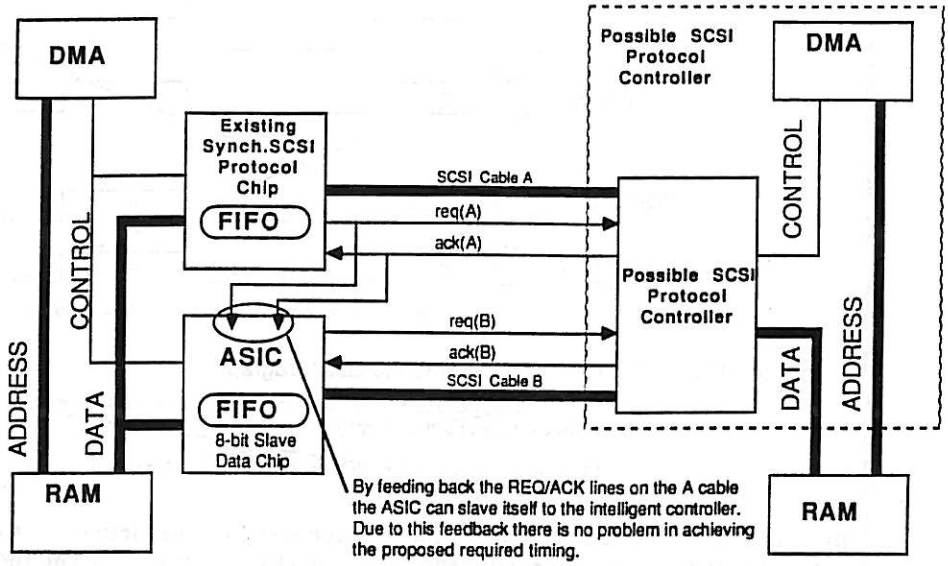
X3T9.2/87-9

APPS

16-bit SCSI Example Block Diagram*



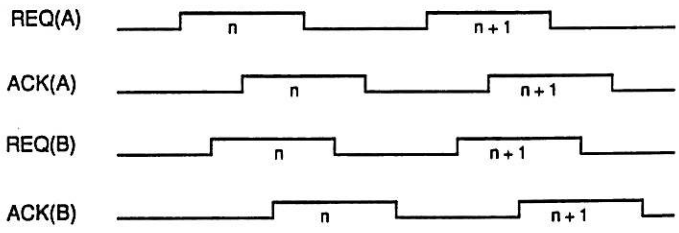
* Only immediate SCSI data paths are shown.
Other elements are needed for a complete system.

National Semiconductor

16bit.scsi.example JES 1/22/87

APPS

16/32-bit Async. Handshake Relative Timing of Req/Ack(A) and Req/Ack(B)



n = one word or double word

Proposed Wording to Sec. 5.1.5.3 (add to last paragraph)

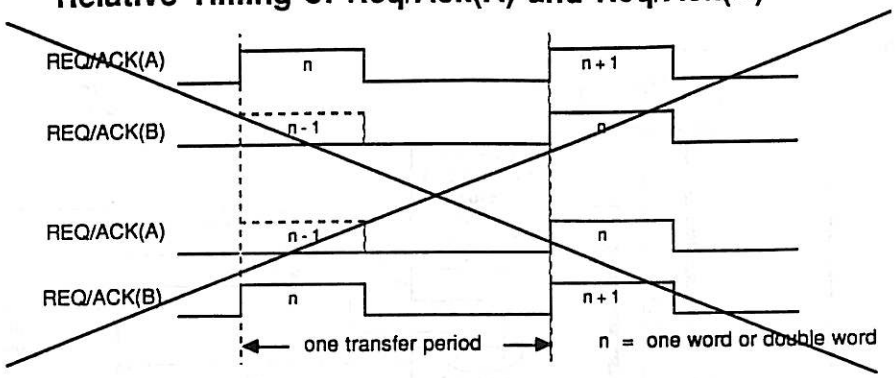
In asynchronous mode, both Requests must be asserted before asserting an Acknowledge on either cable.

Likewise, both Acknowledges must be deasserted before another Request can be asserted on either cable.

National Semiconductor

16/32bit.async.handshake JES 1/22/87

16/32-bit Sync. Handshake
Relative Timing of Req/Ack(A) and Req/Ack(B)



Proposed Wording to Sec. 5.1.5.3 (add to last paragraph)

~~In synchronous mode both Requests for the same word or double word must be asserted within one transfer period of each other.~~

~~Likewise, both Acknowledges for the same word or double word must be asserted within on transfer period of each other.~~

After considering this a bit more, I would recommend no restrictions on the timing of REQ and ACK in Synchronous mode. No significant savings in circuitry is realized by the above wording and in fact, complexity is increased.