

# American National Standard

for Information Technology

## ATA/ATAPI Host Adapters Standard (ATA - Adapter)

Corrected:

Secretariat: Information Technology Industry Council  
Page 1 of 2

Page 11 of INCITS 370-2004 ATA/ATAPI Host Adapters Standard, clause 6.6.2.5, states that bit 3 of the bus master base address register is read/write. This is incorrect. In order to obtain the proper minimum size of the bus master base address, bit 3 shall be read only. In this erratum, page 11 is reprinted with the correction.

#### 6.6.2.2 PCI Base Address Register (BAR) 1

This is the base address for the control register for ATA Channel X. Note that because of the Dword alignment of PCI, the Device Control and Alternate Status Registers are at offset 02h from this base. For example, to put those registers at address 3F6h, this register shall be set to 3F4h (+ Bit 0).

Address Offset        14h  
Default Value        00000001h

When operating in Compatibility Mode any write to the BAR shall be ignored and the value 3F5h always be used.

Attribute            Bits 31-16 may be Read Only, Bits 15-2 Read/Write, Bits 1-0 Read Only.  
Size                  32 bits

#### 6.6.2.3 PCI Base Address Register (BAR) 2

If the device implements two channels this is the base address for the command block registers for ATA Channel Y. If the device only supports one channel this base address is read only and cleared to zero.

Address Offset        18h  
Default Value        00000001h

When operating in Compatibility Mode any write to the BAR shall be ignored and the value 170h shall always be used. In Compatibility Mode an independent IRQ shall be provided that is connected to IRQ15. When the adapter is disabled by using the I/O Enable bit in the PCI Command register, the adapter shall not respond to any I/O addresses, and shall release its IRQ connections.

Attribute            Bits 31-16 may be Read Only; Bits15-3 Read/Write; Bits 2-0 Read Only.  
Size                  32 bits

#### 6.6.2.4 PCI Base Address Register (BAR) 3

If the device implements two channels this is the base address for the control registers for ATA Channel Y. If the device only supports one channel this base address is read only and cleared to zero. Note that because of the Dword alignment of PCI, the Device Control and Alternate Status Registers are at offset 02h from this base.

Address Offset        1Ch  
Default Value        00000001h

When operating in Compatibility Mode any write to the BAR shall be ignored and the value 376h shall always be used.

Attribute            Bits 31-16 may be Read Only, Bits 15-2 Read/Write, Bits 1-0 Read Only.  
Size                  32 bits

#### 6.6.2.5 PCI Base Address Register (BAR) 4

Base address of the ATA Bus Master I/O registers.

Address Offset        20h  
Default Value        00000001h

Attribute            Bits 31-16 may be Read Only, Bits 15-4 Read/Write, Bits 3-0 Read Only.  
Size                  32 bits

#### 6.6.2.6 PCI Base Address Register (BAR) 5

This is a vendor specific BAR

### 6.6.3 PCI Interrupt Line

The host BIOS and host software may use this location to store the system interrupt (IRQ) allocated to this device. The adapter does not use this information. BIOS and host software may use this location to store the information.

Address Offset        3Ch  
Default Value        00h

## 6.7 ATA Bus Master Registers

The bus master -ATA function uses 16 bytes of I/O space. All bus master -ATA I/O space registers can be accessed as byte, word, or Dword quantities. The base address for these registers is PCI BAR 4. The description of the 16 bytes of I/O registers follows: