

DRQ=0 When ERR=1 Feature and Allocation Identify Device Words Proposal

To: T13 Technical committee
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1 Introduction

Under this proposal a new Set Features function would allow a host to indicate to a device that the DRQ status bit is to be zero when ever the error bit is set to 1. This proposal also sets aside a supported and an enabled bit in new Identify words allocated for feature support/enable reporting.

2 DRQ=0 when ERR=1 Function

During the processing of a command devices set either BSY=1 or DRQ=1. DRQ=1 indicates the device is requesting data. DRQ may be asserted when an error has occurred (ERR=1). This behavior is a legacy of buffer management where parallel ATA devices would transfer data to their buffer and set DRQ before detecting the error. The recommended Serial ATA protocol is to disallow the DRQ=1 and ERR=1 condition (Design Guide 21). If this feature is implemented on a Serial ATA drive the drive is guaranteed to do the recommended behavior.

This feature allows the host to require a device to clear DRQ to zero when ERR is set to one, so the error data does not have to be transferred to end the command.

2.1 Set Feature

Table XX - SET FEATURES register definitions

Value (See note)	
5Fh	Enable DRQ bit shall be zero when ERR bit is one.
DFh	Disable DRQ bit shall be zero when ERR bit is one.

2.1.1 Enable/disable DRQ=0 when ERR=1

Subcommand codes 5Fh and DFh enable and disable the clearing of the DRQ Status Register bit to zero when the ERR bit is set to one.

For parallel ATA devices at power-on, or after a hardware reset, the feature shall be disabled. The feature setting shall be preserved over software reset.

For Serial ATA devices if this feature is supported it shall be enabled at all times. Set features codes 5Fh and DFh shall be accepted by the device without changing the behavior of the device.

3 Identify Words 119-120,

This proposal reserves words 119-120 for expansion of the feature implemented/enabled words.

3.1 Bits for DRQ=0 When ERR=1 Feature

IDENTIFY DEVICE information

Word	O/M	F/V	Description
86		F	15 Words 119-120 are valid
119		F	15-1 Reserved
		F	0 1 = Clearing DRQ bit to be always zero when ERR bit is set to one is supported
120		F	15-1 Reserved
		V	0 1= Clearing DRQ bit to be always zero when ERR bit is set to one is enabled 0= Clearing DRQ bit to be always zero when ERR bit is set to one is disabled

Add to word 86:

If bit 15 of word 86 is set to 1 words 119-120 are valid

3.1.1 Word (119) Features/command sets supported

Word (119) shall indicate features/command sets supported. If a defined bit is cleared to zero, the indicated features/command set is not supported.

If bit 0 of word 119 is set to one, the optional DRQ=0 when ERR=1 feature is supported.

3.1.2 Word (120) Features/command sets enabled

Word (120) shall indicate features/command sets supported. If a defined bit is cleared to zero, the indicated features/command set is not enabled.

If bit 0 of word 120 is set to one, the DRQ=0 when ERR=1 feature is enabled.