

Summary of Comments on d1532v3r4a

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Author: relliott

Date: 4/8/2004 10:56:50 AM

missing the ..... before the 252

Plenary Disposition: Accepted 4/20/2004 8:51:27 AM

Page: 21

Author: relliott

Date: 4/8/2004 10:57:17 AM

handling

missing . at end

Plenary Disposition: Accepted 4/20/2004 8:52:06 AM

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Author: relliott

Date: 4/7/2004 1:14:54 PM

SATA 1.0 defined the frequency skew as +350/-2650 ppm, noting it included +350/-150 ppm for the crystal and -0.25% [= -2500 ppm] fixed skew for SSC but excluded +/-0.25% [= +2500/-2500 ppm] AC modulation from SSC. That adds up to +2850/-5150 ppm.

SATA 1.0a defines the frequency skew as +/- 350 ppm for DC skew and +0/-5000 ppm for AC skew (adding up to +350/-5350 ppm). The minimum T,UI is not based on +2850, it's based on +350 ppm:

$$666.666 * (1 - .00285) = 664.76666$$

$$666.666 * (1 - .000350) = 666.4333$$

so the SATA 1.0a change makes the minimum agree.

The maximum of 670.12 ps is based on the old SATA 1.0 -5150 ppm rather than the 1.0a -5350 ppm:

$$666.666 * 1.005150 = 670.10 \text{ (SATA 1.0 maximum, with 2 fs rounding discrepancy)}$$

$$666.666 * 1.005350 = 670.23 \text{ (SATA 1.0a maximum)}$$

For SATA 1.0a and ATA/ATAPI-7, it should be 670.23 ps.

Plenary Disposition: Rejected 4/20/2004 9:03:51 AM

Determination is that the difference between proposed change and current is insignificant. Also, the direction of error is favorable. If this parameter is met, it adds additional constraint, and cannot cause functional or spec failure. The small difference in specification is insignificant and unmeasurable with today's tools. It is believed that changing the spec would cause more confusion than clarification to the specification.

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Author: relliott

Date: 4/8/2004 10:58:39 AM

Fix "Description" cell

Plenary Disposition: Accepted 4/20/2004 9:04:02 AM

Author: relliott

Date: 4/8/2004 10:58:45 AM

delete empty rows

Plenary Disposition: Accepted 4/20/2004 9:04:24 AM

Author: relliott

Date: 4/8/2004 10:58:54 AM

delete the floating -

Plenary Disposition: Accepted 4/20/2004 9:04:47 AM

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Author: relliott

Date: 4/20/2004 9:06:36 AM

delete floating [

Plenary Disposition: Accepted 4/20/2004 9:08:56 AM

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Author: relliott

Date: 4/7/2004 1:15:24 PM

ALIGNs sent by the frame transmitter are not supposed to count against this budget, although they do consume a "DWORD time."

Sending 10 data dwords, 2 ALIGNs, and 10 data dwords would technically violate the above statement but not really be an error.

Plenary Comments:

Making the proposed change would make the requirement less restrictive.

The current requirement is functional and more constraining, but not a functional issue. Recommend review in ATA-8 for improved requirements.

Plenary Disposition: Rejected 4/20/2004 9:25:53 AM

Author: relliott

Date: 4/7/2004 1:15:20 PM

HOLDS sent by the frame transmitter cannot always count against this budget.

Assume the frame transmitter is in LT4:L\_SendData and it finds it has no more data to send, so it moves to LT6:L\_SendHOLD and starts transmitting HOLDS. It remains in that state as long as it has no more data to send. If a HOLD shows up, it does not leave the state and switch to transmitting HOLDAs; it continues sending HOLDS. Only when it decides it has no more data to send does it switch states; it goes to LT5:L\_RcvrHold until the incoming HOLDS go away.

Unlike ALIGNs, the HOLDS cannot just be excluded from the budget. The frame transmitter won't ever leave the HOLD state to send a few more data dwords before sending the HOLDA in reply to a HOLD it received while it was transmitting HOLD itself; it always goes directly to sending HOLDA.

Plenary Resolution:

Add note for exception case where HOLD/HOLD condition overrides 20 DWORD times requirement and HOLDA transition:

(See figures (link xmit & Link Receive) for HOLD/HOLD transition cases that do respond with HOLDA within 20 DWORD latency times)

Status:

Plenary Disposition: Accepted 4/20/2004 9:40:20 AM

Author: relliott

Date: 4/20/2004 10:19:03 AM

The 20/20 transmit/receive rule, based on a mythical wire delay of 0, doesn't make sense. It should either be 19/20 or 20/21 (I prefer 19/20; Knut preferred 20/21). If a transmitter takes n dwords to reply to HOLD with HOLDA, the receiver is going to see the reply n + 1 dwords after it sent the HOLD, not n dwords later.

Incorporating all my comments on this page (assuming 20/21 is chosen), I suggest this text replace most of 15.4.8.1:

"Not including ALIGNs, the frame transmitter shall transmit no more than:

- a) 20 data dwords; or
- b) 20 or fewer data dwords following by one or more HOLD primitives, after receiving a HOLD primitive before transmitting HOLDA primitives.

Not including ALIGNs, the frame receiver shall accept at least:

- a) 21 data dwords; or
- b) 21 or fewer data dwords following by one or more HOLD primitives, after transmitting a HOLD primitive before expecting HOLDA primitives."

Plenary Comments:

The 20 DWORD latency requirement and example includes margin and allows for a certain amount of uncertainty. The requirement, although not precise, is not considered to be technically challenging and examples are provided so that designs are not constrained unnecessarily.

Plenary Disposition: Rejected 4/20/2004 10:22:29 AM

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Author: relliott

Date: 4/8/2004 10:49:59 AM

PMNACK should be PMNAK

Plenary disposition: Global change OK

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Author: relliott

Date: 4/8/2004 10:50:10 AM

PMNACK should be PMNAK

Author: relliott

Date: 4/8/2004 10:50:49 AM

PMNACK should be PMNAK

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Author: relliott

Date: 4/8/2004 10:50:32 AM

PMNACK should be PMNAK

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Subject: Note

Date: 4/20/2004 12:24:46 PM

delete extra period

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Subject: Note

Date: 4/20/2004 12:36:26 PM

Change first sentence to: This state is entered when the byte count for the DRQ data block is reached (see 16.5.7.3)