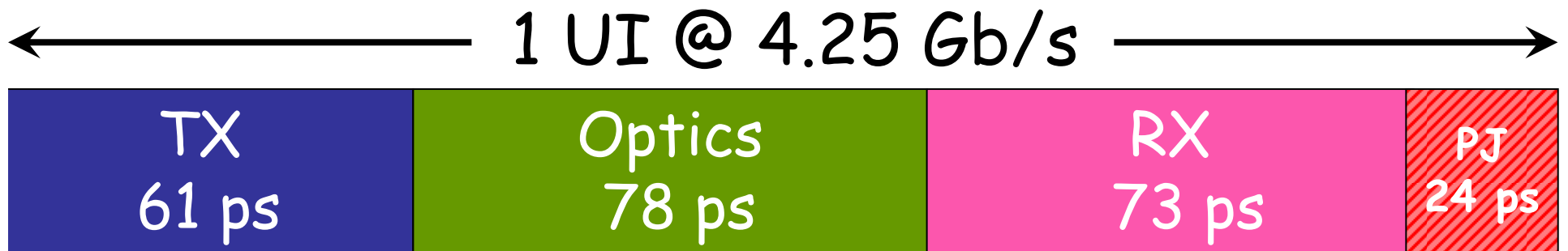


Evolving the 8GFC Delta Point
Budget from 4GFC:
not just "divide by 2"

Mike Jenkins

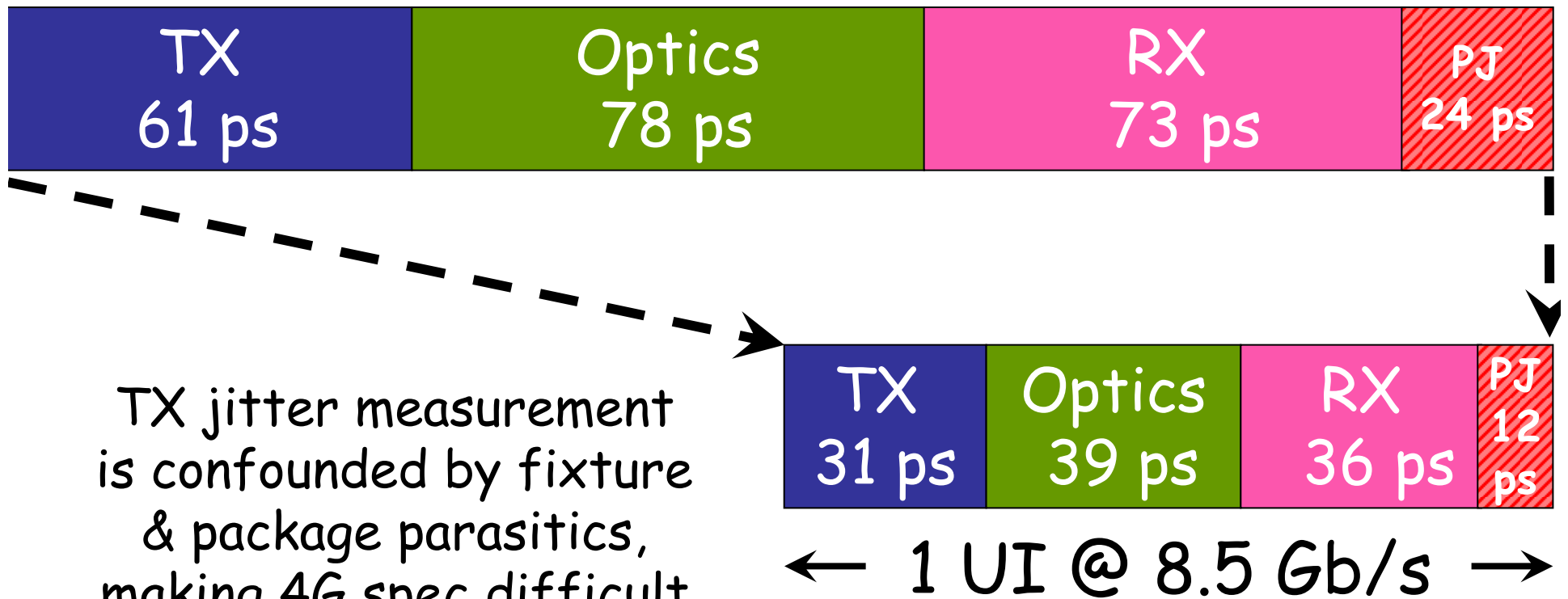


4GFC Delta Point Jitter Specs



- **TX** portion is max allowed jitter
- **Optics** portion is max allowed jitter addition on top of max allowed TX jitter
- **RX** portion is worst case eye opening

Just divide all values by two??

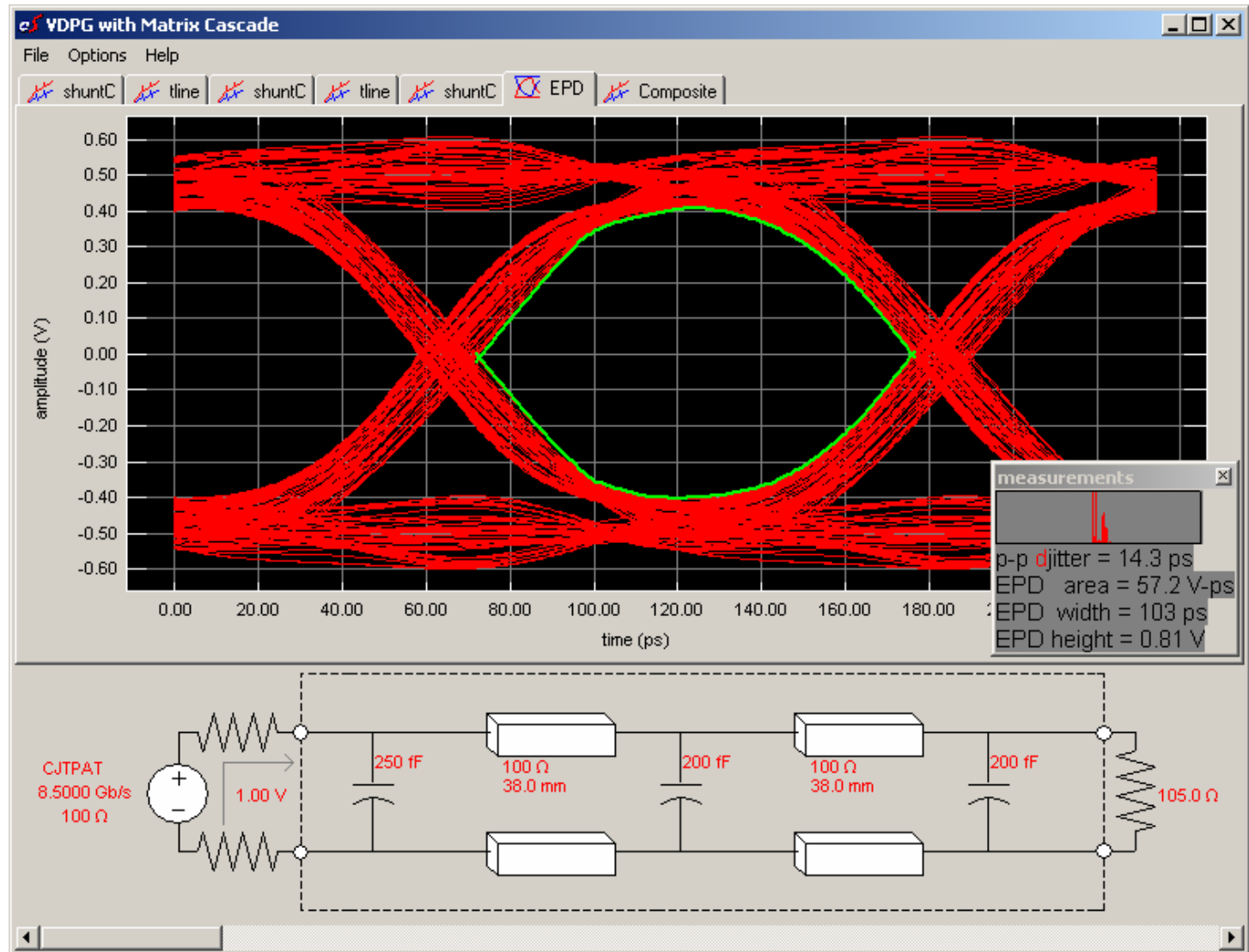


TX jitter measurement is confounded by fixture & package parasitics, making 4G spec difficult and 8G spec *extremely* problematic

A Perfect 8GFC TX falls victim to packaging parasitics...

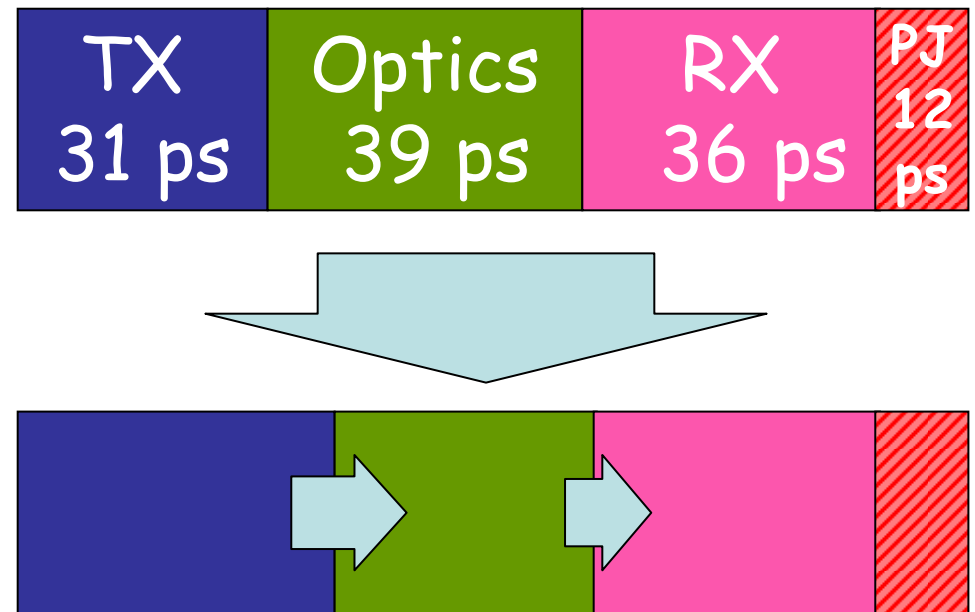
This 8GFC TX has ZERO intrinsic jitter.

However, realistic packaging adds over 14 ps of ISI jitter.



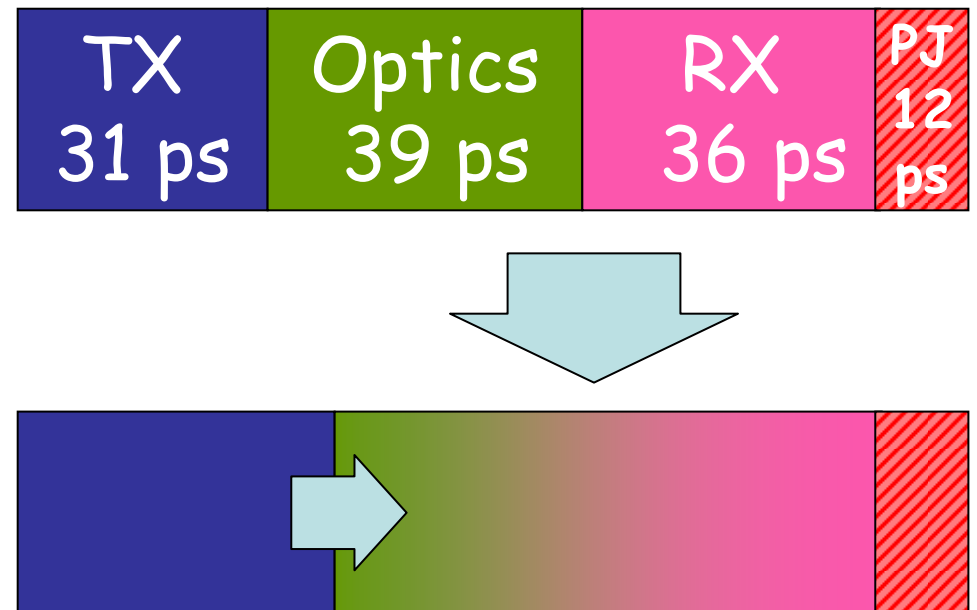
One Alternative: *Lean to the Right*

- New adaptive RX architectures may need a smaller slice of the pie
- Fiber optic xcvrs appear to have more than adequate budget



Another Alternative: Merger

- Fundamental problem is *three* separate jitter domains sharing *one* budget
- Adaptive RX designed for equalizing long PCB traces might also be used to equalize linear optical output (i.e., provide EDC)



Summary

- Moving from 4.25G to 8.5G, TX jitter spec is becoming increasingly difficult compared with Optics & RX budgets
 - TX needs larger budget (in UI) for 8GFC
- SFP+ with *linear RX output* using host SerDes RX to provide EDC function collapses two jitter budgets into one, freeing up more budget for TX