

Calibration and Verification of Jitter Measurement Devices

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The purpose of this paper is to describe how to calibrate and verify the jitter measurement device (JMD) and associated test setup has a proper response to jitter and SSC.

Discussion

In serial interfaces with embedded clocks, a clock must be derived from the data stream at the receiver. A definition of jitter must define this clock and its response to jitter at all frequencies. This clock, the reference clock, provides the distinction between Spread Spectrum Clocking (SSC) and jitter, tracking low frequency modulation and SSC and eliminating the spread spectrum frequency modulation from the jitter measurements.

Devices that implement the reference clock need to be verified for proper operation and calibrated if necessary. The verification process is done by measuring the response of the jitter measurement device (JMD) to known stimuli. The JMD is calibrated by adjusting it to provide the proper response for three conditions: the attenuation, bandwidth, and peaking.

Phase Locked Loop Clock Recovery

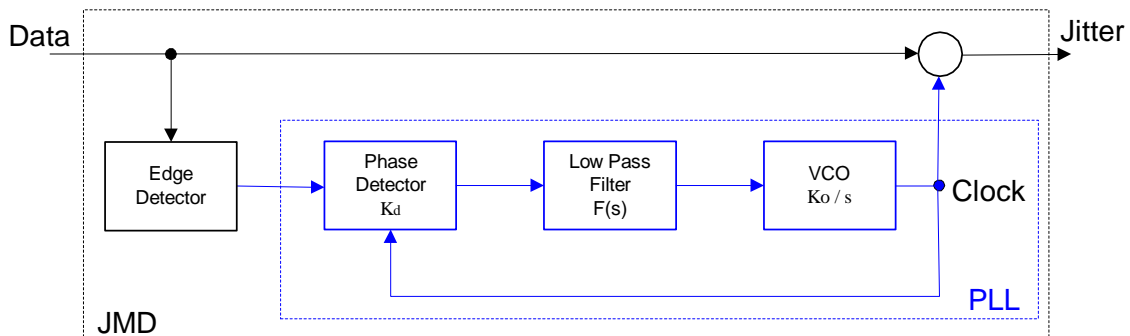
A Phase Locked Loop (PLL) is a common way of achieving the clock recovery with an appropriate jitter rejection and SSC and low frequency tracking. To achieve this separation, at least two poles at or near the origin are necessary; such a PLL is called type 2. A PLL is a feedback control device with an open loop gain, and a closed loop gain. A type 2 PLL has an open loop gain with two poles at the origin and a compensating zero for stability (see Chapter Two: Loop Fundamentals, page 11, 14, and 24 of "Phaselock Techniques" 2nd edition by Gardner ISBN 0-471-04294-3 copyright 1979). The open loop gain of any PLL is

$$G(s) = \frac{K_o K_d F(s)}{s}$$

The closed loop gain is a function of the open loop gain. This is what the specification defines.

$$H(s) = \frac{G(s)}{1 + G(s)}$$

In many Jitter Measurement Devices (JMD) the Reference Clock is not observable, the closed loop response cannot be measured, hence the JMD cannot be verified against the specification requirements. However, JMDs measure jitter and that is observable.



The response to jitter, the jitter transfer function is

$$J(s) = 1 - H(s)$$

A type 2 PLL has loop filter gain of

$$F(s) = K_f \frac{s + \omega_z}{s}$$

Define the loop gain as

$$K = K_o K_d F(0)$$

From this the type 2 PLL closed loop response is, showing two parameters to set to achieve a 3dB point, the loop gain and the zero position.

$$H(s) = \frac{K}{\omega_z} \frac{(s + \omega_z)}{s^2 + \frac{K}{\omega_z} s + K} = K \frac{\left(1 + \frac{s}{\omega_z}\right)}{s^2 + \frac{K}{\omega_z} s + K}$$

The closed loop response expressed as a 2nd order system (servo terminology) is

$$H(s) = \frac{\omega_n^2 \left(1 + \frac{s}{\omega_z}\right)}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

where the natural frequency is

$$\omega_n = \sqrt{K} = 2\omega_z \zeta$$

and the damping ratio is

$$\zeta = \frac{\sqrt{K}}{2\omega_z} = \frac{\omega_n}{2\omega_z}$$

and the jitter response is, showing two parameters to set, the loop gain and the zero position.

$$J(s) = 1 - H(s) = \frac{(s + 2\zeta\omega_n - \omega_n^2)s}{s^2 + 2\zeta\omega_n s + \omega_n^2} = \frac{s^2}{s^2 + \frac{K}{\omega_z} s + K}$$

The bandwidth of the closed loop response is the solution to

$$20\log(|H(s)|) = 20\log\left(K \frac{\left(1 + \frac{s}{\omega_z}\right)}{s^2 + \frac{K}{\omega_z}s + K}\right) = 3$$

the jitter transfer magnitude response is

$$20\log(|J(s)|) = 20\log(|1 - H(s)|) = 20\log\left(\frac{s^2}{s^2 + \frac{K}{\omega_z}s + K}\right)$$

From this discussion, both the closed loop response (specification definition) and the jitter transfer (experimentally observable) are set by the loop gain and zero position and the definition of a type 2 PLL. To achieve a reproducible jitter transfer function, the important parameters to control are the loop gain and the zero position.

The test procedure sets the loop gain and zero position to achieve a consistent response to jitter and SSC in the test setup. Proper operation of the test setup is verified by observing its response to jitter.

Data Transition Density

The response of the PLL also changes with the number of data transitions that appear—this is called the “transition density”. The phase detector provides a phase (time) difference each time a data edge appears. When more data edges appear, more corrections result. As a result, the phase detector gain K_d changes proportionally with transition density, as does the loop gain K . In the type 2 PLL, the loop gain is falling at 20dB/decade at unity gain crossover and in the region where the jitter transfer 3dB point occurs. So the jitter transfer 3dB point varies proportionally with data transition density.

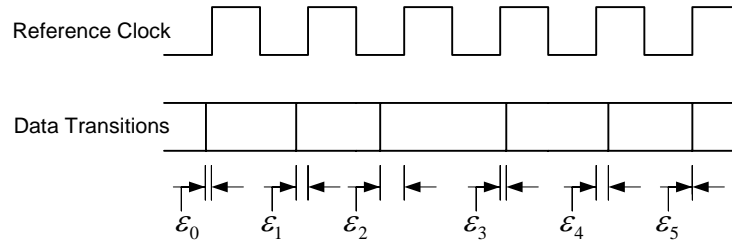
The bandwidth variation of a PLL can be examined through an analysis of the PLL as an estimator of time (phase). To do this, a description of jitter is required. Consider the times when the clock edges occur. A perfect clock has edges that occur at multiples of a given period T , and each clock edge is identified by an integer index. The times of ideal clock edges is expressed by

$$t_c(i) = iT$$

Data transitions always occur on a clock edge. Ideal data transitions occur at the same times as clock edges. In real systems, the data transitions do not occur at ideal times. The time error from ideal of the data transitions is called the "jitter". This is expressed by

$$t_D(i) = iT + \varepsilon_i$$

where the ε_i are time deviations from ideal, the clock to edge jitter. This is depicted below.



The response time of the PLL is in the microseconds because the bandwidth is in the megahertz. Over this time interval, thousands of bit transitions occur, hence the loop converges to a long term average. Over a time interval of tens of bits, the action of the PLL on the time deviations or error ε_k tends to simply average the error.

For a 01010101 signal with 5 bits and errors at each data edge, the PLL correction is

$$\sum_{i=0}^4 \frac{\varepsilon_i}{5} = \Delta t$$

For a signal with a run length of 5, there are only two data transitions and the phase detector gain and PLL bandwidth are lower. The error is still averaged with a lower scaling factor since not as many edges are present.

$$\frac{\varepsilon_0 + \varepsilon_4}{5} = \Delta t$$

Suppose it was desired the bandwidth be constant over data transition density. In a practical phase detector, this would require the error in the 5th bit be amplified. The first bit could not be amplified as well since the PLL is causal.

$$\frac{\varepsilon_0 + 4\varepsilon_4}{5} = \Delta t$$

Each timing error ε_k is no more an indicator of the true data transition time than another. So, the error in Δt would be greater since the error term ε_4 is weighted too heavily; it is best the error be weighted equally. Hence, the PLL as an estimator of time (phase) is better when the PLL bandwidth changes with data transition density.

Calibration

Calibration of the response to known jitter levels of a Jitter Measurement Device (JMD) is calibrated and verified in two frequency bands. The lower frequency band is at the fundamental of the SSC (30 KHz) and the second higher frequency band is in the transition region between the reference clock tracking and not tracking the jitter (around 2.6 MHz). The reference clock is part of the JMD and may be implemented in hardware or software. By calibrating the JMD to these two bands, the response to jitter is calibrated and allows for improved correlation among JMDs.

The lower frequency band requirement is tested with a 3Gb/s D24.3 pattern on which 20.8 ns p-p sinusoidal phase (time) modulation at 30 KHz is added. The ratio of the reported jitter to the amount actually applied (measured independently) is the attenuation and must meet the -73.5 dB requirement.

The specification defines two parameters related to SSC, f_{baud} the baud rate or 3GHz, and SSC_{tol} the spread spectrum modulation deviation. The frequency deviation (of the clock in the data source) is related to the spread spectrum modulation (SSC) frequency deviation by

$$\Delta f = SSC_{tol} f_{baud}$$

The sinusoidal phase modulation is related to frequency modulation by

$$\Delta f = f_m \Delta \phi$$

where Δf is the frequency deviation in Hz, f_m is the modulation frequency in Hz, and $\Delta \phi$ is the phase deviation in radians.

The phase deviation is related to the phase modulation in time by

$$\Delta \phi = 2\pi f_{baud} \Delta T$$

From these relationships, an expression for the SSC frequency deviation from the JTF test parameters is given, calculated for the test conditions and shown to be within the specification limits.

$$SSC_{tol} = 2\pi f_m \Delta T = 2\pi (30 \cdot 10^3) (20.83 \cdot 10^{-9}) = 3926 \text{ ppm}$$

From these calculations, either frequency or phase modulation may be used. A separate means of verifying the level of the modulation is used to make sure the test conditions are correct. The independent separate means of verification of the 30kHz test signal is equivalent to a frequency demodulator or wide range phase demodulator; realizations of this are: time interval error plot with constant frequency clock on a real time oscilloscope, equivalent time oscilloscope, and frequency demodulator.

Two tests are performed in the upper frequency band. The adjustment of the -3 dB bandwidth of the JTF (2.6 MHz) and the verification of the peaking (3.5 dB maximum). Both of these tests use a 3Gb/s D24.3 pattern with sinusoidal periodic phase modulation, or periodic jitter (PJ) that has been independently verified to produce 100 ps +/- 10% p-p consistently over a frequency range of 0.5 MHz to 50 MHz. In both tests a 0 dB reference level is initially determined so all other measurements are relative to this level, not the absolute level of the source. It is important that the PJ source level does not vary in amplitude over this test range, or the variation must be extracted in the final calculations.

For the tests in the upper frequency band it is necessary to have a phase or jitter modulator. The independent separate means of verification of the 2.6MHz and 50MHz test signals is equivalent to a deterministic jitter measurement with constant clock; realizations of this are: time interval error plot with constant frequency clock on a real time oscilloscope, equivalent time oscilloscope with histogram and constant frequency clock, bit error rate tester (BERT) and constant frequency clock, or spectral analysis with the Bessel expansion of angle modulated sidebands (see "Precision Jitter Transmitter", Agilent applications note).

There are two typical JMD adjustments for clock recovery: "loop BW" and another known as "peaking" or "damping" or ζ . These adjustments may refer to the closed loop response or be specific to a particular design, so they cannot be used directly to ensure the JTF response to jitter. It is suggested that the "loop BW" be adjusted initially (with the "peaking" fixed) and if both

the low frequency band requirements and the high frequency band requirements can not both be simultaneously be met, the “peaking” be adjusted to modify the JTF shape in the upper band. In the case of hardware based reference clocks, moderate levels of “peaking” may be required to achieve the proper attenuation at 30 KHz. The “peaking” setting is usually specific to the JMD. With software based clock recovery, the suggested starting “peaking” level or “damping” may be low, close to the critically damped condition of $\zeta = 0.707$.

The test sequence for all measurements also removes the baseline deterministic jitter, DJ of the source and JMD such that what is being measured is the reported jitter only due to the added test jitter and not any baseline residual jitter in the test system. This is important to insure the accuracy of the measurement at low reported jitter levels.

Test Procedure

Resource requirements:

Pattern Generator for SAS signals
Sine wave source, 30kHz, and 0.5MHz to 50MHz.
Test cables
Jitter Measuring Device

The response to jitter of the Jitter Measurement Device (JMD)(the reference clock is part of the JMD) is measured with three different jitter modulation frequencies corresponding to the three cases: 1) SSC (full tracking) 2) jitter (no tracking) 3) the boundary between SSC and jitter. The jitter source is independently verified by separate means. This ensures the jitter response of the JMD is reproducible across different test setups.

The three test signals are: 1) a 1.5GHz +/- 0.01% square wave (which is a D24.3, 00110011 pattern) with risetime longer than 0.25UI 20 to 80% with a sinusoidal phase modulation of 20.8nS +/- 10% peak to peak at 30kHz +/- 1%. 2) a 1.5GHz square wave with a sinusoidal phase modulation of 100pS +/- 10% peak to peak at 50MHz +/- 1%. 3) a 1.5GHz square wave with no modulation.

An independent separate means of verification of the test signals is used to make sure the level of the modulation is correct.

The test procedure checks two conditions: the JTF attenuation and the JTF bandwidth. Care is taken to minimize the number of absolute measurements taken, making most relative; this reduces the dependencies and improves accuracy.

1. Adjust the pattern generator for a 6Gb/s D24.3 pattern (00110011, with a risetime within specified limits) modulation to produce a 30 KHz +/- 1%, 20.8 ns p-p +/- 10% sinusoidal phase modulation.
2. Verify the level of modulation meets the requirements and record the p-p level, **DJSSC**. The independent separate means of verification of the 30kHz test signal is equivalent to a frequency demodulator or wide range phase demodulator; realizations of this are: time interval error plot with constant frequency clock on a real time oscilloscope, equivalent time oscilloscope, and frequency demodulator.
3. Apply test signal to the JMD. Turn off the sinusoidal phase modulation. Record the reported DJ, **DJSSCOFF**.
4. Turn on the sinusoidal phase modulation. Record the reported DJ, **DJSSCON**.
5. Calculate and record the level of measured DJ by subtracting the DJ with modulation off from DJ with modulation on, **DJMSSC = DJSSCON - DJSSCOFF**. Calculate the jitter attenuation by $20\text{Log}(\text{DJMSSC} / \text{DJSSC})$. This value must fall within the range of – 73.5dB +/- 3dB. Adjust the JMD settings to match this requirement.

6. Adjust the pattern generator for a 6Gb/s D24.3 pattern (00110011) and modulation to produce a 50 MHz +/-1%, 0.3 UI p-p +/- 10% (100pS) sinusoidal phase modulation, also known as periodic jitter, PJ.
7. Verify the level of modulation meets the requirements and record the p-p level, **DJM**. The independent separate means of verification of the 50MHz test signal is a jitter measurement by separate means from the JMD under calibration; realizations of this are time interval error plot with constant frequency clock on a real time oscilloscope, equivalent time oscilloscope with histogram and constant frequency clock, bit error rate tester (BERT) and constant frequency clock, or spectral analysis.
8. Apply test signal to the JMD. Turn off the sinusoidal phase modulation. Record the reported DJ, **DJMOFF**.
9. Turn on the sinusoidal phase modulation. Record the reported DJ, **DJMON**.
10. Calculate the difference in reported DJ for these two cases, **DJMM = DJMON - DJMOFF**. Calculate the -3dB value: **DJ3DB = DJMM * 0.707**
11. Adjust the frequency of the PJ source to 2.6MHz. Measure the reported DJ difference between PJ on versus PJ off **DJ = DJON - DJOFF** and compare to the (DJ -3dB) value, **DJ3DB**. Shift the frequency of the PJ source until the reported DJ difference between PJ on versus PJ off is equal to (DJ -3dB). The PJ frequency is the -3dB BW of the JTF; record this value **F3DB**.
12. Adjust the JMD settings to bring the PJ -3dB frequency to 2.6MHz +/- 1MHz. Repeat step 4 through step 12 until both the jitter attenuation and 3dB frequency are in the acceptable ranges.
13. Check the peaking of the JTF. Adjust the pattern generator for a 6Gb/s D24.3 pattern and modulation to produce sinusoidal phase modulation (PJ) at the -3dB BW frequency found above, and 0.3 UI p-p +/- 10% (100pS). Increase the frequency of the modulation to find the maximum reported DJ; it is not necessary to increase beyond 20MHz. Measure the reported DJ difference between PJ on versus PJ off, **DJPK = DJPKON - DJPKOFF**. Record this DJ difference (**DJPK**) and frequency, **F3PK**.
14. Calculate the JTF Peaking value: $20\text{Log}(\text{DJPK} / \text{DJMM})$. Record this value.