To: **T10 Technical Committee/SPI-4 Working Group**
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FAST-160 Phase Encoded Data Enabling

Proposal 99-262 describes a method of using a free running clock and enabling valid data with the P1 signal. In that proposal, the P1 signal represents the transfer enable as a simple NRZ signal.

This proposal describes a method for enabling data using a free-running clock and a phase encoded enable signal. The proposal does not replace 99-262 but is intended to complement it.

Advantages:

1) Allows transitions of the enable during training packets. This allows the data enable signal to be trained as well as the data signals.
2) This proposal addresses the issue of how to recognize the start and stop of a training packet, which 99-262 did not.
3) For future speed increases in SCSI, where ISI on the data enable signal may be a concern, phase encoding reduces ISI by limiting the maximum run length.

Methodology:
In free-running clock mode, the transmitter will assert REQ/ACK (depending on direction) as a free running clock and P1 as the data transfer enable.

At the beginning of each DT DATA IN or DT DATA OUT phase that uses a free-running clock, there is a clock start-up state, during which the free-running REQ or ACK runs for several cycles with no data and with P1 negated.

A training pattern state is started by the sending device by asserting the P1 signal simultaneously with the first word of the training pattern (corresponding to the leading edge of REQ or ACK that starts the training pattern). The P1 signal is alternately asserted for two transfer periods and negated for two transfer periods during the training pattern. The training pattern must be an even number of words in length. The minimum length of the training pattern is not specified in this proposal but it is expected that SPI-4 will include a specification for this length. Since the sending device (particularly if it is an initiator) may not have data ready to send by the end of the training pattern, the sending device may extend the training pattern until it has data ready. The receiving device may optionally ignore the training pattern after it has received the minimum length.

At the end of the training pattern, a valid data state begins. The sending device indicates this state by reversing the phase of the P1 signal; i.e., by withholding the next transition of P1 during the first two transfer periods of valid data. Beginning with the third valid data word, P1 is toggled every two transfer periods during valid data. The minimum duration of the data valid state is two transfer periods, and the data valid state must last an even number of transfer periods.

Figure 1 illustrates the initial clock start-up period, training pattern and start of valid data for DT DATA IN phase.

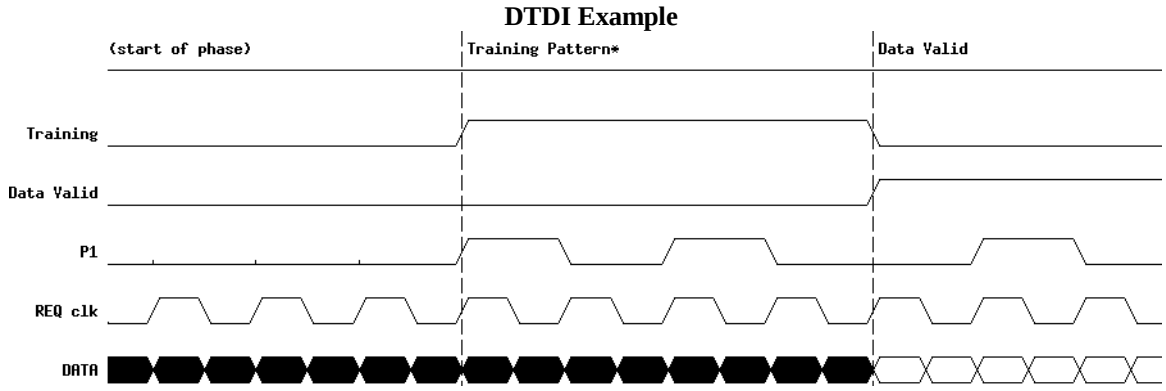

*Figure 1 (*note: number of idle and training pattern cycles TBD)*

If the sending device pauses from sending data, it again reverses the phase of P1 by withholding P1 transitions for the first two transfer periods that do not have valid data. Beginning with the third transfer period without valid data, P1 is toggled every two transfer periods until valid data is sent. The data invalid state must have at least one transition of P1 before changing states. Thus, the minimum data invalid time is 4 data transfer periods. This ensures a maximum run length of three cycles for P1. The data invalid state must last an even number of transfer periods.

From the data invalid state, the sending device may resume sending data by reversing the phase of P1 again.

Figure 2 illustrates a sequence of alternating data valid and data invalid states for DT DATA IN phase.

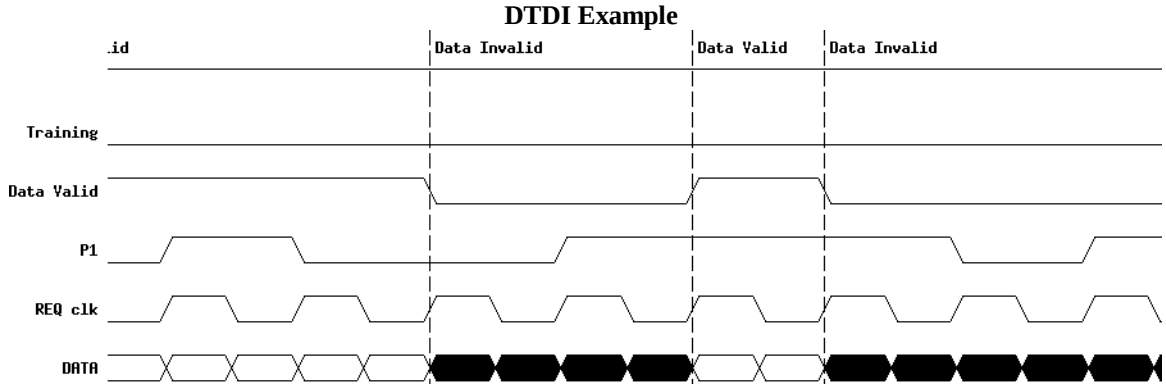

Figure 2

P1 has the same transmit setup and hold time requirements as data and is always detected by the receiving device on the leading edge of the clocking REQ or ACK signal. Since these setup and hold time requirements have not been determined yet, Figures 1 and 2 show P1 and DATA transitions to be simultaneous with REQ transitions.

NOTE: A variation has been suggested to align P1 transitions with the trailing edge of REQ or ACK instead of the leading edge. This scheme is not recommended in the present proposal. The proposed scheme of aligning P1 with the leading edge of REQ or ACK is consistent with the method used for parallel CRC signaling via P_CRCA. P_CRCA is transitioned at the same time the transmitted information switches from valid data to pad or CRC bytes, and from CRC bytes to valid data.