To: **T10 Technical Committee/SPI-4 Working Group**
From: **Gary Dickinson, Greg Goodemote, Chuck Micalizzi, and Richard Moore**
QLogic Corporation
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FAST-160 Phase Encoded Data Enabling

Proposal 99-262 describes a method of using a free running clock and enabling valid data with the P(1) signal. The method described in 99-262 helps to eliminate ISI on the REQ/ACK signals, but does not address the possible ISI on the enable signal itself.

This proposal describes a method for enabling data using a free-running clock and a phase encoded enable signal.

Advantages:

1) Phase encoded data transfer enabling extends ISI protection across both data transfer control signals while adding minimal impact to existing designs.
2) Training packets are more effective if the enable signal is de-skewed with respect to the free-running clock and data. This can be achieved with phase encoded data transfer enabling by allowing transitions of the enable during training packets.

Methodology:
In this mode, the transmitter will assert REQ/ACK (depending on direction) as a free running clock and P(1) as the data transfer enable (XFR_ENABLE). When the free-running clock starts to transition in DT data phase, XFR_ENABLE will transition at one-half the rate of the clock. This will begin the training pattern. The transmitter shall signal to the receiver that data is valid by not transitioning ENABLE for 2 clocks. This will result in a phase shift in XFR_ENABLE, and the receiver shall accept data until another phase shift occurs on XFR_ENABLE. Each transition of XFR_ENABLE will enable 2 edges of the free-running clock, making the minimum transfer length equal to 4 bytes.

DTDI Example

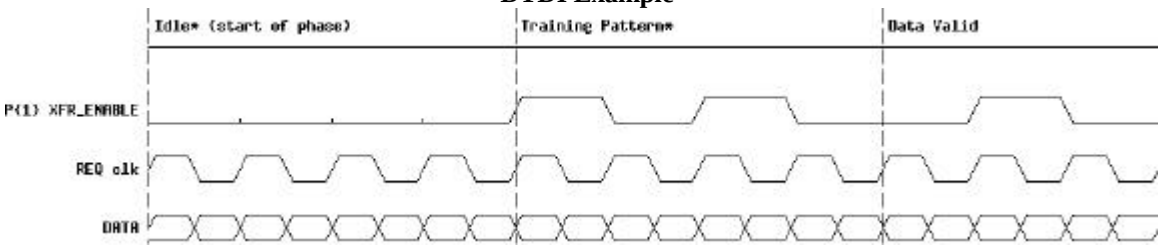

*Figure 1 (*note: number of training pattern cycles TBD)*

The Data Invalid State must have at least one transition of XFR_ENABLE before changing states. Thus, the minimum Data Invalid time is 2 cycles, whereas the minimum Data Valid time is 1 cycle. Therefore, the maximum run length of XFR_ENABLE is three cycles.

DTDI Example

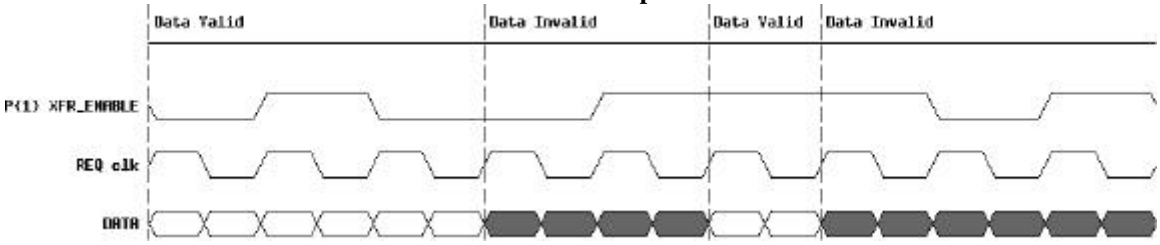

Figure 2