SPI-3 Revision 10 Letter Ballot Comments
28 October 1999
by Rob Elliott, Compaq Computer Corporation

All page numbers refer to the printed page number, not the PDF page number.

The first three comments need to be addressed to change the NO vote to a YES vote.

CPQ 101
Page 085 Section 9.1 Table 32

The receive assertion period and receive negation period at fast-80 DT are too large. The transmitted values are 11.5 ns. The receive values are 10 ns. Over a variety of backplanes, an achievable number is 8.5 ns. The periods with P_CRCA transition should be similarly reduced by 1.5 ns.

The slower rates are acceptable as is. The new timing values would be:

	fast-10DT	fast-20DT	fast-40DT	fast-80DT
Receive assertion period	80	40	20	~~10~~ **8,5**
Receive negation period	80	40	20	~~10~~ **8,5**
Receive assertion period with P_CRCA transitioning	85,5	48	32,5	~~22,5~~ **21**
Receive negation period with P_CRCA transitioning	85,5	48	32,5	~~22,5~~ **21**

CPQ 102
Page 100 Section 10.2.2

Compaq has some old devices that respond to single-bit selections. These devices might think they are being selected during the QAS force BUS FREE algorithm described. These changes should help:

> 1) Perform a QAS arbitration;
> 2) on winning QAS arbitration, assert SEL while asserting only the initiator's own ID on the data bus;
> **2.5) wait a bus settle delay;**
> **2.6) if BSY is detected true within a selection abort time, send an INQUIRY command to the target. The target should force a BUS FREE after completing the command;**
> **2.7) if BSY is detected false throughout the selection abort time, release SEL and the data bus;**
> ~~3) after detecting BSY false, release SEL and the data bus; and~~
> 4) after a bus settle delay from SEL and BSY false, the bus is in BUS FREE phase. The initiator may then arbitrate using a normal arbitration and perform a selection if it wins.

CPQ 103
Page 258   Section L.2.2 and L.5

Remove the paragraph "During these tests, the application client should prevent other processes from using the SCSI device. The application client should use the RESERVE command to prevent other initiators from altering the data buffer in the target". This topic is covered by section L.5 Buffer Protection.

Change L.5 as follows:

The READ BUFFER and WRITE BUFFER commands access physical buffers in the target. Many implementations do not protect the buffer contents if there is an intervening command from any other process. Therefore, the application client should ensure that no other SCSI processes are active while performing tests.

~~The RESERVE command may be used to block commands from other initiators. However, using the RESERVE command is not sufficient to prevent commands from the same initiator (possibly issued by other processes) from corrupting the buffer contents. Also, targets with multiple logical units may corrupt the buffer if commands are processed on other logical units.~~

The READ BUFFER and WRITE BUFFER commands include an echo buffer option that ~~may be especially valuable when performing these tests~~*provides buffer protection in multi-initiator environments.~~.~~ Other mechanisms that may help prevent buffer corruption in multiple initiator environments are RESERVE/RELEASE and linked commands.*

The remaining comments are not required to be addressed to convert the vote to a YES.

CPQ 104
Page xxii Section Introduction

Second line: remove "typically"

CPQ 105
Page 001 Section 1

Third line: end with a colon
First b) and c): remove commas after each "SCSI-2" (3 times)

CPQ 106
Page 001 Section 1

Formatting is different between the first a) b) list and the second a) b) c) d) list. The first style seems prevalent in the rest of the document, although the second is more readable.

CPQ 107
Page 002 Section 1

Change "Fiber" to "Fibre" (2 times)

CPQ 108
Page 003 Section 2.2

Add SCC to the approved references list (referred to on page 165)

CPQ 109
Page 020 Section 4.8.2.1   Second paragraph

If the number of the bytes in the data field is 3, there should not be a pad. This doesn't match "is not a multiple of 4." Something like this text would clarify the description:
    The number of bytes in the data field shall be even. An unused byte in the data field may be indicated by the IGNORE WIDE RESIDUE message.

CPQ 110
Page 042, 045 Section 5.4.1 and 5.4.2 Tables 5 and 8

Change "DB((15)" to "DB(15)"

<u>***CPQ 111***</u>
Page 050 Section 6.3.10

Change header "Cross talk" to "Crosstalk"
Change "3.0" to "3,0"

<u>***CPQ 112***</u>
Page 075 Section 7.4.2 Note 15

Change "fast-40" to "fast-40 or fast-80" (2 times) or "rates faster than fast-20"

<u>***CPQ 113***</u>
Page 079 Section 8.2

The P_CRCA signal definitions are still confusing. Also, the signal is valid in SELECTION phase which is not mentioned. I suggest a hierarchical description.

> **P_CRCA (PARITY/CRC AVAILABLE).** A signal indicating either parity or CRC available based on bus phase and negotiated settings. This uses the same line as the DB(P0) signal in previous versions of this standard.

> > **SELECTION phase,**
> > **ST DATA phase,**
> > **COMMAND phase,**
> > **MESSAGE phase,**
> > **STATUS phase. Referred to as DB(P_CRCA).** A signal sourced by the SCSI device driving the data bus during these phases. This signal is associated with the DB(7-0) signals and is used to detect the presence of an odd number of bit errors within the byte. The parity bit is driven such that the number of logical ones in the byte plus the parity bit is odd.

> > **DT DATA phase (data group transfer enabled).   Referred to as P_CRCA.** A signal sourced by a target during DT DATA phases to control whether a data group field is a pad field, pCRC field, or data field (see 10.5.2.2.2). When asserted the data group field shall be pad or pCRC fields that shall not be transferred to the ULP. When negated the data group field shall be a data field that shall be transferred to the ULP.

> > **DT DATA phase (information unit transfers enabled). Referred to as P_CRCA.** During DT DATA phases, while information unit transfers are enabled, a signal sourced by a target that shall be continuously negated by the target and shall be ignored by the initiator.

<u>***CPQ 100***</u>
Page 079 Section 8.2

The P1 signal definitions are still confusing. Also, the signal is valid in SELECTION phase which is not mentioned. I suggest a hierarchical description.

> **P1 (PARITY 1).** A signal normally sourced by the SCSI device driving the data bus. This uses the same line as the DB(P1) signal in previous versions of this standard.

> > **SELECTION phase,**

COMMAND phase,
MESSAGE phase,
STATUS, phase,
ST DATA phase (8-bit transfer width). Referred to as DB(P1). A signal that shall not be driven by any SCSI device.

DT DATA phase. Referred to as P1.   A signal sourced by the SCSI device driving the data bus during ST DATA phases. This signal is associated with the DB(15-8) signals and is used to detect the presence of an odd number of bit errors within the byte. The parity bit is driven such that the number of logical ones in the byte plus the parity bit is odd.

DT DATA phase.   Referred to as P1. A signal that shall be continuously negated by the SCSI device driving the DB(15-0) signals and shall be ignored by the SCSI device receiving the DB(15-0) signals during DT DATA phases.

CPQ 114
Page 078-079 Section 8.2

The order of the signals is not obvious. Consider one of these options:
a) alphabetical order
b) create a hierarchy
        OR-tied signals (BSY SEL RST)
        Target-driven (CD IO MSG REQ)
        Initiator-driven (ACK ATN)
        Initiator or target-driven (DB, P_CRCA, P1)

CPQ 115
Page 081 Section 8.3.2. Figure 43

Change "Signaling sense" to "LVD signaling sense"

CPQ 116
Page 082 Section 8.5 Table 29

Init note: change "this signal" to "the signal"
Targ note: change "If the signal is driven, it shall" to "If driven, the signal shall" to match the Init note wording
PT note: Change "Target that initiated" to "The signal shall be driven by the target that initiated"

CPQ 117
Page 083, 084, 085 Section 9.1, Tables 30, 31, 32

Add a column named "Type" that indicates whether the number is a minimum or maximum value. The text usually clarifies the type, but it would be helpful if it were mentioned in the table.

All types would be minimums except for these maximums:

        Table 30. bus clear delay, bus set delay, cable skew, data release delay, power on to selection, QAS assertion delay, QAS release delay, reset to selection, selection abort time
        Table 31. cable skew, signal timing skew, transmit req(ack) period tolerance.
        Table 32. cable skew, signal timing skew, transmit req(ack) period tolerance.

(Note: another comment discusses whether the tolerances should be minimums or maximums)

Page 089 Section 9.2.34

Currently, "Signal Timing Skew" is a superset of another entry in the table, "Cable Skew." Page 96 and 97 (figures 49 and 50) contain further definitions for these terms:
> Signal timing skew includes cable skew and signal distortion skew
> Signal distortion skew includes ISI (intersymbol interference) and signal crossing time through the receiver detection range

I suggest creating a new timing value called "Signal distortion skew" and simplifying the Signal Timing Skew definition to refer to the two components.

These are the values for Signal distortion skew that would go in the tables (calculated as Signal Timing Skew minus Cable Skew):
> table 31: 4 ns/4ns/4ns/2ns/2ns
> table 32: 22,8 ns/10,4ns/4,2ns/0,85ns

The type would be "max" for the Type column recommended by a previous comment.

Remove the notes from the figures 49 and 50 since they are redundant.

New and modified text:
> **9.2.xx Signal Distortion Skew**
> The maximum skew allowed from intersymbol interference (ISI), transmission line reflections, and signal crossing time through the receiver detection range.
>
> Intersymbol interference causes skew when transferring random data in combination with interruptions of the REQ (ACK) signal transitions (e.g., pauses caused by offsets).
>
> The receiver detection range is the part of the signal between the "may detect" level and the "shall detect" level on either edge. (see 9.3)
>
> **9.2.34 Signal Timing Skew**
> The maximum signal timing skew consists of cable skew plus signal distortion skew.
> ~~The maximum signal timing skew occurs when transferring random data and in combination with interruptions of the REQ (ACK) signal transitions (e.g., pauses caused by offsets). The signal timing skew includes cable skew (measured with 0101... patterns) and signal distortion skew caused by random data patterns and transmission line reflections as shown in figure 44, figure 45, figure 46, and figure 47.~~
> ~~The receiver detection range is the part of the signal between the "may detect" level and the "shall detect" level on either edge. (see 9.3)~~

Page 088, 089 Section 9.2.25, 9.2.40

The definitions for transmit and receive REQ(ACK) period tolerance do not agree on minimum/maximum wording:

Transmit: The maximum tolerance that a SCSI device may subtract from the REQ (ACK) period.
Receive: The minimum tolerance that a SCSI device shall allow to be subtracted from the REQ (ACK) period.

The Transmit wording seems correct. If the REQ (ACK) period is 25 ns, a fast-80 transmitter may subtract 0.6 ns from it, transmitting with a period of 24.4 ns. It may not subtract 1.0 ns.

The Receive wording seems wrong. The fast-80 receiver "shall allow" a minimum of 0.7 ns to be subtracted from the REQ (ACK) period of 25 ns. Since 1.0 ns is greater than 0.7 ns, does it mean the receiver must tolerate a 24 ns input period?

I suggest:
Transmit: The maximum tolerance that a SCSI device may subtract from the REQ (ACK) period.
Receive: The maximum tolerance that a SCSI device shall allow to be subtracted from the REQ (ACK) period.

CPQ 120
Page 086-090 Section 9.2.

I suggest adding short explanations of some of these timing values. Since these questions keep coming up in committee meetings, readers with just the specification must be even more confused.

- *Bus settle delay:* This provides time for a signal transition to propagate from the driver to the terminator and back to the driver.
- *ATN transmit setup time:* Extra time is specified to provide the increased ATN receive setup time, subject to intersymbol interference, cable skew, and other distortions.
- *ATN receive setup time:* Extra time is specified to ease receiver timing requirements (previous versions of this standard provided two system deskew delays of setup time).
- *pCRC Transmit setup time:* Extra time is specified to provide the increased Receive setup time, subject to intersymbol interference, cable skew, and other distortions.
- *pCRC Receive setup time:* Extra time is specified to ease receiver timing requirements and ensure that this signal, which is outside CRC protection, is received correctly.
- *Transmit REQ assertion period with P_CRCA transitioning:* Extra time is specified to provide the increased Receive REQ assertion period, subject to loss on the interconnect.
- *Receive REQ assertion period with P_CRCA transitioning:* Extra time is specified to ensure that the assertion period is longer than the receive hold time plus the receive setup time.
- *Transmit REQ negation period with P_CRCA transitioning:* Extra time is specified to provide the increased Receive REQ negation period, subject to loss on the interconnect.
- *Receive REQ negation period with P_CRCA transitioning:* Extra time is specified to ensure that the negation period is longer than the receive hold time plus the receive setup time.

CPQ 121
Page 088 Section 9.2.28
The text does not specify whether this is a minimum or maximum time.
Change "is measured from" to "is the minimum time between".

Also, change "qualified the assertion edge" to "qualified on the assertion edge."

CPQ 122
Page 090 Section 9.3
Change "differential" to "LVD".

CPQ 123
Page 093 Section 9.3.3 Figure 46 and 47

Figure 46: add * by the leftmost "may be detected" and "shall be detected "arrows. This forces the first zero crossing to be chosen for the "may" level (shorter SETUP) and the last –100 mV crossing to be chosen for the "shall" level (shorter HOLD).

Figure 46: add a new ** by the rightmost "may be detected" and "shall be detected" arrows. The comment for these would be "Use the crossing that yields the shorter ASSERTION PERIOD and NEGATION PERIOD".

Figure 47: add * by the each of the "may be detected" and "shall be detected" arrows. Change the note to "Use the crossing that yields the shorter SETUP time, HOLD time, ASSERTION PERIOD, and NEGATION period"

CPQ 124
Page 095-097 Section 9.4

The "board skew" and "protocol chip" values are introduced here for the first time. They're not mentioned in the main timing tables earlier. Some definition of them might be appropriate.

Add this text:
Table 31 and Table 32 specify setup and hold times at the device connector. Figure 49 and Figure 50 illustrate a possible timing budget behind the device connector, with time apportioned to board skew and to the protocol chip.

CPQ 125
Page 096-097 Section 9.4

The figures show how the time adds up for setup and hold times.

There is no similar explanation of how the clock assertion and negation signals are allowed to degrade. At fast-80DT rates, the transmit period is 11.5 ns and the receive period is 10 ns. The overall REQ/ACK period is 25 ns, subject to a REQ/ACK period tolerance. Figures showing how these numbers relate would be helpful. There seems to be no guidance in the standard about how fast the transmit protocol chip must switch the signal, how much loss the board may introduce.

Something like this.

fast-80DT	REQ/ACK Period	
Nominal	25	
period tolerance	-0.6	
Actual budget	24.4	
	Assertion period	Negation period
Nominal	12.5	12.5
period tolerance split evenly	-0.3	-0.3
transition time	-0.5	-0.5
Transmit protocol chip	11.7	11.7
board loss	-0.2	-0.2
Transmit connector (Transmit A/N Period)	11.5	11.5
cable loss	-1.5	-1.5
Receive connector (Receive A/N Period)	10	10
board loss	-0.2	-0.2
Receive Protocol chip	9.8	9.8

CPQ 126
Page 098 Section 10

Should BUS FREE, ARBITRATION, SELECTION, and RESELECTION collectively be called the control phases? If done, then change the header for Table 30 (Section 9.1) to refer to "control phase" instead of "control".

CPQ 127
Page 099 Section 10.2

Change semicolon to colon after "SCSI bus"

CPQ 128
Page 099 Section 10.2.1

Add blank line between b) and c).
Change ", however" to ". However," in item c)

CPQ 129
Page 099 Section 10.2.1

Remove "in the Disconnect-Reconnect mode page (see 18.1.1). Initiators don't have that page, yet still might be fair.

CPQ 130
Page 099 Section 10.2

Integrate basic fairness algorithm requirements into the arbitration section.

Add some text about fairness as the last paragraph:
> SCSI devices with arbitration fairness enabled shall maintain a fairness register which records the SCSI IDs of devices that need a chance to arbitrate (see Annex B). Fairness in normal arbitration is enabled in targets by the Disconnect-Reconnect mode page (see 18.1.1). Fairness is always enabled in QAS.

CPQ 131
Page 099 Section 10.2.1 Note 23

Add ", and may not be ensured fair arbitration by the arbitration fairness algorithm." to the end of the note.

CPQ 132
Page 100 Section 10.2.1

First line. Change "true and within" to "true, within"
Second line. Change "SEL" to "SEL signal".

CPQ 133
Page 100 Section 10.2.1

Integrate basic fairness algorithm requirements into the normal arbitration description.

Add an item and note between d) and e):
> d.5) After the bus free delay in step (b), SCSI devices with arbitration fairness enabled which are not arbitrating shall wait a bus set delay and start sampling the DATA BUS to determine which SCSI devices attempted arbitration, which SCSI device won, and which SCSI devices lost. This sampling shall continue for an arbitration delay after the bus free

delay in step (b). Each SCSI device shall update its fairness register with all lower-priority device IDs that lost arbitration.

NOTE xx: For ease of implementation, this sampling may begin when BSY is true following BUS FREE and end when SEL is true.

CPQ 134
Page 100 Section 10.2.2

Change "An initiator that supports QAS shall negotiate…using the PPR, in order to enable QAS" to "An initiator that supports QAS may negotiate…using the PPR message." The "in order to" is too far away from the start of the sentence. It seems to be requiring QAS be used with QAS targets.

CPQ 135
Page 100 Section 10.2.2

Remove "and normal" from "SCSI devices that support QAS shall implement the fairness algorithm during all QAS and normal arbitrations." QAS capability has no bearing on non-QAS arbitration behavior.

CPQ 136
Page 100 Section 10.2.2.1

Item b) Change "message and if the initiator did not create an attention condition then" to "message, if there is no attention condition, "

CPQ 137
Page 100 Section 10.2.2.1

Item c) Change "true and if there is no attention condition the" to "true, if there is no attention condition, "

CPQ 138
Page 100 Section 10.2.2.1

Item f) Change "of the SCSI signals" to "the SCSI signals"

CPQ 139
Page 101 Section 10.2.2.1

Integrate basic fairness algorithm requirements into the QAS description.

Item a) Remove "if allowed under the fairness algorithm."
Item c) Add to end: "If arbitration fairness is enabled, the SCSI device shall not arbitrate until its fairness register is cleared."

Add item after e):
> f) After the QAS arbitration delay in step (d), SCSI devices with arbitration fairness enabled which are not arbitrating shall start sampling the DATA BUS to determine which SCSI devices are attempting arbitration, which SCSI device won, and which SCSI devices lost. This sampling shall continue for a bus settle delay plus two system deskew delays. The devices shall update their fairness register with all device IDs that lost in arbitration.

CPQ 140

Page 101 Section 10.2.2.1

Item b) Change "of a two" to "of two"

CPQ 141
Page 102 Section 10.3.1
Page 104 Section 10.4.1

Change:
> 10.3.1 The SCSI device that won the arbitration becomes an initiator by not asserting the I/O signal.
> 10.4.1 The winning SCSI device becomes a target by asserting the I/O signal.

to:
> 10.3.1 The SCSI device that won the arbitration identifies itself as an initiator by not asserting the I/O signal.
> 10.4.1 The SCSI device that won the arbitration identifies itself as a target by asserting the I/O signal.

CPQ 142
Page 104 Section 10.4

To match the wording in section 10.3:
Change "RESELECTION is a phase that allows" to "The RESELECTION phase allows"

Add a sentence to the end of the paragraph: "During the RESELECTION phase the I/O signal is asserted to distinguish this phase from the SELECTION phase."

CPQ 143
Page 113 Section 10.5.2.3

Add a sentence to the end of the section: "The IGNORE WIDE RESIDUE message may be used to indicate that the byte is undefined." Add similar text for packetized.

CPQ 144
Page 115 Section 10.9.2

Third paragraph. Change "ensures" to "ensure"
Fifth paragraph. Change" transfer at least" to "transferring at least"

CPQ 145
Page 115 Section 10.8

The last paragraph if 10.8 and the first sentence of section 10.8.1 both imply that the status phase is one byte long. The first two paragraphs don't mention that restriction.

In the first paragraph, change "The STATUS phase allows the target to request that status information" to "The STATUS phase allows the target to request that a status byte".

CPQ 146
Page 116 Section 10.9.2

Change "(e.g. ABORT TASK SET" to "(e.g. after receiving ABORT TASK SET"

CPQ 147
Page 117 Section 11.2.1

Change "is guaranteed to detect" to "detects"

CPQ 148
Page 120 Section 12.1

Fifth paragraph. Change "an attention setup time" to "an ATN setup time"
Sixth paragraph. Change "information unit and then may" to "information unit, which may"
List of items. Change "If an attention condition is created" to "If an attention condition is detected" in each of a) through g)

Last paragraph: Change "asserted if more than one byte" to "asserted throughout the MESSAGE OUT phase if more than one byte".

CPQ 149
Page 123 Section 13 Last paragraph

Change "Also any" to "Also, any"
Change "BUS FREE phase but many" to "BUS FREE phase, but many"

CPQ 150
Page 133-134 Section 14.2.1 Table 37, 38

Capitalize task in the header of each table
Use small caps for "task management function not supported" in the last row of table 38

CPQ 151
Page 137 Section 14.2.3 Last paragraph

Use small caps for "iucrc interval" on the first line
Use small caps for "iucrc" on the second line and third line

CPQ 152
Page 134-140 around Section 14.2

Fix the mixed formatting for "IUCRC" (small caps IU, lower case CRC in several places)

CPQ 153
Page 145 Section 16.2 Table 49
Page 163 Section 16.3 Table 63
Page 165 Section 16.4 Table 68

Yes: change "message" to "MESSAGE OUT"
Not required: change "message" to "MESSAGE OUT"
n/a: Add "(MESSAGE IN)"

CPQ 154
Page 145 Section 16.2 Table 49
Combine the DISCONNECT IN and OUT rows like MESSAGE REJECT, PPR, SDTR, and WDTR are combined:
        04/O/O/DISCONNECT/In/Out/Yes

CPQ 155
Page 151 Section 16.2.9 Table 55

Change "12.5" to "12,5"

CPQ 156
Page 170 Section 18.1.1 Second paragraph

Change "manor" to "manner"

CPQ 157
Page 258 Section L

Change "Integrity Checking" to "Domain Validation" everywhere. This is the marketing term, and is the same term approved for the SCSI Domain Validation technical report which may grow to replace this annex.

CPQ 158
Page 258 Section L.1.1

Move NOTE 57 from section L.1.1 to section L.3, which talks about PPR, WDTR, and SDTR.

CPQ 159
Page 259 Section L.3

Change "parameters for example" to "parameters; for example, "

CPQ 160
Page 261 Section M.1

Remove the duplicated paragraph.

CPQ 161
Page 263 Section M.2.2

Change BCH to "Bose, Chaudhuri and Hocquenghem (BCH)"

CPQ 162
Page 265 Section M.6.1

Change the C code font to a monospace font or manually line up the closing comment markers. Change "an fifteen" to "a fifteen" near the bottom

CPQ 163
Page 267 Section M.6.2

Change Verilog to "Verilog® Hardware Description Language (IEEE 1364)"