Fast-160 Presentation

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SCSI Fast-160

- F-160 Transfer (320 Mbytes/Sec for Wide bus)
  - Maintains existing protocol & Driver/Receiver types
  - Double REQ/ACK frequency
- Skew compensation methodology
  - Use training sequence for determining skew
- ISI pre-compensation in the REQ/ACK and data driver
**F-160 Transfer (2X Scale of F-80)**

- Double existing F-80 ACK/REQ Frequency
  - 320 Mbytes/Sec for Wide bus (vs. 160 Mbytes/sec)
  - Transfer 2-bytes every 6.25 ns (vs. 12.5 ns)
  - 3.125 ns nominal Setup/Hold time (vs. 6.25 ns)
F-160 Transfer (2X Scale of F-80)

- 3.125 ns Setup/Hold time leaves very little (0.225 ns) remaining cable plant budget for “Signal Timing Skew”
  - Signal timing skew includes cable skew and signal distortion skew
  - Signal distortion skew includes ISI (inter-symbol interference) and signal crossing time through the receiver detection range
Signal Skew Limits Direct Scaling

- System skew is dominated by time invariant parameters (during data transfer)
  - Sender ASIC skew (silicon process, logic)
  - Sender board skew (trace length and impedance control, pin cap.)
  - Cable plant skew (physical wire impedance variations, lumped/distributed loading, stubs and connectors)
  - Receiver board skew
  - Receiver ASIC skew

- This system skew can be greatly reduced by realigning the strobe and data to the desired relationship by de-skewing logic at the receiver

- Each receiving device realigns data and strobe bits uniquely according to skew detected by dedicated logic for each bit
Signal Skew Detection

- Strobe to signal skew is measured by successive sampling of the data bit by delayed versions of the REQ/ACK strobe
  - Optimal setup/hold relationship can be determined by digital solution
  - Accuracy will be determined by the sampling resolution
- This setup/hold relationship is then used for data transfer
- A “training sequence” is used to establish a known strobe/data relationship between sender and receiver, so that the receiver can measure skew

![Diagram of REQ/ACK and DB(n) signals with successive sampling marks]
Skew Compensation Limitation

- With 50% Setup/Hold, REQ/ACK to data relationship moves into the next cell time, to return to strobe centering, strobe and data must be adjusted.
  - Data bits need to be delayed individually and REQ/ACK needs to be delayed also when REQ/ACK proceeds data center (not preferred).
  - Otherwise, REQ/ACK needs to be delayed individually per data bit (preferred) and all data bits delayed by a fixed amount (not preferred).
F-160 Transfer (Early Strobe Solution)

- Proposing to align strobe and data so individual data bits do not have to be delayed by a fixed amount
  - Double ACK/REQ Frequency
  - 320 Mbytes/Sec for Wide bus (transfer 2-bytes every 6.25 ns)
  - 0ns Setup / 6.25 ns Hold time (nominal), for positive delay strobe alignment

[Diagram showing strobe and data sequence with 6.25 ns intervals for REQ/ACK and DB(15:0) signals]
Skew Compensation Timing Budget

- Maximum skew to be compensated is 5.4 ns
  - Sender ASIC skew - 1.25 ns
  - Sender board skew - 0.2 ns
  - Cable plant skew - 2.5 ns for 25 m cable (30 ps/ft)
  - Receiver board skew - 0.2 ns
  - Receiver ASIC skew - 1.25 ns

- Allows de-skew logic to delay REQ/ACK by less than 6.25 ns (F-160 DT period)
F-160 Transfer (with Skew Comp.)

- Cable plant budget for “Signal Timing Skew” can be increased by de-skewing data
  - e.g. cable plant budget for “Signal Timing Skew” can be increased to 3.85 ns by de-skewing data by 3.625 ns

Setup and Hold Timings for DT Data Transfers
(All times in ns)

<table>
<thead>
<tr>
<th>Protocol Chip</th>
<th>SCSI Device Connector</th>
<th>Cable</th>
<th>SCSI Device Connector</th>
<th>Protocol Chip</th>
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<tr>
<td>Fast-80</td>
<td>6.25 - 1.25 = 5</td>
<td>5</td>
<td>0.2 = 4.8</td>
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</tr>
<tr>
<td></td>
<td>6.25</td>
<td>5</td>
<td>4.8</td>
<td></td>
</tr>
<tr>
<td>Fast-80</td>
<td>6.25 - 1.25 = 5.25</td>
<td>5.25</td>
<td>0.2 = 4.8</td>
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</tr>
<tr>
<td></td>
<td>6.25</td>
<td>5.25</td>
<td>4.8</td>
<td></td>
</tr>
<tr>
<td>Fast-160</td>
<td>3.125 - 1.25 = 1.875</td>
<td>1.875</td>
<td>0.2 = 1.675</td>
<td>(2.375)</td>
</tr>
<tr>
<td></td>
<td>3.125</td>
<td>1.875</td>
<td>1.675</td>
<td>(2.375)</td>
</tr>
<tr>
<td></td>
<td>3.125</td>
<td>1.875</td>
<td>1.675</td>
<td>(2.375)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- 3.85</td>
<td>(2.175)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(2.175)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- 0.2</td>
<td>(2.375)</td>
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<td>(2.375)</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>1.25</td>
<td>Setup Hold</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>2.375</td>
<td>Setup Hold</td>
</tr>
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</table>

For 1.25 ns setup/hold at protocol chip, [2.375 + 1.25] = 3.625 ns of de-skewing is needed + 3.625
Skew Compensation

- De-skew data in the receiver by delaying REQ/ACK per data bit
Adaptive Skew Compensation Training

The diagram illustrates the flow of data through a system with adaptive skew compensation training. Key components include:

- **DB(n)**
- **REQ/ACK**
- **Taps**
- **Delay**
- **DEL**
- **SHIFT**
- **EN**
- **Adaptive Selection SM**
- **STROBE**

Connections and signals are indicated with arrows, showing the direction of data flow. The diagram also includes symbols for DB_NE(n) and DB_AE(n) at the output.
Adaptive Skew Compensation Training

00000000001111111111111111111111

11

16

32

Err

10/12/99 - 13
Mayank Patel

T10/99-XXXR0
Skew Comp. - Training Sequence

- Train at beginning of every data phase (no setup required to be remembered)
- Single edge training requires massive amount of logic per data bit (not preferred)
- Training is done on assertion edge only, negation edge skew differences assumed to be acceptably small
- Count fixed # of REQ/ACKs for training at F-80 rate (DT period of 12.5 ns)
  - First 3 pulses for ISI settling time
    - 3 pulses => 6 F-80 DT periods => 75 ns
  - Then, 5 pulses for training for 5 training edges
    - e.g. 32 samples requires $2^5 = 32$ => 5 training edges => 10 F-80 DT periods => 125 ns
Training Sequence Overhead

% Improvement over F-80

<table>
<thead>
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<th>Transfer Size (bytes)</th>
<th>80</th>
<th>85</th>
<th>90</th>
<th>95</th>
<th>100</th>
<th>105</th>
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<td>.5 K</td>
<td>90</td>
<td>95</td>
<td>100</td>
<td>105</td>
<td>100</td>
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<td>85</td>
<td>90</td>
<td>95</td>
<td>100</td>
<td>105</td>
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<tr>
<td>4 K</td>
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<td>80</td>
<td>85</td>
<td>90</td>
<td>95</td>
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<tr>
<td>8 K</td>
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<td>75</td>
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<td>85</td>
<td>90</td>
<td>95</td>
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<td>70</td>
<td>75</td>
<td>80</td>
<td>85</td>
<td>90</td>
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<tr>
<td>32 K</td>
<td>60</td>
<td>65</td>
<td>70</td>
<td>75</td>
<td>80</td>
<td>85</td>
</tr>
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</table>
Secondary Effects - ISI

- ISI (Inter Symbol Interference) such as first pulse problem
- Skew compensation alone may be sufficient to bring timing margin back to F-80 levels
- Additional compensation will improve timing margin
ISI Pre-compensation

- Driver adjusts strength for first pulse problem by lowering the strength for runs (or incrementing the strength for non-runs)