Title: Proposal for turn-on/turn-off of a free-running clock

To: T10 Technical committee
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x1 Introduction

T10/99-262r0 proposes the use of a free-running clock at 80 MHz (for a maximum transfer rate of 320 megabytes per second) to eliminate ISI on the clock line as a source of timing error. This proposal suggests a method for starting and stopping this free running clock.

The following is a quick summary of 99-262r0 (for background): Either the REQ or ACK signal would become a free-running clock during the appropriate DT DATA phase, depending on the direction of data transfer. The P1 signal, driven by the data source, would be a qualifier, indicating whether there is valid data on each clock edge.

x2 Starting the clock for a DT DATA IN phase

During transfers from the target to the initiator (DT DATA IN phase) the REQ signal becomes the free-running clock. The steps for starting the clock are:

1. The target shall change phase to DT DATA IN;
2. The target shall wait the required Bus Settle Delay (400ns);
3. The target shall drive a clock waveform on the REQ signal, with the P1 signal deasserted;
4. After a minimum of 5 clock pulses, the target may begin asserting the P1 signal to transmit data.

> Note: The requirement that the clock be asserted for 5 pulses minimum before any data transfer (assertion of P1) is to ensure that the line has been conditioned – i.e., there is no more ISI.

x3 Stopping the clock for a DT DATA IN phase

To stop the clock in DT DATA IN phase:

1. If information unit transfers are enabled, the target shall transfer all the data for the current packet, and then deassert the P1 signal;
2. If information unit transfers are disabled, the target shall transfer an entire data group, and then deassert the P1 signal;

NOTE: this is not meant to imply that the P1 signal cannot be asserted and deasserted throughout the transfer for flow control.

3. The target shall wait for all ACK edges to be received (REQ/ACK offset = 0);
4. The target may then deassert the REQ signal.

x4 Starting the clock for a DT DATA OUT phase

During transfers from the initiator to the target (DT DATA OUT phase), the ACK signal becomes the free-running clock. The steps for the initiator to start the clock are:

1. The target shall change phase to DT DATA OUT.
2. The target shall wait the required Bus Settle Delay (400ns);
3. The target shall assert REQ (the target may then deassert and assert REQ at the negotiated speed up to the negotiated offset limit);
4. Once the initiator detects the first assertion of REQ, it shall begin driving a clock waveform on the ACK signal, with the P1 signal deasserted;
5. After a minimum of 5 clock pulses, the initiator may begin asserting the P1 signal to transmit data.

x5 Stopping the clock for a DT DATA OUT phase

To stop the clock in DT DATA OUT phase:

1. If information unit transfers are enabled, the target shall assert enough REQs for all data for the current packet, and then keep REQ deasserted;
2. If information unit transfers are disabled, the target shall assert REQs for an entire data group, then keep REQ deasserted;
3. The target shall wait for all data to be received from the initiator (REQ/ACK offset = 0);
4. The target may then transition to another phase, or if information unit transfers are enabled, it may transition to bus free;
5. Within 200ns of detecting the phase change, the initiator shall deassert the ACK signal.