T10/99-295r5

Seagate Technology
10323 West Reno (West Dock)
Oklahoma City, OK 73127-9705
P.O. Box 12313
Oklahoma City, OK 73157-2313
Tel: 405-324-3070
Fax: 405-324-3794
gene_milligan@notes.seagate.com

5/1/2000
John Lohmeyer
T10 Chairman

Subject: **Proposal for Enhanced signalling to be included in SPI-4**

At the 4/27/2000 SPI-4 working group meeting, T10/99-295r4 was voted into SPI-4 with modifications agreed to in the meeting. The modifications were a combination of changes by unanimous consent and a few specific motions that were not unanimous but decisive.

A new document number will be requested for the figures and tables that have been left for generation after this proposal was agreed to and incorporated into SPI-4.

Gene Milligan
Director, Development Strategy
Seagate Technology Inc.

p.s. Although the SPI-3 files were used, clause numbers, figure numbers, and table numbers are as FrameMaker determined and have not been synchronized exactly to SPI-3. New timing terms were placed at the end of the definitions rather than scattered alphabetically. Correcting these format differences could be fun and games for the SPI-4 technical editor. Since time to wrestle with FrameMaker was finite, some figure cleanup was left also for editor amusement. Finally the change bar formatting did not seem to be working.

Contents:

3.1.X asymmetry: the total (peak to peak) time difference of a SCSI data bus signal from the nominal time of the signal at a given point (e.g., the difference in time of a one versus a zero in a continuous data pattern of alternating ones and zeros).

3.1.X REQ(ACK) offset: for Fast =<80 transfers the number of REQ assertions that may be sent by the target in advance of the number of ACK assertions received from the initiator, establishing a pacing mechanism. For Fast 160 during Data Out transfers the number of REQ transitions that may be sent by the target in advance of the number of P1 enabled data transfers received from the initiator, establishing a data pacing mechanism. For Fast 160 during Data In transfers the number of P1 enabled data transfers that may be sent by the target in advance of ACK transitions received from the initiator, establishing a data pacing mechanism.

7 SCSI parallel interface electrical characteristics

7.5.1 LVD driver characteristics

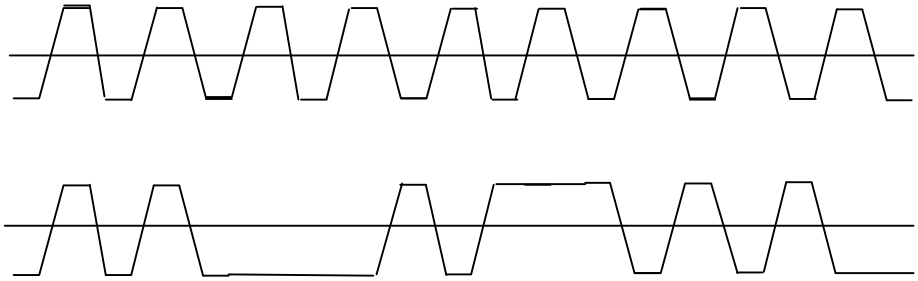
The LVD driver shall provide balanced asymmetrical sources that provide current from positive supply voltage to one signal line while sinking the same current to ground from the other signal line as shown in figure 42. Diagonally opposite sources operate together to produce a signal assertion or a signal negation. An assertion is produced when positive supply voltage current is sourced from SOURCE 4 to the +SIGNAL line and SOURCE 2 sinks the same current from the -SIGNAL line to ground. A negation is produced when positive supply voltage current is sourced from SOURCE 1 to the -SIGNAL line and SOURCE 3 sinks the same current from the +SIGNAL line to ground.

During data transfer phases, if the transfer mode is one with the PPR P_EN (Precomp Enable) bit set to one, the driver source current shall comply with precompensation requirements in Table (New 1). Nominal driver current is sourced to or from the SCSI Data bus line for the first data transfer time after a change in the data bus line state from asserted to negated or from negated to asserted. After a data transfer time from the last data bus line state change the current sourced to or from the SCSI Data bus line shall be cutback (reduced) (see A.2.1). The rules for precompensation shall apply to REQ, ACK, P1, P_CRCA as well as DB(15-0).

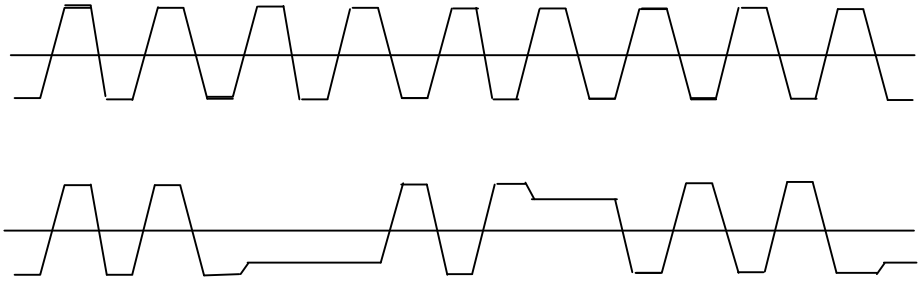
Table 28 - Precompensation

First data bits	Cutback	Notes
1**$\overline{0101010}$**	Cutback first one and no cutback of overlined bold bits	Last bit of training is a one yielding one - one start
11**$\overline{0}$1**1**$\overline{0}$1**1	Cutback all but overlined bold bits and no cutback of overlined bold bits	Cutback once whenever bit value does not change
111**$\overline{0}$**00**$\overline{1}$**1	Cutback all but overlined bold bits and no cutback of overlined bold bits	Cutback once whenever bit value does not change
$\overline{01010101}$	No cutback of overlined bold bits (all)	Last bit of training is a one yielding 10 start
$\overline{0}$0**$\overline{1}$0**$\overline{1}$0**0	Cutback all but overlined bold bits and no cutback of overlined bold bits	Cutback once whenever bit value does not change
$\overline{0}$00**$\overline{1}$**11**$\overline{0}$**0	Cutback all but overlined bold bits and no cutback of overlined bold bits	Cutback once whenever bit value does not change
Note: The state of a databus line, after training shall follow the above rules regardless of whether or not the state is qualified as valid or invalid (pause) by the P1 phase state. The training pattern shall also follow the precompensation rules.		

Figure TBD illustrates the transmitter drive strength technique.



a) Drivers without precompensation



b) Drivers with precompensation

Figure 42 - Illustration of the driver precompensation technique.

8 Adjust clause number to ballpark for clause 9 stuff

Table 29 - Transceiver/speed support map

Transceiver	Maximum transfer rate						
	Async.	**Fast-5**	**Fast-10**	**Fast-20**	**Fast-40**	**Fast-80**	**Fast-160**
LVD (ST)	yes	yes	yes	yes	yes	no	no
LVD (DT)	no	no	yes	yes	yes	yes	yes
Key: yes = Transceiver/speed combination supported by this standard. No =Transceiver/speed combination not supported by this standard.							

9 Adjust clause number to ballpark

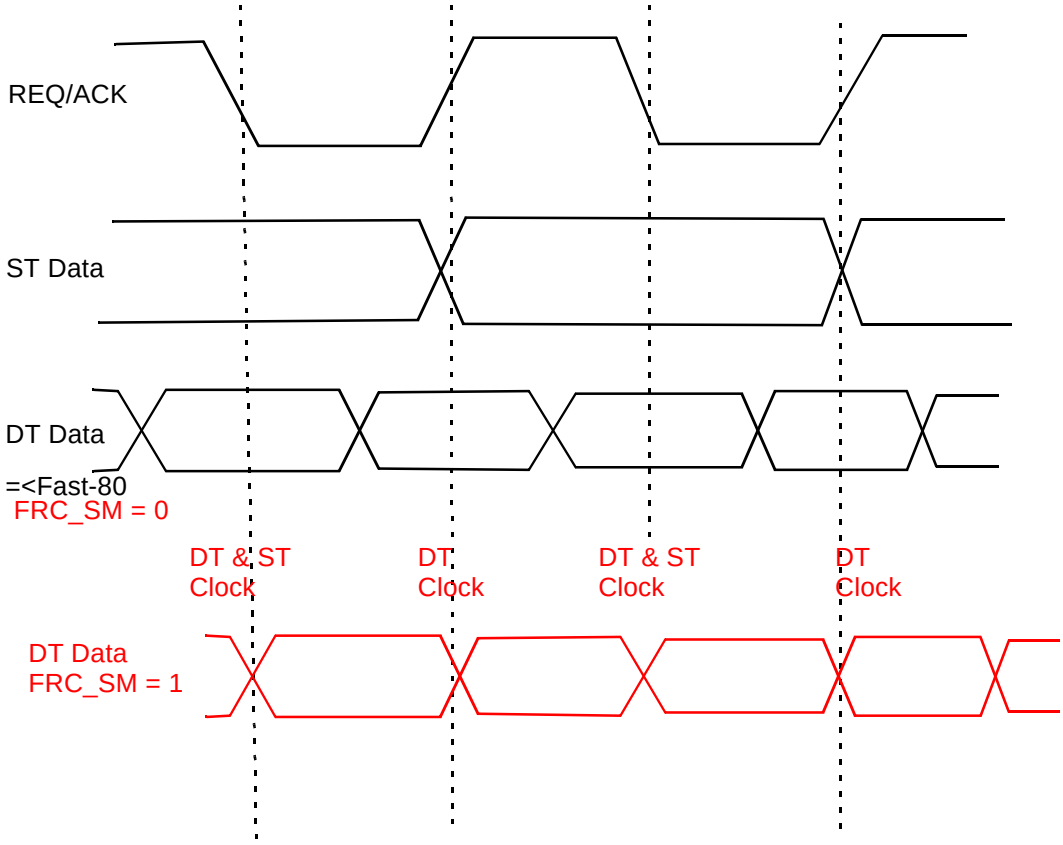


Figure 43 - ST latching data vs. DT latching data

See XXX (where Table 33 is).

Table 30 - LVD maximum bus path length between terminators

Interconnect	Maximum bus path length between terminators (meters)					
	Fast-5	Fast-10	Fast-20	Fast-40	Fast-80	Fast-160
Point-to-point interconnect	25	25	25	25	25	25
Multidrop interconnect	12	12	12	12	12	12
Note:						

Proposer note: Table 29 was voted into SPI-4 at the 3/7/2000 meeting without a Note 1.

9.1 Adjust clause number to ballpark

9.2 Timing description

9.3 SCSI parallel bus timing values (Table X and Y [formerly 30 & 31] not changed yet but will change or be deleted)

Old Table SCSI bus data & information phase DT timing values

(First Method is with timing specifications as measured at the SCSI bus connector.)

Potential new table SCSI bus data & information phase DT timing values (Fast-160 Second Method is with setup and hold timing specifications as if after deskewing and strobe offset.)

Table 31: SCSI Fast-160 Timing Budget Template

Item	Fast-80 (Reference)	Fast-160	Comments
Nominals:			
REQ(ACK) Period	**25 ns**	**12,5 ns**	
Data transfer period	**12,5 ns**	**6,25 ns**	
Ideal Setup/Hold	**6,25 ns**	**3,125 ns**	
Non-compensatable:		**pk to pk**	
REQ(ACK) period tolerance / 2	**0,3 ns**	**0,06 ns**	**Tolerance of transmitter Note 1**
Driver asymmetry	**0,5 ns**	**0,50 ns**	
REQ(ACK) Driver asymmetry			**Deleted due to double counting**
Receiver asymmetry	**0,5 ns**	**0,35 ns**	
REQ(ACK) Receiver asymmetry	**0,5 ns**		**Deleted due to Double counting**
System noise at launch	**0,25 ns**	**0,25 ns**	**Time impact**
System noise at receiver	**0,25 ns**	**0,25 ns**	**Time impact**
Near end Crosstalk	**0,25 ns**	**0,7 ns**	**Time impact**
Crosstalk			**Deleted due to Double counting**
Chip noise	**0,1 ns**	**0,2 ns**	
Receiver amplitude skew	**0,2 ns**	**0,2 ns**	**Post compensation delta**
Clock jitter	**0,5 ns**	**0,25 ns**	**Negative jitter only**
Strobe offset tolerance	**0,0 ns**	**0,5 ns**	
Residual Skew error	**0,0 ns**	**0,3 ns**	**After skew compensation**
Non-compensatable total:	**3,1 ns**	**3,81 ns**	
Compensatable skew:			**Or partially**

Table 31: SCSI Fast-160 Timing Budget Template

Item	Fast-80 (Reference)	Fast-160	Comments
Transmitter chip skew	**0,75 ns**	**0,75 ns**	**Fast 80 is 1,25 but judged to include asym-metry term**
Receiver chip skew	**0,75 ns**	**0,75 ns**	**Fast 80 is 1,25 but judged to include asym-metry term**
Cable skew	**2,5 ns**	**2,5 ns**	
Two x trace skew	**0,4 ns**	**0,4 ns**	
ISI of data	**0,425 ns**	**4,0 ns**	**Worse case pattern (+2 ns/ -1 ns)**
ISI of REQ(ACK)	**0,425 ns**	**0,0 ns**	**Post preamble**
May detect to shall detect ambiguity	**1,5 ns**	**0,0 ns**	**Assumed to be negligi-ble in given chip**
Compensatable total:	**6,75 ns**	**8,4 ns**	
ISI Compensation	**0,0 ns**	**2,0 ns**	**(+1ns / -0,5 ns)**
Skew compensation	**0,0 ns**	**4,4 ns**	
Compensation total:	**0,0 ns**	**6,4 ns**	
Total Error Inputs:	**9,85 ns**	**11,96 ns**	
Post compensation error:	**9,85 ns**	**5,56 ns**	
Minimum data valid window (data time-net error)	**1,65 ns**	**0,69 ns**	**Note 2, Note 3**

Notes:
1) Tolerance adjusted for half cycle (data transfer period)
2) Fast-80 budget in SPI-3 neglects asymmetry & detection ambiguity and lumps chip noise, clock jitter, crosstalk, noise, ISI and receiver amplitude skew into other terms (e.g., signal distortion skew) and/or ignores the effects.
3) Minimum compensated setup and hold half this value if ISI symmetrical or if strobe set to split the ISI difference.

9.2.8 Cable skew

The maximum difference in propagation time allowed between any two SCSI bus signals measured between any two SCSI devices excluding any signal distortion skew delays.

9.2.9 pCRC receive hold time

The minimum time required at the receiver between the transition of the REQ signal and the transition of the P_CRCA signal while pCRC protection is enabled (see 16.3.10).

9.2.10 pCRC receive setup time

The minimum time required at the receiver between the transition of the P_CRCA signal and the transition of the REQ signal while pCRC protection is enabled (see 16.3.10).

Specified to ease receiver timing requirements and ensure that this signal, which is outside CRC protection, is received correctly.

9.2.11 pCRC transmit hold time

The minimum time provided by the transmitter between the transition of the REQ signal and the transition of the P_CRCA signal while pCRC protection is enabled (see 16.3.10).

9.2.12 pCRC transmit setup time

The minimum time provided by the transmitter between the transition of the P_CRCA signal and the transition of the REQ signal while pCRC protection is enabled (see 16.3.10).

Specified to provide the increased receive setup time, subject to intersymbol interference, cable skew, and other distortions.

9.2.21 Receive assertion period

The minimum time required at a SCSI device receiving a REQ signal for the signal to be asserted while using synchronous data transfers, provided P_CRCA is not transitioning with pCRC protection enabled (see 16.3.10). Also, the minimum time required at a SCSI device receiving an ACK signal for the signal to be asserted while using synchronous data transfers. For SE fast-5 and fast-10 operation, the time period is measured at the 0,8 V level. For SE fast-20 operation the period is measured at the 1,0 V level. For LVD see figure 46 and figure 47 for signal measurement points.

9.2.22 Receive hold time

For ST data transfers the minimum time required at the receiving SCSI device between the assertion of the REQ signal or the ACK signals and the changing of the DATA BUS, DB(P_CRCA), and/or DB(P1) signals while using synchronous data transfers, provided P_CRCA is not transitioning with pCRC protection enabled (see 16.3.10). For DT data transfers the minimum time required at the receiving SCSI device between the transition (i.e. assertion or negation) of the REQ signal or the ACK signals and the changing of the DATA BUS, DB(P_CRCA), and/or DB(P1) signals while using synchronous data transfers.

NOTE 19 - This definition may need to be tweaked depending upon the final method chosen in the timing tables to show the results of the timing budget.

9.2.23 Receive negation period

The minimum time required at a SCSI device receiving a REQ signal for the signal to be negated while using synchronous data transfers. Also, the minimum time required at a SCSI device receiving an ACK signal for the signal to be asserted while using synchronous data transfers. For SE fast-5 and fast-10 operation, the time period is measured at the 2,0 V level. For SE fast-20 operation the period is measured at the 1,9 V level. For LVD see figure 46 and figure 47 for signal measurement points.

9.2.24 Receive setup time

For ST data transfers the minimum time required at the receiving SCSI device between the changing of DATA BUS, DB(P_CRCA), and/or DB(P1) signals and the assertion of the REQ signal or the ACK signal while using synchronous data transfers. For DT data transfers the minimum time required at the receiving SCSI device between the changing of DATA BUS, DB(P_CRCA), and/or DB(P1) signals and the transition of the REQ signal or the ACK signal while using synchronous data transfers.

NOTE 20 - This definition may need to be tweaked depending upon the final method chosen in the timing tables to show the results of the timing budget.

9.2.25 Receive REQ (ACK) period tolerance

The minimum tolerance that a SCSI device shall allow to be subtracted from the REQ (ACK) period. The tolerance comprises the transmit REQ (ACK) tolerance plus a measurement error due to noise.

9.2.26 Receive REQ assertion period with P_CRCA transitioning

The minimum time required at a SCSI device receiving a REQ signal for the signal to be asserted while using synchronous data transfers with P_CRCA transitioning with pCRC protection enabled (see 16.3.10).

Specified to ensure that the assertion period is longer than the receive hold time plus the receive setup time.

9.2.27 Receive REQ negation period with P_CRCA transitioning

The minimum time required at a SCSI device receiving a REQ signal for the signal to be negated while using synchronous data transfers with P_CRCA transitioning with pCRC protection enabled (see 16.3.10). Specified to ensure that the negation period is longer than the receive hold time plus the receive setup time.

9.2.28 REQ (ACK) period

The REQ (ACK) period during synchronous data transfers, specified in table 30 for ST DATA phases and in table 31 for DT DATA phases, is the nominal time between adjacent assertion edges of the REQ or ACK signal for the fastest negotiated data transfer rate. For the purpose of calculating the actual REQ (ACK) period tolerance the REQ (ACK) period should be measured without interruptions (e.g., offsets pauses). To
minimize the impact of crosstalk and ISI the measurements should be made by averaging the time between edges during long (i.e., greater than 512 bytes) all zero or all ones data transfers and by ignoring the first and last 10 transitions.

In DT DATA phases the negotiated transfer period for data is half of the REQ (ACK) period since data is qualified on both the assertion and negation edges of the REQ or ACK signal. In ST DATA phases the negotiated transfer period for data is equal to the REQ (ACK) period during synchronous data transfers since data is only qualified on the assertion edge of the REQ or ACK signal.

9.2.29 Reset delay

The minimum time that the RST signal shall be continuously true before the SCSI device shall initiate a reset.

9.2.30 Reset hold time

The minimum time that the RST signal is asserted. There is no maximum time.

9.2.31 Reset to selection

The recommended maximum time from after a reset condition until a SCSI target is able to respond with appropriate status and sense data to the TEST UNIT READY, INQUIRY, and REQUEST SENSE commands (See SCSI Primary Commands-2 standard).

9.2.32 Selection abort time

The maximum time that a SCSI device shall take from its most recent detection of being selected or reselected until asserting the BSY signal in response. This time-out is required to ensure that a target or initiator does not assert the BSY signal after a SELECTION or RESELECTION phase has been aborted.

9.2.33 Selection time-out delay

The minimum time that an initiator or target should wait for the assertion of the BSY signal during the SELECTION or RESELECTION phase before starting the time-out procedure. Note that this is only a recommended time period.

9.2.34 Signal timing skew

The maximum signal timing skew occurs when transferring random data and in combination with interruptions of the REQ or ACK signal transitions (e.g., pauses caused by offsets). The signal timing skew includes cable skew (measured with 0101... patterns) and signal distortion skew caused by random data patterns and transmission line reflections as shown in figure 44, figure 45, figure 46, and figure 47.
The receiver detection range is the part of the signal between the "may detect" level and the "shall detect" level on either edge. (see 9.3)

NOTE 21 - For timing budget purposes the value stated in the table is calculated without the benefit of skew compensation.

9.2.36 Transmit assertion period

The minimum time that a target shall assert the REQ signal while using synchronous data transfers, provided it is not transitioning P_CRCA with pCRC protection enabled (see 16.3.10). Also, the minimum time that an initiator shall assert the ACK signal while using synchronous data transfers.

9.2.37 Transmit hold time

For ST data transfers the minimum time provided by the transmitting SCSI device between the assertion of the REQ signal or the ACK signal and the changing of the DATA BUS, DB(P_CRCA), and/or DB(P1) signals while using synchronous data transfers. For DT data transfers the minimum time provided by the transmitting SCSI device between the transition of the REQ signal or the ACK signal and the changing of the DATA BUS, DB(P_CRCA), and/or DB(P1) signals while using synchronous data transfers.

NOTE 22 - This definition may need to be tweaked depending upon the final method chosen in the timing tables to show the results of the timing budget.

9.2.38 Transmit negation period

The minimum time that a target shall negate the REQ signal while using synchronous data transfers, provided it is not transitioning P_CRCA with pCRC protection enabled (see 16.3.10). Also, the minimum time that an initiator shall negate the ACK signal while using synchronous data transfers.

9.2.39 Transmit setup time

For ST data transfers the minimum time provided by the transmitting SCSI device between the changing of DATA BUS, DB(P_CRCA), and/or DB(P1) signals and the assertion of the REQ signal or the ACK signal

while using synchronous data transfers. For DT data transfers the minimum time provided by the transmitting SCSI device between the changing of DATA BUS, DB(P_CRCA), and/or DB(P1) signals and the transition of the REQ signal or the ACK signal while using synchronous data transfers.

NOTE 23 - This definition may need to be tweaked depending upon the final method chosen in the timing tables to show the results of the timing budget.

9.2.40 Transmit REQ (ACK) period tolerance

The maximum tolerance that a SCSI device may subtract from the REQ (ACK) period.

9.2.41 Transmit REQ assertion period with P_CRCA transitioning

The minimum time that a target shall assert the REQ signal during a DT DATA phase while transitioning P_CRCA with pCRC protection enabled (see 16.3.10).

Specified to provide the increased receive REQ assertion period, subject to loss on the interconnect.

9.3.1 Transmit ISI Precompensation

The effective reduction in worse case ISI timing shift provided by the transmitting SCSI device as seen at the receiving SCSI device connector.

9.3.2 Receive Skew Compensation

The effective reduction in worse case timing skew of data, parity, and strobe signals provided by the receiving SCSI device but not directly observable at the receiving SCSI device connector.

9.3.3 Strobe offset tolerance

The tolerance on the time used to delay the compensated REQ/ACK to strobe the data and parity signals provided by the receiving SCSI device but not directly observable at the receiving SCSI device connector.

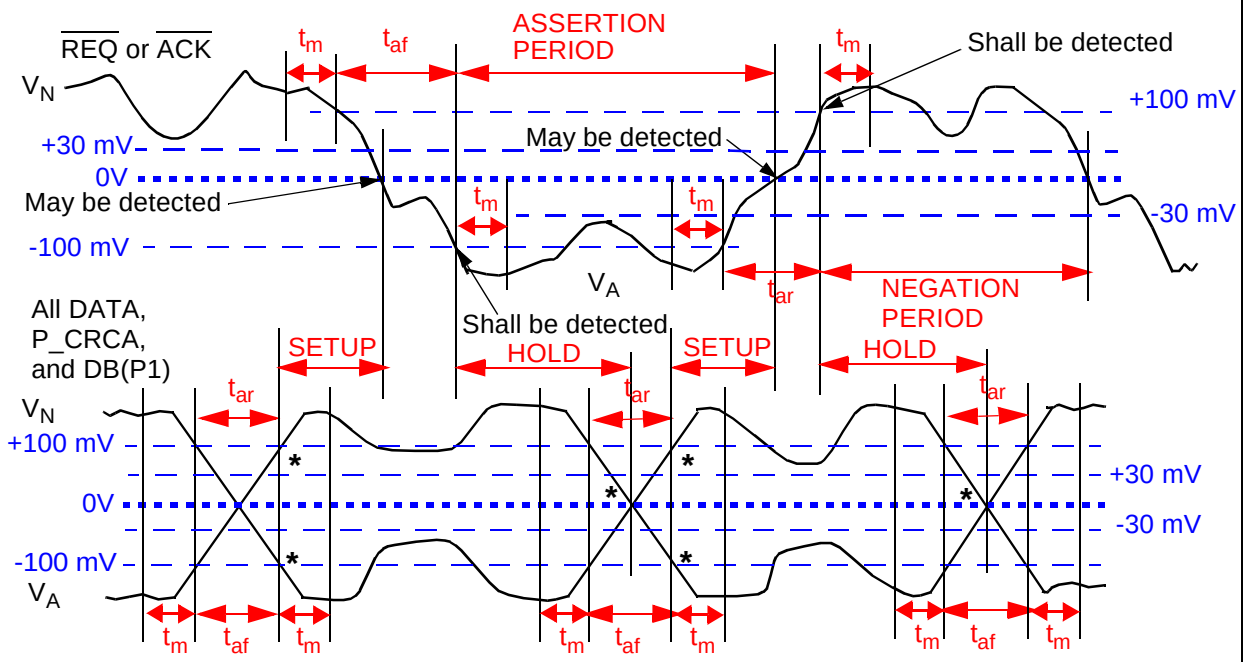
9.3.4 Net Receive Internal Setup and Hold times

The net effective setup or hold time measured within the receiving SCSI device from the worse case bit (data or parity) to the compensated offset strobe. This time may not be observable to other than the SCSI device designer. Failure to meet the requirement may only be observable in terms of increased error rates.

9.4 Measurement points

The measurements points for SE and differential ACK, REQ, DATA, P_CRCA, and PARITY signals are defined in this clause.

If the FRC_SM bit equals one, the timing shall be measured relative to the zero crossing of the differential signal.



* Use the crossing that yields the shorter SETUP and HOLD time

Notes:

1 V_N - negated signal

2 V_A - asserted signal

3 t_m = 1,25ns minimum

4 V_A or V_N are required to drive the 100 mV at the leading edge of the transition. Those signals shall be at least |100 mV| for at least t_m before and after the transition.

5 Differential voltage signals in all cases.

6 t_{af} and t_{ar} shall be less than 3 ns.

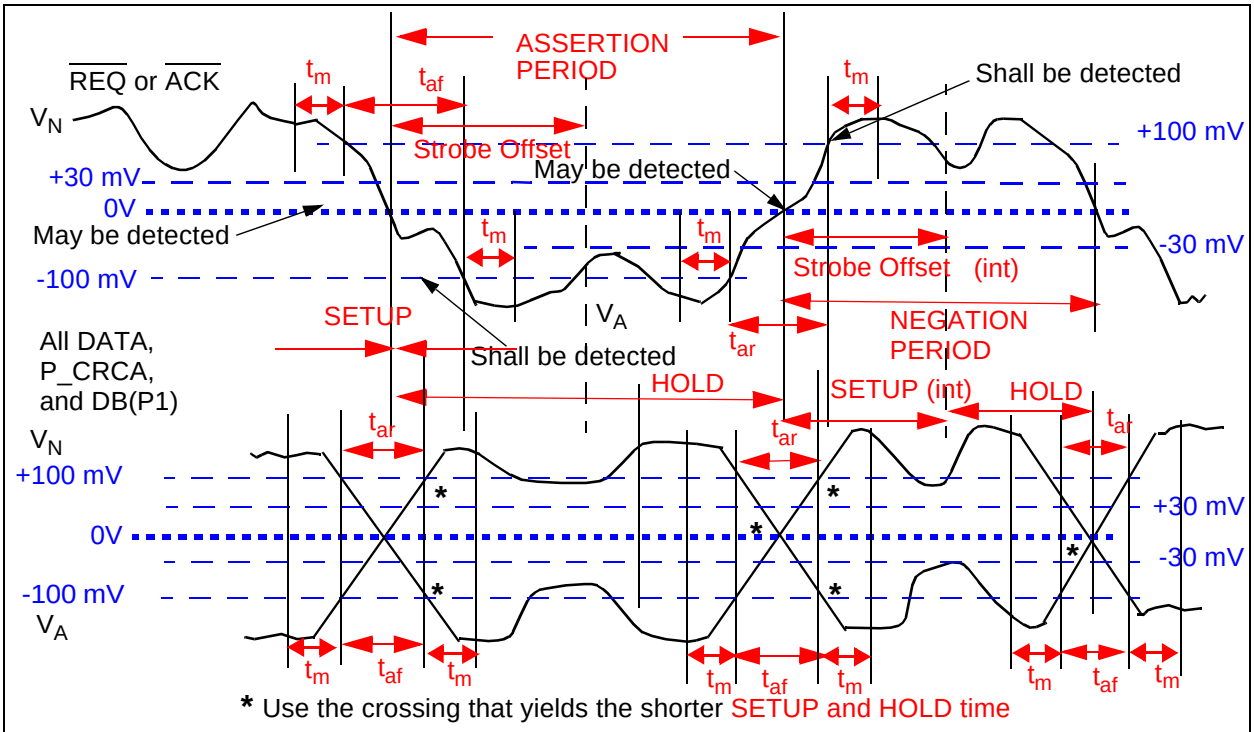
7 Any signal structure may occur at the receiver while in the t_{af} or t_{ar} region including slope reversal.

Figure 44 - LVD timing measurement points for DT =< Fast-80 data transfers

The signal shall transition from -100 to +100 mV or +100 to - 100 mV in 0 to 3 ns, the waveform between -100 and +100 mV is not otherwise specified. Signals shall remain above the |100 mV| level for 1,25 ns at each end of the transition. The signals shall not drop below |30 mV| except during the transitions. Conditions exist with longer, loaded SCSI busses and irregular REQ and ACK pulse widths where long assertions or negations produce a much larger signal than short assertions or negations. This sets up an environment where the short REQ or ACK pulses may not have adequate timing margin unless the definitions in figure 44 are used in the measurement of timing parameters. If the P_EN bit equals one precompensation mitigates the charging effect and helps timing margin.

Measurement of driver timing parameters shall be performed using the circuit and test conditions defined in A.2.5 applied to the SCSI device connector. Receiver timing parameters are defined by the waveforms existing at the connector of the receiving SCSI device. The receiver timing parameters include the effects of data pattern. The receiver data pattern is therefore not defined.

Figure 46 shows the LVD signal requirements at the receiving SCSI device.



Notes:

1 V_N - negated signal

2 V_A - asserted signal

3 t_m = 1,25ns minimum

4 V_A or V_N are required to drive the 100 mV at the leading edge of the transition. Those signals shall be at least |100 mV| for at least t_m before and after the transition.

5 Differential voltage signals in all cases.

6 t_{af} and t_{ar} shall be less than 3 ns.

7 Any signal structure may occur at the receiver while in the t_{af} or t_{ar} region including slope reversal.

8 Strobe Offset is from the actual detected time to the implemented offset time. (int) = internal. Since effective timing is based upon actual detection, all timing measurements shall be based upon zero crossings when the FRC_SM bit equals one.

Figure 45 - LVD timing measurement points for DT = Fast - 160 data transfers

Figure TBD (46) shows the LVD signal requirements at the receiving SCSI device for Fast =<80. SCSI devices, during Fast - 160, shall operate with signals at the receiving SCSI device meeting either Figure TBD (47), Figure (48) or both. Mask 1 is applicable to signals that have more timing margin than those for Mask 2 and allows less amplitude margin than does Mask 2. The lower amplitude margin of Mask 1 may result in timing margin loss internal to the receiver. The higher amplitude margin of Mask 2 should result in less timing margin loss internal to the receiver.

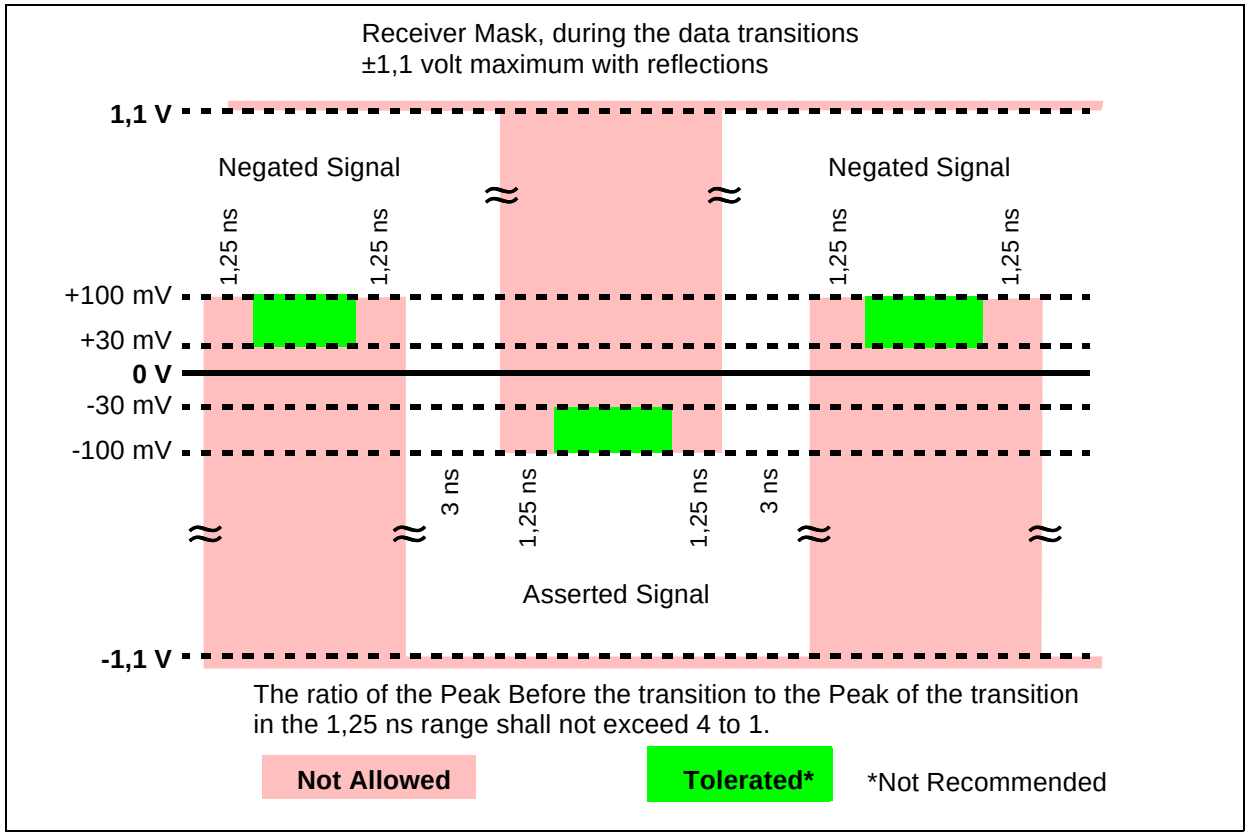


Figure 46 - LVD receiver mask =< Fast 80

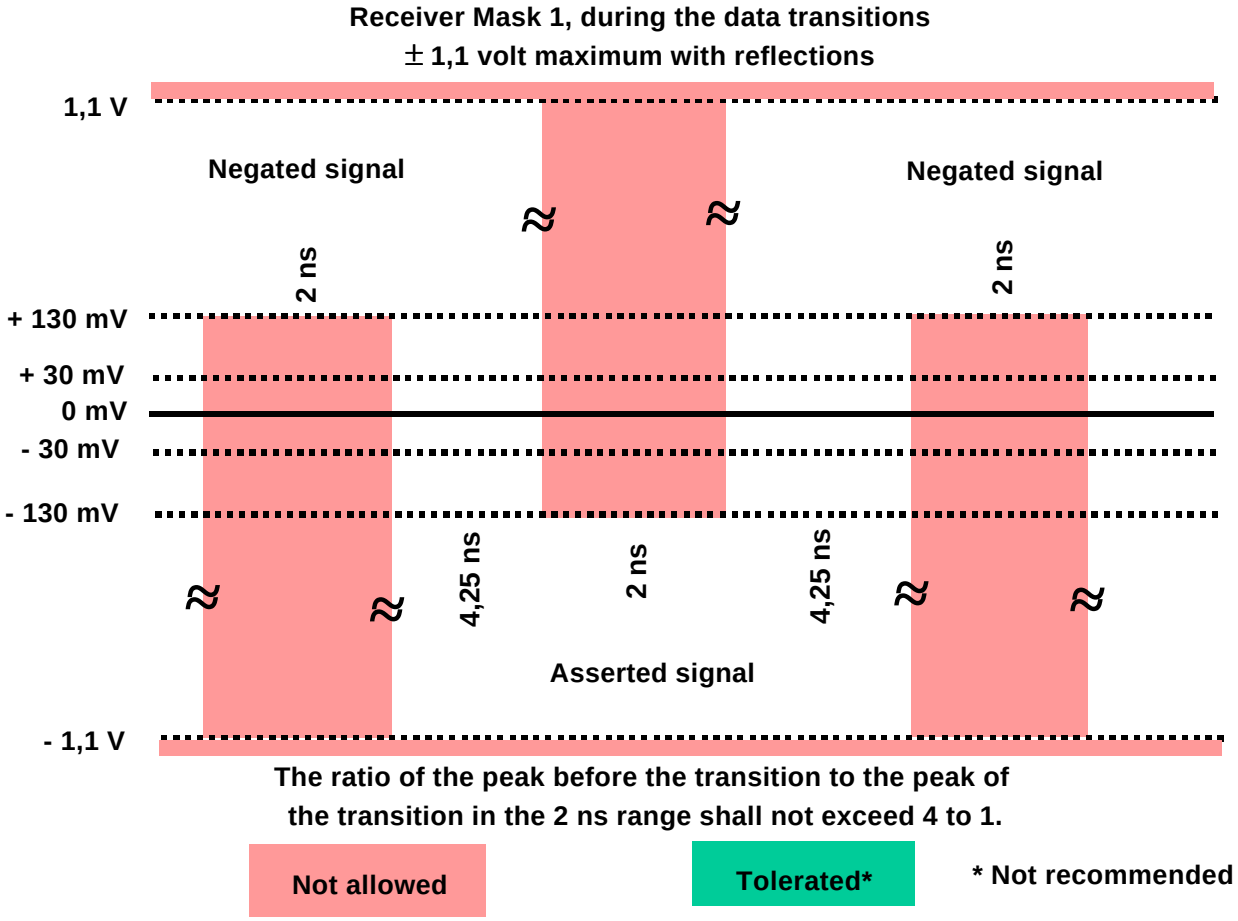


Figure 47 - LVD receiver mask 1 = Fast 160

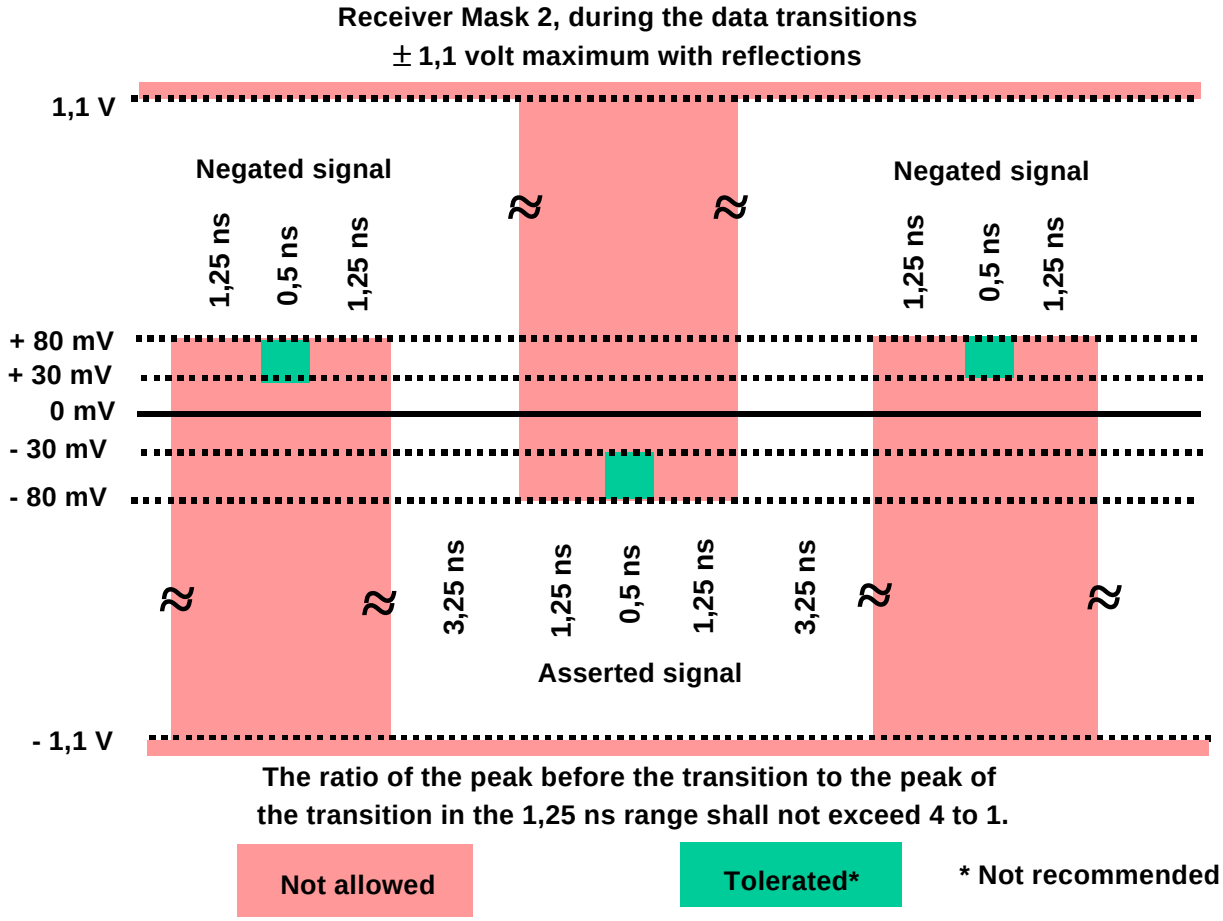


Figure 48 - LVD receiver mask 2 = Fast 160

9.5 Setup and hold timings

9.5.1 DT data transfer calculations

Figure 49 shows how the setup and hold times are calculated for various physical configurations on SCSI devices that support DT data transfers. The minimum set up and hold timings specified in figure 49 shall be used. Note that these values are different for the driver and the receiver but that the receiver sensitivity provides the threshold points for both. This is required because both extreme cases of attenuation need to be covered:

a) receivers connected to drivers with very short interconnect, and
b) receivers connected to drivers through worst case interconnect.

Figure 49 - System setup and hold timings for DT data transfers (all times in ns) (TBD)

Editors note: Will be redone when timing in Table 32 is agreed to.

9.5.1.1 DT synchronous data transfer

When a DT data transfer agreement has been established the target shall only use the DT DATA IN phase and DT DATA OUT phase for data transfers.

During DT data transfers at up to Fast-80, with the FRC_SM bit equal zero, data shall be clocked by the originating SCSI device with a clock preceding both the assertion and negation of the REQ(ACK) signal lines by half a bit period. During DT data transfers at up to Fast-80, with the FRC_SM bit equal zero, data shall be clocked by the receiving SCSI device by both the assertion and negation of the REQ and ACK signal lines. References to REQ(ACK) transitions in this subclause refer to either an assertion or a negation of the REQ or ACK signal.

During DT data transfers with the FRC_SM bit equal one, if the P1 phase established state (see TBD[9.5.1.2]) is enabled at strobe time, data shall be clocked by the originating SCSI device by both the assertion and negation of the REQ/ACK signal lines. If the P1 phase established state is disabled at strobe time, data shall not be clocked by the originating SCSI device and shall be ignored by the receiving SCSI device. The originating SCSI device shall apply driver precompensation to all the data, parity, and REQ(ACK) signals. DT data transfers with the FRC_SM bit equal one shall be clocked by the receiving SCSI device by both the assertion and negation of the REQ(ACK) signal line after having been deskewed and delayed by the receiving SCSI device.

The REQ/ACK offset specifies the maximum number of REQ transitions, with the P1 phase established state enabled if the transfer is a DATA IN transfer and the FRC_SM bit equals one, that shall be sent by the target in advance of the number of ACK transitions received from the initiator, establishing a pacing mechanism. If the number of REQ transitions exceeds the number of ACK transitions by the REQ/ACK offset, the target shall not transition the REQ signal until after the next ACK transition is received. For successful completion of the DT DATA phase the number of ACK and REQ transitions shall be equal and both REQ and ACK shall be negated.

If received pCRC and computed pCRC do not match (i.e., a pCRC error is detected), or if an improperly formatted data group is transferred, then the associated data group shall be considered invalid.

If the target does not retry transferring the information transfer or it exhausts its retry limit the target shall go into a STATUS phase and send a CHECK CONDITION status with a sense key set to ABORTED COMMAND and an additional sense code set to SCSI PARITY ERROR for the task associated with the pCRC error.

9.5.1.2 P1 Offset Control (Data pacing)

If the FRC_SM bit is equal to zero, P1 offset control shall not be used. If FRC_SM is equal to one P1 Offset Control shall be used as defined in this subclause.

At the end of the training pattern or near the start of a data phase without a training pattern, a valid data state may begin. The sending device shall indicate the valid data state by reversing the phase of the P1 signal coincident with a REQ(ACK) assertion (i.e., by withholding the next transition of P1 at the start of the first two transfer periods of valid data). Beginning with the third valid data word, P1 shall be toggled every two transfer periods, coincident with a REQ(ACK) assertion during valid data. The minimum duration of the data valid state is two transfer periods, and the data valid state shall last an even number of transfer periods.

Figure (new) illustrates an initial clock start-up period and start of valid data for a data phase.

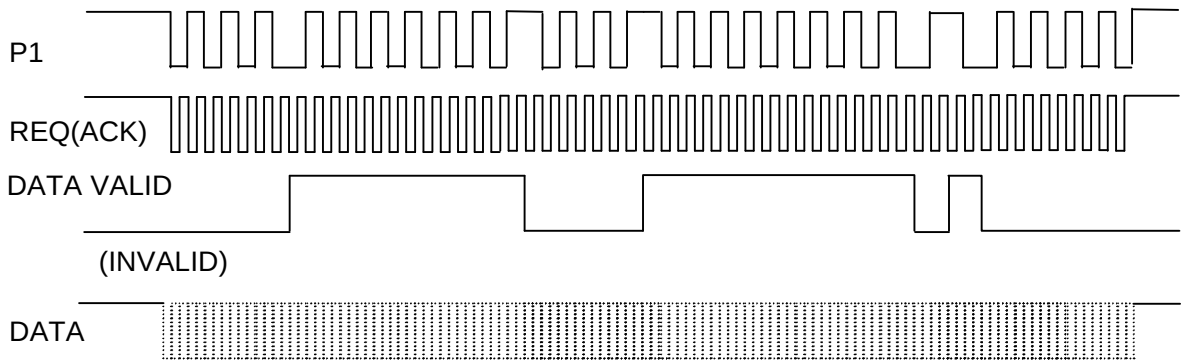


Figure 50 - P1 Offset Control (Data Pacing)

If the sending device pauses the sending of data, it shall again reverses the phase of P1 by withholding P1 transitions at the start of the first two transfer periods that do not have valid data. Beginning with the third transfer period without valid data, P1 shall be toggled every two transfer periods until valid data is sent. The data invalid state shall have at least one transition of P1 before changing states. The minimum data invalid time is four data transfer periods. This ensures a maximum run length of three cycles for P1. The data invalid state shall last an even number of transfer periods.

From the data invalid state, the sending device may resume sending data by reversing the phase of P1 again.

P1 has the same transmit setup and hold time requirements as data and shall always be detected by the receiving device on the assertion edge of the delayed clocking REQ or ACK signal.

9.5.1.3 Fast 160 Training Pattern

The training pattern shall be transferred at the start of the first data phase for each data transfer direction of an IT-Nexus when the FRC_SM bit equals one. The training pattern shall not be transferred again after the start of the first data phase for each data transfer direction of an IT-Nexus and shall not be transferred at all when the FRC_SM bit equals zero. The training pattern for Data In shall conform to Figure TBD. The training pattern for Data Out shall conform to Figure TBD. The receiving SCSI device shall use some or all elements of the training pattern to achieve deskewing. The transmitting device shall not make an intentional shift in relative timing between the databus and the REQ(ACK) signal subsequent to the training pattern during the DT data phase. The requirement to not intentionally change relative timing does not

include the effects of ISI, noise, or jitter.

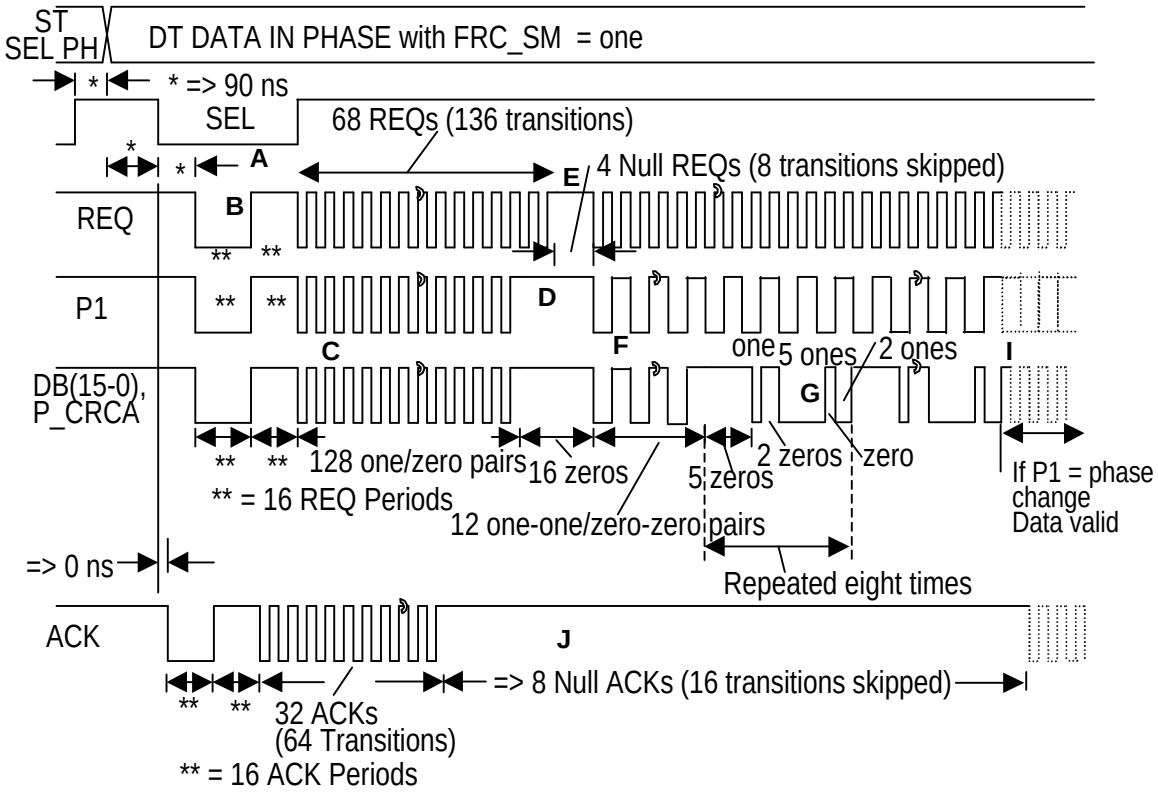


Figure 51 - Data In Training Pattern

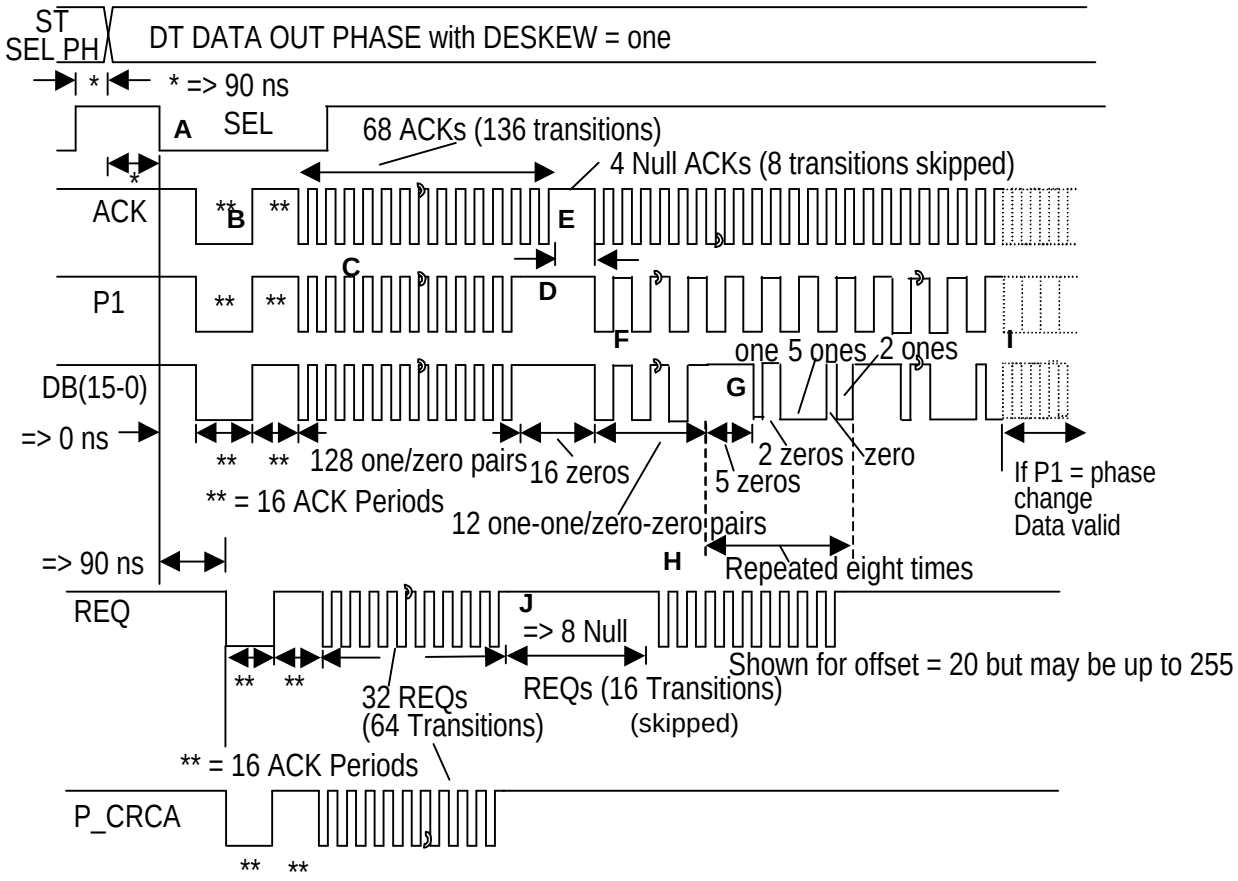


Figure 52 - Data Out Training Pattern

The training pattern elements are shown in Table (new n).

Table 32 - Training Pattern Elements

Element	Pattern	Purpose
A	SEL asserted in DT Data Phase	Signals training
B	Wide asserted followed by wide negated	Provides full cable charging
C	Alternating assertions and negations at negotiated frequency	Provides maximum frequency signal
D	8 REQ(ACK) Periods of negated	Set up deskewing
E	4 Null REQ(ACKS) of negated	Identify first REQ(ACK) for deskewing
F	12 one-one/zero-zero pairs	Deskewing
G	16 bit pattern of (0000010011111011) repeated eight times	Combination training
H	Data Out phase only a burst of REQs up to the offset agreement	Prime the pump for the initiator data transfers
I	End of eight repetition of 16 bit pattern (G)	End of training start of data transfer opportunity
J	=>8 Null REQ(ACKS) of negated	End of return REQ(ACK) training and start of start of payload REQ(ACK) opportunity

9.5.1.4 Deskewing

The deskewing technique used in the receiving SCSI device is vendor specific. Any technique that works with the SPI-4 specified training pattern and complies with the specified Receive Skew Compensation timing requirement is allowed. The training pattern is not available in Fast=<80, with FRC_SM = 0, and consequently deskewing is only used for Fast 160 with FRC_SM = 1. Deskewing shall not be used if the FRC_SM bit equals zero and shall be used if the FRC_SM bit equals one.

Editor's Note: The material after the first sentence of Deskewing may be deleted and/or moved to the model clause.

9.5.2 PARALLEL PROTOCOL REQUEST

PARALLEL PROTOCOL REQUEST messages (see table 33) are used to negotiate a synchronous data transfer agreement, a wide data transfer agreement, and set the protocol options between two SCSI devices.

Table 33 - PARALLEL PROTOCOL message format

Bit / Byte	7	6	5	4	3	2	1	0
0	EXTENDED MESSAGE (01h)							
1	EXTENDED MESSAGE LENGTH (06h)							
2	PARALLEL PROTOCOL REQUEST (04h)							
3	TRANSFER PERIOD FACTOR							
4	RESERVED							
5	REQ/ACK OFFSET							
6	TRANSFER WIDTH EXPONENT (m)							
7	P_EN	RESERVED	RESERVED	RESERVED	FRC_SM	QAS_REQ	DT_REQ	IU_REQ

The PERIOD FACTOR field is defined in table 34.

Table 34 - TRANSFER PERIOD FACTOR field

Code	Description
00h-07h	Reserved (note 1)
08h	Transfer period equals 6.25 ns (note 2). This code is only valid if the PROTOCOL OPTIONS field has a value selected that supports double-transition data transfers.
09h	Transfer period equals 12.5 ns (note 3). This code is only valid if the PROTOCOL OPTIONS field has a value selected that supports double-transition data transfers.
0Ah	Transfer period equals 25 ns (note 4)
0Bh	Transfer period equals 30,3 ns (note 4)
0Ch	Transfer period equals 50 ns (note 5)
0Dh-18h	Transfer period equals the period factor x 4 (note 5)
19h-31h	Transfer period equals the period factor x 4 (note 6)
32h-FFh	Transfer period equals the period factor x 4 (note 7)

note:
1 - Faster timings may be allowed by future SCSI parallel interface standards.
2 - Fast-160 data is latched every 6,25 ns.
3- Fast-80 data is latched every 12,5 ns.
4- Fast-40 data is latched every 25 ns or 30,3 ns.
5- Fast-20 data is latched using a transfer period of less than or equal 96 ns and greater than or equal to 50 ns.
6- Fast-10 data is latched using a transfer period of less than or equal 196 ns and greater than or equal 100 ns.
7- Fast-5 data is latched using a transfer period of less than or equal 1020 ns and greater than or equal to 200 ns

For ST synchronous data transfer the REQ/ACK OFFSET is the maximum number of REQ assertions allowed to be outstanding before a corresponding ACK assertion is received at the target. The size of a data transfer may be 1or 2 bytes depending on the values in the transfer width exponent field.

For DT synchronous data transfer the REQ/ACK OFFSET is the maximum number of REQ transitions allowed to be outstanding before a corresponding ACK transition is received at the target. The size of a data transfer shall be 2 bytes.

See 4.7 for an explanation of the differences between DT and ST data transfers.

The REQ/ACK OFFSET value is chosen to prevent overflow conditions in the SCSI device's reception buffer and offset counter. A REQ/ACK OFFSET value of zero shall indicate asynchronous data transfer mode and that the PERIOD FACTOR field and the PROTOCOL OPTIONS field shall be ignored; a value of FFh shall indicate unlimited REQ/ACK offset.

The TRANSFER WIDTH EXPONENT field defines the transfer width to be used during DATA IN phases, and

DATA OUT phases. The transfer width that is established applies to all logical units on both SCSI devices. Valid transfer widths are 8 bits (m=00h) and 16 bits (m=01h) if all the protocol options bits are zero. The only valid transfer width is 16 bits (m=01h) if any of the protocol options bits are one. TRANSFER WIDTH EXPONENT field values greater than 01h are reserved.

The protocol options bits (IU_REQ, DT_REQ, ~~and,~~ QAS_REQ, and FRC_SM) are used by the originating SCSI device to indicate the protocol options to be enabled. The responding SCSI device uses the protocol options bits to indicate the protocol options requested by the originating SCSI device the responding SCSI device has enabled.

An information units enable request bit (IU_REQ) of zero indicates that information unit transfers shall not be used (i.e., data group transfers shall be enabled) when received from the originating SCSI device and that information unit transfers are not supported when received from the responding SCSI device. An IU_REQ bit of one indicates that information unit transfers shall be used when received from the originating SCSI device and that information unit transfers are supported when received from the responding SCSI device. If the IU_REQ bit is changed from the previous agreement (i.e., zero to one or one to zero) as a result of a negotiation the target shall go to a BUS FREE phase on completion of the negotiation.

A DT enable request bit (DT_REQ) of zero indicates that DT DATA phases are to be disabled when received from the originating SCSI device and that DT DATA phases are not supported when received from the responding SCSI device. An DT_REQ bit of one indicates that DT DATA phases are to be enabled when received from the originating SCSI device and that DT DATA phases are supported when received from the responding SCSI device.

A QAS enable request bit (QAS_REQ) of zero indicates that QAS is to be disabled when received from the originating SCSI device and that QAS is not supported when received from the responding SCSI device. An QAS_REQ bit of one indicates that QAS is to be enabled when received from the originating SCSI device and that QAS is supported when received from the responding SCSI device.

The FRC_SM bit shall be cleared to zero for **TRANSFER PERIOD FACTOR** field values larger than 08h. A a free running clock and skew management bit (FRC_SM) of zero indicates that:

a) the transmitting SCSI device shall transfer the data, during a data phase, with the REQ(ACK) strobe offset by half of a Data Transfer period and that the receiving SCSI device shall not use deskewing.
b) the transmitting SCSI device shall us the REQ(ACK) signal for offset control (data pacing).

The FRC_SM bit shall be set to one for **TRANSFER PERIOD FACTOR** field values of 08h. A FRC_SM BIT of one indicates that:

a) the transmitting SCSI device shall transfer the data, during a data phase, with the REQ(ACK) strobe synchronized in time with the nominal Data Transfer transition
b) the receiving SCSI device shall use deskewing.
c) the transmitting SCSI device shall not use the REQ(ACK) signal for offset control (data pacing).
d) the transmitting SCSI device shall use phase changes of the P1 signal for offset control (data pacing).

The protocol option bit Parity Enable (P_EN) issued by the PPR originating SCSI device to request the state of data phase driver precompensation to be used by the responding SCSI device. The responding SCSI device uses the protocol option bit P_EN to request the state of data phase driver precompensation to be used by the originating SCSI device. SCSI devices that support Fast 160 shall support receipt, but may not transmit, of both states of the P_EN bit. The P_EN bit shall be cleared to zero by both devices for Fast =< 80.

For Fast 160, if the PPR originating SCSI device clears the P_EN bit to zero the responding SCSI device shall not use driver precompensation. If the PPR originating SCSI device sets the P_EN bit to one the responding SCSI device shall use driver precompensation during the data phase. If the responding SCSI

device clears the P_EN bit to zero the originating SCSI device shall not use driver precompensation. If the responding SCSI device sets the P_EN bit to one the PPR originating SCSI device shall use driver precompensation during the data phase. For Fast 160 the SCSI device that sets or clears the P_EN bit is not indicating whether or not that SCSI will use driver precompensation and the two SCSI devices may set or clear the P_EN bit differently during the PPR protocol according to the signal conditions the devices are requesting to be received.

Not all combinations of the protocol options bits are valid. Only the bit combinations defined in table 35 shall be allowed. All other combinations are reserved.

Table 35 - Valid protocol options bit combinations

P_EN	FRC_SM	QAS_REQ	DT_REQ	IU_REQ	Description
0	0	0	0	0	Use ST DATA IN and ST DATA OUT phases to transfer data, data and REQ(ACK) out of phase, offsets allowed using REQ(ACK), and no precompensation.
0	0	0	1	0	Use DT DATA IN and DT DATA OUT phases with data group transfers, data and REQ(ACK) out of phase, offsets allowed using REQ(ACK), and no precompensation.
0	0	0	1	1	Use DT DATA IN and DT DATA OUT phases with information unit transfers, data and REQ(ACK) out of phase, offsets allowed using REQ(ACK), and no precompensation.
0	0	1	1	1	Use DT DATA IN and DT DATA OUT phases with information unit transfers and use QAS for arbitration, data and REQ(ACK) out of phase, offsets allowed using REQ(ACK), and no precompensation.
0	1	0	1	0	Use DT DATA IN and DT DATA OUT phases with data group transfers, data and REQ(ACK) in phase, offsets controlled by P1, and not using precompensation.
0	1	0	1	1	Use DT DATA IN and DT DATA OUT phases with information unit transfers, data and REQ(ACK) in phase, offsets controlled by P1, and not using precompensation.
0	1	1	1	1	Use DT DATA IN and DT DATA OUT phases with information unit transfers and use QAS for arbitration, data and REQ(ACK) in phase, offsets controlled by P1, and not using precompensation.
1	1	0	1	0	Use DT DATA IN and DT DATA OUT phases with data group transfers, data and REQ(ACK) in phase, offsets controlled by P1, and using precompensation.
1	1	0	1	1	Use DT DATA IN and DT DATA OUT phases with information unit transfers, data and REQ(ACK) in phase, offsets controlled by P1, and using precompensation.
1	1	1	1	1	Use DT DATA IN and DT DATA OUT phases with information unit transfers and use QAS for arbitration, data and REQ(ACK) in phase, offsets controlled by P1, and using precompensation.

A PARALLEL PROTOCOL REQUEST agreement applies to all logical units of the two SCSI devices that negotiated agreement. That is, if SCSI device A, acting as an initiator negotiates a data transfer agreement with SCSI device B (a target), then the same data transfer agreement applies to SCSI devices A and B even if SCSI device B changes to an initiator.

A data transfer agreement only applies to the two SCSI devices that negotiate the agreement. Separate

data transfer agreements are negotiated for each pair of SCSI devices. The data transfer agreement only applies to DATA phases and information unit transfers.

A PARALLEL PROTOCOL REQUEST message exchange shall be initiated by a SCSI device whenever a previously arranged parallel protocol agreement may have become invalid. The agreement becomes invalid after any condition that may leave the parallel protocol agreement in an indeterminate state such as:

a) after a hard reset;
b) after a TARGET RESET message;
c) after a power cycle;
d) after a change in the transceiver mode (e.g., LVD mode to SE mode).

Any condition that leaves the data transfer agreement in an indeterminate state shall cause the SCSI device to enter an asynchronous, eight-bit wide data transfer mode with all the protocol options bits set to set to zero.

A SCSI device may initiate a PARALLEL PROTOCOL REQUEST message exchange whenever it is appropriate to negotiate a data transfer agreement. SCSI devices that are currently capable of supporting any of the PARALLEL PROTOCOL REQUEST options shall not respond to a PARALLEL PROTOCOL REQUEST message with a MESSAGE REJECT message.

Renegotiation after every selection is not recommended, since a significant performance impact is likely.

The PARALLEL PROTOCOL REQUEST message exchange establishes an agreement between the two SCSI devices;

a) on the permissible periods and the REQ/ACK offsets for all logical units on the two SCSI devices. This agreement only applies to ST DATA IN phases, ST DATA OUT phases, DT DATA IN phases, and DT DATA OUT phases. All other phases shall use asynchronous transfers;
b) on the width of the data path to be used for DATA phase transfers between two SCSI devices. This agreement only applies to ST DATA IN phases, ST DATA OUT phases, DT DATA IN phases, and DT DATA OUT phases. All other information transfer phases shall use an eight-bit data path; and
c) on the protocol option is to be used.

The originating SCSI device (the SCSI device that sends the first of the pair of PARALLEL PROTOCOL REQUEST messages) sets its values according to the rules above to permit it to receive data successfully. If the responding SCSI device is able to receive data successfully with these values (or smaller periods or larger REQ/ACK offsets or both), it returns the same values in its PARALLEL PROTOCOL REQUEST message. If it requires a larger period, a smaller REQ/ACK offset, or a smaller transfer width in order to receive data successfully, it substitutes values in its PARALLEL PROTOCOL REQUEST message as required, returning unchanged any value not required to be changed. Each SCSI device when transmitting data shall respect the negotiated limits set by the other's PARALLEL PROTOCOL REQUEST message, but, if the FRC_SM bit is set to zero, it is permitted to transfer data with larger periods, smaller synchronous REQ/ACK offsets, or both. Each SCSI device when transmitting data shall respect the negotiated limits set by the other's PARALLEL PROTOCOL REQUEST message, but, if the FRC_SM bit is set to one, it shall not use a larger data transfer period although it is permitted to transfer data with ~~larger periods,~~ smaller synchronous REQ/ACK offsets~~, or both~~. The completion of an exchange of PARALLEL PROTOCOL REQUEST messages implies an agreement as shown in table 36.

If the responding SCSI device does not support the selected protocol option it shall clear as many bits as required to set the protocol option field to a legal value that it does support.

Table 36 - PARALLEL PROTOCOL REQUEST messages implied agreements

Responding SCSI device PARALLEL PROTOCOL REQUEST response	Implied agreement
Non-zero REQ/ACK offset	Synchronous transfer (i.e., Each SCSI device transmits data with a period equal to or greater than and a REQ/ACK offset equal to or less than the negotiated values received in the responding SCSI device's PPR message).
REQ/ACK offset equal to zero	Asynchronous transfer
Non-zero TRANSFER WIDTH EXPONENT	Wide transfer (i.e., the initiator and the target transmit data with a transfer width equal to the responding device's transfer width). If the initiating SCSI device does not support the responding SCSI device's TRANSFER WIDTH EXPONENT then the initiating SCSI device shall MESSAGE REJECT the PARALLEL PROTOCOL REQUEST message (see 7.9.9.1 and 7.9.9.2).
TRANSFER WIDTH equal to zero	Eight-bit data
protocol options equal to 0h and transfer period factor equal to 9h	Eight-bit/asynchronous data transfer with PROTOCOL OPTIONS field set to 0h
IU_REQ, DT_REQ, and QAS_REQ equal to zero	ST DATA IN and ST DATA OUT phases to transfer data
P_EN bit equal to zero	Precompensation not used by the other SCSI device
P_EN bit equal to one	Precompensation used by the other SCSI device
DT_REQ equal to one	DT DATA IN and DT DATA OUT phases to transfer data with iuCRC
IU_REQ, and DT_REQ equal to one	DT DATA IN and DT DATA OUT phases with information units
IU_REQ, DT_REQ, and QAS_REQ equal to one	DT DATA IN and DT DATA OUT phases with information units and use QAS for arbitration
FRC_SM bit equal to one	Free running clock, deskewing, and P1 phase pacing used
MESSAGE REJECT message	Eight-bit/asynchronous data transfer with protocol options field set to 0h
Parity error (on responding message)	Eight-bit/asynchronous data transfer with PROTOCOL OPTIONS field set to 0h
Unexpected bus free (as a result of the responding message)	Eight-bit/asynchronous data transfer with PROTOCOL OPTIONS field set to 0h
No response	Eight-bit/asynchronous data transfer with protocol options field set to 0h

If there is an unrecoverable parity error on the initial PARALLEL PROTOCOL REQUEST message (see 10.9.1 and 10.9.2) the initiating SCSI device shall retain its previous data transfer mode and protocol options. If there is an unexpected bus free on the initial PARALLEL PROTOCOL REQUEST message the initiating SCSI device shall retain its previous data transfer mode and protocol options.

Annex A Additional requirements for LVD SCSI drivers and receivers

(normative)

A.1 System level requirements

The requirements for LVD SCSI drivers and receivers in this annex are based on the system level requirements stated in table A.1. Some of these requirements are specifically called out in other subclauses while others are derived from bus loading conditions and trade-offs between competing parameters.

Table A.1 - System level requirements

Parameter	Minimum	Maximum	Cross-reference
V_A (except OR-tied signals)	-1 V	- 80 mV	note 1
V_N (except OR-tied signals)	80 mV	1 V	note 1
V_A (OR-tied signals)	-3,6 V	- 80 mV	note 1
V_N (OR-tied signals)	100 mV	125 mV	note 1
attenuation (%)		15	note 2
loaded media impedance (Ohms)	85	135	note 3
unloaded media impedance (Ohms)	110	135	subclause 6.3
terminator bias (mV)	100	125	subclause 7.3.1
terminator impedance (Ohms)	100	110	subclause 7.3.1
device leakage (µA)	-20	20	table 16
number of SCSI devices	2	16	subclause 4.7
ground offset level (mV)	-355	355	note 4

Note:
1 -These are the signal levels at the receiver, the system allows 60 mV crosstalk for calculating the minimum driver level.
2 -Measured from the driver to the farthest receiver.
3 -Caused by the addition of device capacitive load (see table 9 for calculations).
4 -This is the difference in voltage signal commons for SCSI devices on the bus (see figure 3).

A.2 Driver requirements

A.2.1 Driver requirements overview

The fundamental requirement for an LVD driver is the generation of a first-step differential output voltage magnitude at the driver connections to the balanced media to achieve required minimum differential signals at every receiver connection to the bus. In order to minimize ISI during data transfer phases while controlling power requirements, if the P_EN bit received from the other SCSI device during the prior PPR negotiation equaled one, the driver amplitude shall be cutback (reduced) by a minimum of 15% to a maximum of 40% after the first bit of a series of adjacent ones or adjacent zeros. Other characteristics that affect overall noise margin are the common-mode output voltage, the maximum differential output voltage, the driver output impedance, and the output signal wave shape.

The driver requirements are defined in terms of the voltages and currents depicted in figure 42.

A.2.2 Differential output voltage, V_S

This subclause does not specify requirements for drivers with source impedances less ~~then~~ than 1000 Ohms.

To assure sufficient voltage to define a valid logic state at any device connection on a fully loaded LVD bus at least a minimum differential output voltage shall be generated. This value shall be large enough that, after allowance for attenuation (AC and DC), reflections, terminator bias difference, and differential noise coupling, V_S is at least $\pm$100 mV at the device connector to the LVD SCSI bus.

The SCSI device shall also comply with the upper limits for the differential output voltages and to the symmetry of the differential output voltage magnitudes between logic states in order to assure a first-step transition to the opposite logic state.

With the test circuit of figure A.1 and the test conditions V1 and V2 in table A.2 applied, the steady-state magnitude of the differential output voltage, V_S, for an asserted state (V_A), shall be greater than or equal to 320 mV and less than or equal to 800 mV. For the negated state, the polarity of V_S shall be reversed (V_N) and the differential voltage magnitude shall be greater than or equal to 320 mV and less than or equal to 800 mV. The relationship between V_A and V_N specified in table A.2 and shown graphically in figure A.2 shall be maintained.

The assertion drivers and negation drivers require different strengths to achieve the near equality in V_A and V_N shown in figure A.2 because the applied V1 and V2 simulate the effects of the bus termination bias.

Table A.2 - Driver steady-state test limits and conditions and alternating 1/0 data transfer phase

Test parameter	Test conditions (figure A.1)[1]	Minimum (mV)[2]	Maximum (mV)
$\lvert V_A \rvert$ Differential output voltage magnitude (asserted) (note)	V_1 = 1,056 V V_2 = 0,634 V	320	800
	V_1 = 1,866 V V_2 = 1,444V	320	800
$\lvert V_N \rvert$ Differential output voltage magnitude (negated) (note)	V_1 = 1,056 V V_2 = 0,634 V	320	800
	V_1 = 1,866 V V_2 = 1,444V	320	800
$\lvert V_A \rvert$ Differential output voltage magnitude (asserted)	All four above conditions	0,69 x $\lvert V_N \rvert$ + 50	1,45 x $\lvert V_N \rvert$ - 65

Notes:
1)The test circuit (figure A.1) is approximately equivalent to two terminators creating the normal system bias.
2) Including cutback.
3) The test limits shall be within the shaded domain of Figure A.2.

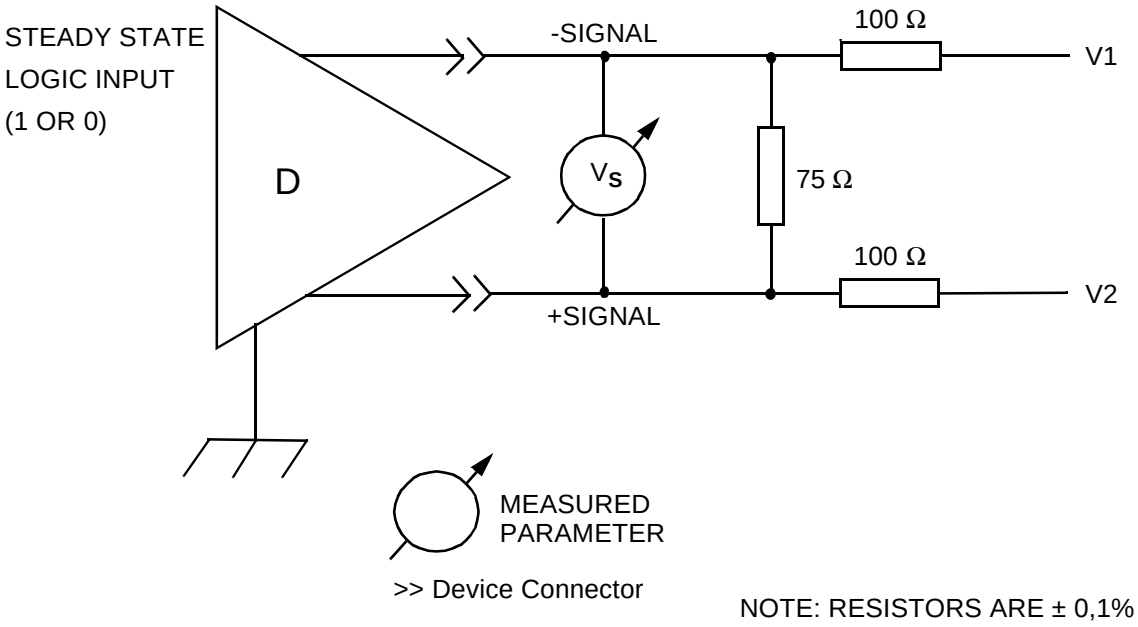


Figure A.1 - Differential steady-state output voltage test circuit

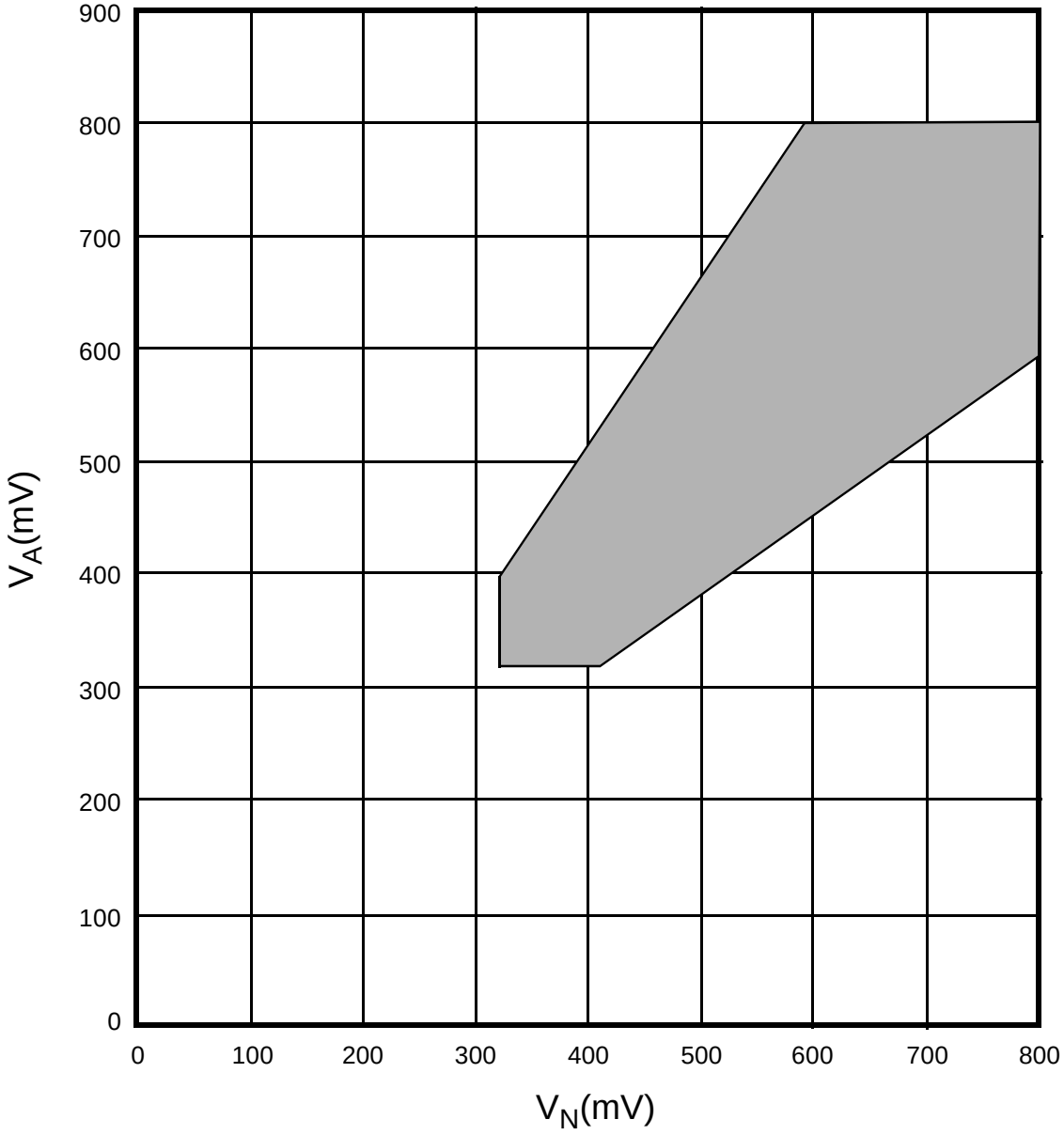


Figure A.2 - Domain for driver assertion and negation levels

Editor's Note: Additional Fast-160 analysis needs to be done regarding the limits of Figure A.2 and receiver analysis.

A.2.3 Offset (common-mode output) voltage, V_{CM}

A.2.4 Short-circuit currents, I_{O-S} and I_{O+S}

A.2.5 Open-circuit output voltages, $V_{O-(OC)}$ and $V_{O+(OC)}$

A.2.6 Output signal waveform

The differential output rise or fall time of a driver is specified since they influence the timing measurements and stub lengths of an LVD interface. Excessive over and under shoot of the output signal may cause

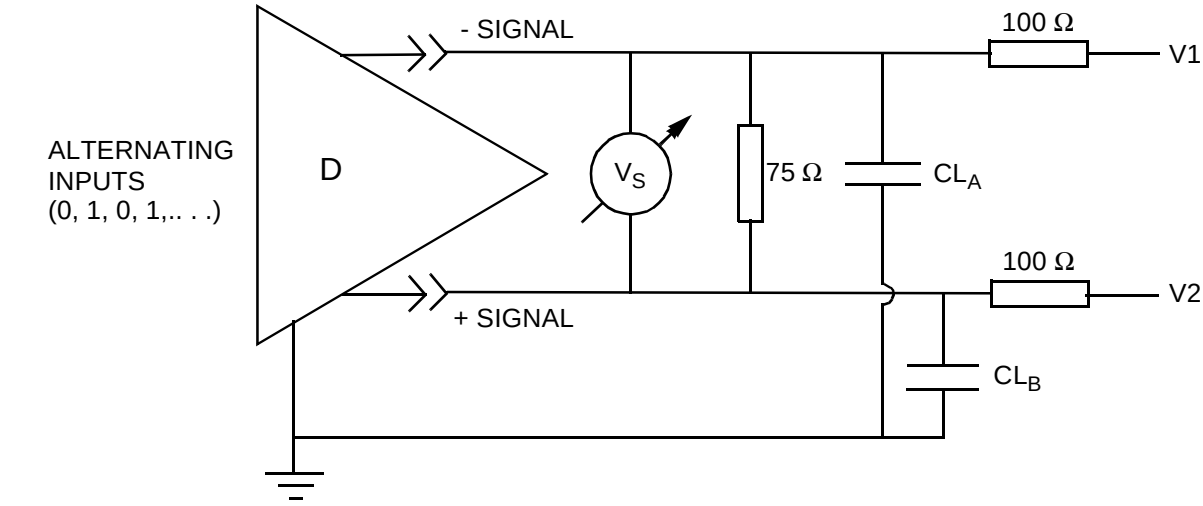
electromagnetic emissions or false logic state changes.

During transitions of the driver output between alternating logical states (one - zero, zero - one, one - off, off - one, zero - off, off - zero), the differential voltage measured with the test circuit of figure A.3 and table A.3, shall be such that the voltage monotonically changes between 0,2 and 0,8 of the steady-state output, V_{SS}. V_{SS} is defined as the voltage difference between the two steady-state values of the driver output ($V_{SS} = |V_A| + |V_N|$) (See figure A.4 and table A.2). V_{SS} is expected to be different for different transitions.

The output signal rise or fall times (see t_r in figure A.4) between 0,2 and 0,8 of V_{SS} shall be between 1 ns and 2,5 ns.

The rise and fall times specified above are requirements for a driver when using the LVD test circuit in figure A.3. They are not the observed rise or fall rates on an actual SCSI bus.

Measurement equipment used for rise and fall rate testing shall provide a bandwidth of 2 GHz minimum.



Notes:

a) Resistors are ±1% and surface-mount metal film type.
b) CL_A and CL_B are 5 pF ±0,2 pF and include the instrumentation capacitance.
c) The longest physical dimension between the device connector pins and any test circuit component shall be no greater than 0,1 meter.
d) V1 and V2 are applied voltages from a source having a source impedance of less than 5 Ω from 0 Hz to 80 MHz.

Figure A.3 - Differential output switching voltage test circuit

Table A.3 - Driver switching test circuit parameters

Test condition (see figure A.3)	V1	V2
Low common-mode voltage	1,311 V	0,889 V
High common-mode voltage	1,611 V	1,189 V

The signal voltage shall comply with the requirements shown in figure A.4.

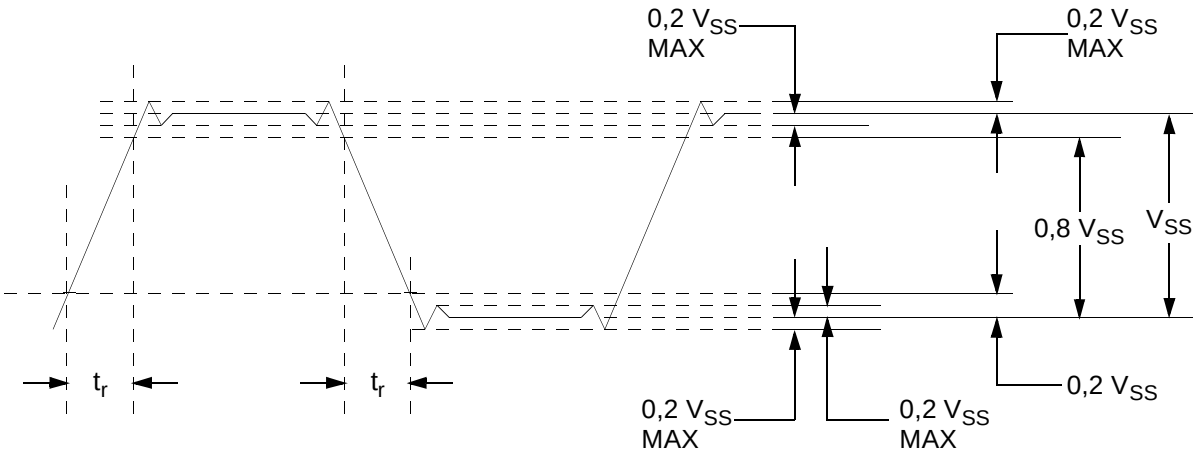


Figure A.4 - Driver output signal waveform