T10/99-295r1

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10/31/99

John Lohmeyer
T10 Chairman

Subject: **Proposal for Fast-160 to be included in SPI-4**

Revision on of this proposal incorporates changes based upon the October SPI-4 working group meeting. The enclosed proposal addresses Fast-160 and introduces the concept (PPR code) for Fast-120 as an intermediate negotiation. Specifics are given for Fast-160. Specifics for Fast-120 are left as an action item after agreement on the specifics of Fast-160. It is assumed that Fast-120 is a scaling of Fast-160. Additional intermediate steps are not proposed due to the issues of providing additional clocks and/or additional compensation delays.

The key elements of the proposal are similar to descriptions made in recent T10 presentations with the intent of packaging the elements of Fast-160 in a single package as T10 agreements are reached pending an initial SPI-4 draft with Fast-160 included. Discussion at the October meeting indicated that a free running clock should be added since even if some environments do not need it other environments will exist that need it.

The key elements of this document as revised are: ISI precompensation (exact technique vendor specific); standard training pattern for each Fast-160 DT data phase; REQ/ACK continuous during Fast-160 DT data phases; P1 used for flow control; and deskewing (exact technique vendor specific).

The method for Fast-160 terminators to detect DT data phases to remove bias voltage in revision 0 was removed since it did not distinguish lower rate DT data phases. The data to date does not yet show whether or not the removal of the bias voltage will be required and thus whether new Fast-160 terminators should be required even if desirable.

Revision one adds an additional Fast-160 timing budget table using a different format for grouping the items. A Fast-80 reference column is included, at least during development of the standard, for comparison. It is anticipated that additional timing factors may be included in an informative annex to track how the timing budget was constructed (e.g., see William Petty's 99-261r2). Revision one changes are marked with change bars. All changes from SPI-3 Revision 10 are marked with underlines and strike-outs.

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p.s. Although the SPI-3 files were used, clause numbers, figure numbers, and table numbers are as FrameMaker determined and have not been synchronized exactly to SPI-3. New timing terms were placed at the end of the definitions rather than scattered alphabetically. Correcting these format differences could be fun and games for the SPI-4 technical editor. Since time to wrestle with FrameMaker was finite, some

figure cleanup was left also for editor amusement.

8 Adjust clause number to ballpark for clause 9 stuff

Table 28 - Transceiver/speed support map

Transceiver	Maximum transfer rate						
	Async.	**Fast-5**	**Fast-10**	**Fast-20**	**Fast-40**	**Fast-80**	**Fast-160**
SE	yes	yes	yes	yes	no	no	no
MSE (Note)	yes	yes	yes	yes	no	no	no
LVD (ST)	yes	yes	yes	yes	yes	no	no
LVD (DT)	no	no	yes	yes	yes	yes	yes
Key: yes = Transceiver/speed combination supported by this standard. No =Transceiver/speed combination not supported by this standard.							
Note-MSE is identical to SE except for the requirements in 7.4, table 16, and table 17.							

9 Adjust clause number to ballpark

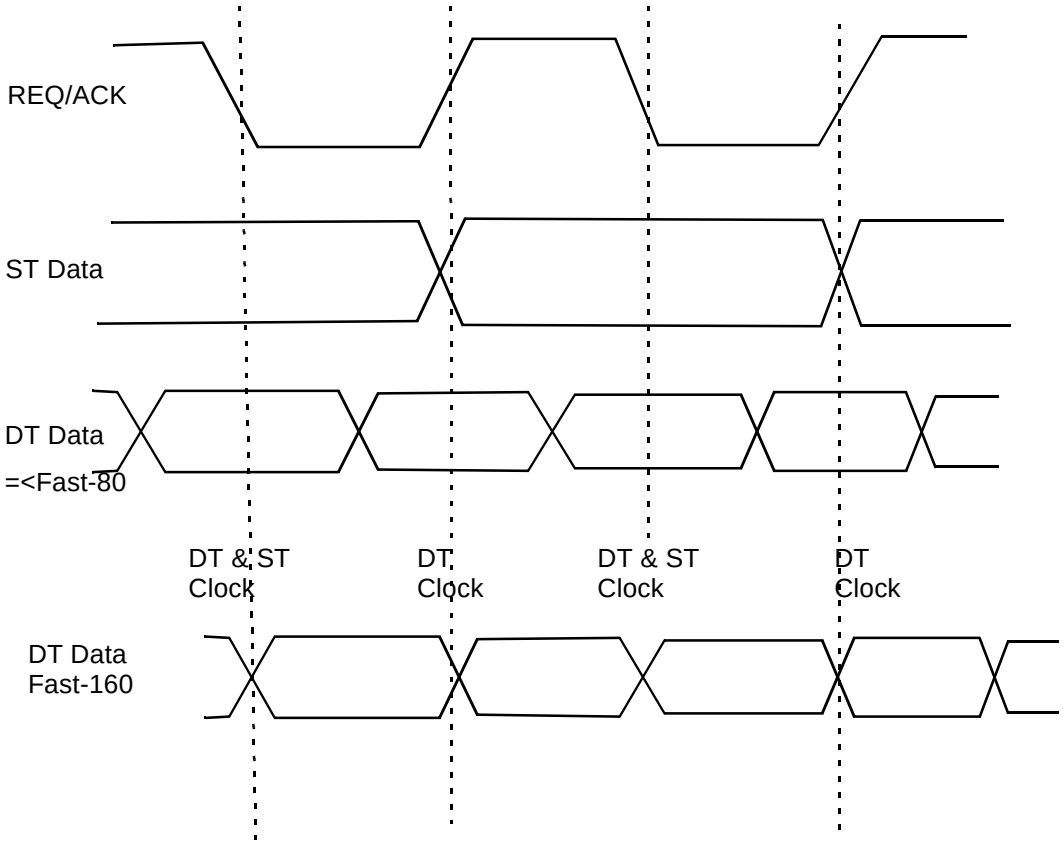


Figure 42 - ST latching data vs. DT latching data

Table 29 - LVD maximum bus path length between terminators

Interconnect	Maximum bus path length between terminators (meters) (note 1)					
	Fast-5	Fast-10	Fast-20	Fast-40	Fast-80	Fast-160
Point-to-point interconnect	25	25	25	25	25	25
Multidrop interconnect	12	12	12	12	12	12

Note:
1 For environments where all elements of the bus (cables, device interfaces, environmental noise and other values) are controlled to be better than minimally required, it may be possible to extend the path length and SCSI device count (see note 10 in 7.2.4). But compliance to the standard shall not be required.

(Eliminated LVD termination change)

9.1 Adjust clause number to ballpark

9.2 Timing description

9.3 SCSI parallel bus timing values (Table 30 & 31 not changed yet but will change)

Table 30 - SCSI bus data & information phase DT timing values (Fast-160 First Method)

Clause	Timing description	Timing Values (note 4)				
		Fast-10	Fast-20	Fast-40	Fast-80	Fast-160
9.2.2Table 31:	ATN Transmit Setup Time	48,4 ns	29,2 ns	19,6 ns	14,8 ns	11,675 ns
9.2.3	ATN Receive Setup Time	13,6 ns	7,8 ns	4,9 ns	3,45 ns	2,95 ns
9.3.1	Cable Skew (note 1)	4 ns	3 ns	2,5 ns	2,5 ns	2,5 ns
9.3.2	pCRC Receive Hold Time (note 5)	11,6 ns	5,8 ns	2,9 ns	1,45 ns	(2,175) ns
9.3.3	pCRC Receive Setup Time (note 5)	18,6 ns	12,8 ns	9,9 ns	8,45 ns	1,825 ns
9.3.4	pCRC Transmit Hold Time (note 5)	38,4 ns	19,2 ns	9,6 ns	4,8 ns	1,675 ns
9.3.5	pCRC Transmit Setup Time (note 5)	48,4 ns	29,2 ns	19,6 ns	14,8 ns	6,675 ns
9.3.6	Receive Assertion Period (note 2)	80 ns	40 ns	20 ns	10 ns	5 ns
9.3.7	Receive Hold Time (note 2 and note 3) (note 5)	11,6 ns	5,8 ns	2,9 ns	1,45 ns	(2,175) ns
9.3.8	Receive Negation Period (note 2)	80 ns	40 ns	20 ns	10 ns	5 ns
9.3.9	Receive Setup Time (note 2 and note 3) (note 5)	11,6 ns	5,8 ns	2,9 ns	1,45 ns	(2,175) ns
9.3.10	Receive REQ (ACK) Period Tolerance	0,7 ns	0,7 ns	0,7 ns	0,7 ns	0,7 ns
9.3.11	Receive REQ Assertion Period with P_CRCA transitioning	85,5 ns ?	48 ns ?	32,5 ns ?	22,5 ns ?	TBD
9.3.12	Receive REQ Negation Period with P_CRCA transitioning	85,5 ns ?	48 ns ?	32,5 ns ?	22,5 ns ?	TBD
9.3.14	Signal Timing Skew (note 5)	26,8 ns	13,4 ns	6,7 ns	3,35 ns	3,85 ns
9.3.13	REQ (ACK) Period	200 ns	100 ns	50 ns	25 ns	12,5 ns
9.3.17	Transmit Assertion Period (note 2)	92 ns	46 ns	23 ns	11,5 ns	5,75 ns
9.3.16	Transmit Hold Time (note 2 and note 3) (note 5)	38,4 ns	19,2 ns	9,6 ns	4,8 ns	1,675 ns
9.3.17	Transmit Negation Period (note 2)	92 ns	46 ns	23 ns	11,5 ns	5,75 ns
9.3.18	Transmit Setup Time (note 2 and note 3)	38,4 ns	19,2 ns	9,6 ns	4,8 ns	1,675 ns
9.3.19	Transmit REQ (ACK) Period Tolerance	0,6 ns	0,6 ns	0,6 ns	0,6 ns	0,6 ns

Notes:
1 Cable Skew is measured at each SCSI device connection with the transmitted skew subtracted from the received skew.
2 See 9.4 for measurement points for the timing specifications.
3 See 9.5 for examples of how to calculate setup and hold timing.
4 SCSI bus timing values specified by the maximum transfer rate for the given range shall apply even if a slower transfer rate within the given range is negotiated.
5 Calculated without the benefit of ISI compensation and before skew compensation.
6 Calculated with the benefit of ISI compensation and skew compensation.

Table 30 - SCSI bus data & information phase DT timing values (Fast-160 First Method)

Clause	Timing description	Timing Values (note 4)				
		Fast-10	Fast-20	Fast-40	Fast-80	Fast-160
9.3.20	Transmit REQ Assertion Period with P_CRCA transitioning	97,5 ns	54 ns	35,5 ns	24 ns	TBD
9.3.21	Transmit REQ Negation Period with P_CRCA transitioning	97,5 ns	54 ns	35,5 ns	24 ns	TBD
	Transmit ISI Compensation	Note 5	Note 5	Note 5	Note 5	0,8 ns
	Receive Skew Compensation	N/A	N/A	N/A	N/A	4,15
	Strobe Offset Tolerance	N/A	N/A	N/A	N/A	1,0 ns
	Net Receive Internal Setup/Hold Time (note 6)	10,15 to 10,95 ns	4,35 to 5,15 ns	1,45 to 2,25 ns	0 to 0,8 ns	0,325 ns

Notes:
1 Cable Skew is measured at each SCSI device connection with the transmitted skew subtracted from the received skew.
2 See 9.4 for measurement points for the timing specifications.
3 See 9.5 for examples of how to calculate setup and hold timing.
4 SCSI bus timing values specified by the maximum transfer rate for the given range shall apply even if a slower transfer rate within the given range is negotiated.
5 Calculated without the benefit of ISI compensation and before skew compensation.
6 Calculated with the benefit of ISI compensation and skew compensation.

Table 31: SCSI bus data & information phase DT timing values (Fast-160 Second Method)

Clause	Timing description	Timing Values (note 4)			
		Fast-80	Fast-160	RCVR Internal	After, ISIC, Offset & Deskew
9.2.2Table 31:	ATN Transmit Setup Time	14,8 ns	8,55 ns		
9.2.3	ATN Receive Setup Time	3,45 ns	4,7 ns	2,75 ns	2,75 ns
9.3.1	Cable Skew (note 1)	2,5 ns	2,5 ns		
9.3.2	pCRC Receive Hold Time (note 5)	1,45 ns	0,95 ns	(0.5) ns	0,325 ns
9.3.3	pCRC Receive Setup Time (note 5)	8,45 ns	2,55 ns	1,10 ns	8,175 ns
9.3.4	pCRC Transmit Hold Time (note 5)	4,8 ns	4,8 ns		
9.3.5	pCRC Transmit Setup Time (note 5)	14,8 ns	8,550 ns		
9.3.6	Receive Assertion Period (note 2)	10 ns	5 ns		
9.3.7	Receive Hold Time (note 2 and note 3) (note 5)	1,45 ns	0,95 ns	(0.5) ns	0,325 ns
9.3.8	Receive Negation Period (note 2)	10 ns	5 ns		
9.3.9	Receive Setup Time (note 2 and note 3) (note 5)	1,45 ns	(5,3) ns	(6.75)	0,325 ns
9.3.10	Receive REQ (ACK) Period Tolerance	0,7 ns	0,7 ns		
9.3.11	Receive REQ Assertion Period with P_CRCA transitioning	22,5 ns ?	TBD		
9.3.12	Receive REQ Negation Period with P_CRCA transitioning	22,5 ns ?	TBD		
9.3.14	Signal Timing Skew (note 5)	3,35 ns	3,85 ns		
9.3.13	REQ (ACK) Period	25 ns	12,5 ns		
9.3.17	Transmit Assertion Period (note 2)	11,5 ns	5,75 ns		
9.3.16	Transmit Hold Time (note 2 and note 3) (note 5)	4,8 ns	4,8 ns		
9.3.17	Transmit Negation Period (note 2)	11,5 ns	5,75 ns		
9.3.18	Transmit Setup Time (note 2 and note 3)	4,8 ns	(1,45) ns		

Notes:
1 Cable Skew is measured at each SCSI device connection with the transmitted skew subtracted from the received skew.
2 See 9.4 for measurement points for the timing specifications.
3 See 9.5 for examples of how to calculate setup and hold timing.
4 SCSI bus timing values specified by the maximum transfer rate for the given range shall apply even if a slower transfer rate within the given range is negotiated.
5 Calculated without the benefit of ISI compensation and before skew compensation.
6 Calculated with the benefit of ISI compensation and skew compensation.

Clause	Timing description	Timing Values (note 4)			
		Fast-80	Fast-160	RCVR Internal	After, ISIC, Offset & Deskew
9.3.19	Transmit REQ (ACK) Period Tolerance	0,6 ns	0,6 ns		
9.3.20	Transmit REQ Assertion Period with P_CRCA transitioning	24 ns	TBD		
9.3.21	Transmit REQ Negation Period with P_CRCA transitioning	24 ns	TBD		
	Transmit ISI Compensation	Note 5	0,8 ns		
	Receive Skew Compensation	N/A	4,15		
	Strobe Offset Tolerance	N/A	1,0 ns		
	Net Receive Internal Setup/Hold Time (note 6)	0 to 0,8 ns		(6.75)/(0.5)	0.325

Notes:
1 Cable Skew is measured at each SCSI device connection with the transmitted skew subtracted from the received skew.
2 See 9.4 for measurement points for the timing specifications.
3 See 9.5 for examples of how to calculate setup and hold timing.
4 SCSI bus timing values specified by the maximum transfer rate for the given range shall apply even if a slower transfer rate within the given range is negotiated.
5 Calculated without the benefit of ISI compensation and before skew compensation.
6 Calculated with the benefit of ISI compensation and skew compensation.

Table 32: SCSI Fast-160 Timing Budget Template

Item	Fast-80 (Reference)	Fast-160	Comments
Nominals:			
REQ(ACK) Period	**25 ns**	**12,5 ns**	
Data transfer period	**12,5 ns**	**6,25 ns**	
Ideal Setup/Hold	**6,25 ns**	**3,125 ns**	
Non-compensatable:			**Without PLL**
REQ(ACK) period tolerance / 2	**0,3 ns**	**0,3 ns**	**Tolerance of transmitter Note 1**
Driver asymmetry / 2	**0,25 ns**	**0,25 ns**	**Data bus Note 2**
Receiver asymmetry / 2	**0,25 ns**	**0,25 ns**	**Data bus Note 2**
Driver asymmetry / 2	**0,25 ns**	**0,25 ns**	**REQ(ACK) Note 2**
Receiver asymmetry / 2	**0,25 ns**	**0,25 ns**	**REQ(ACK) Note 2**
Crosstalk & noise	**0,5 ns**	**0,5 ns**	**Time impact on data bus**
Crosstalk & noise	**0,5 ns**	**0,5 ns**	**Time impact on data REQ(ACK)**
Chip noise	**0,1 ns**	**0,2 ns**	**Transmitter & Receiver?**
Receiver amplitude skew	**0,2 ns**	**0,2 ns**	**Post compensation delta**
Clock jitter	**0,5 ns**	**0,25 ns**	**Less due to %?**
Non-compensatable total:	**3,1 ns**	**2,95 ns**	
Compensatable skew:			**Or partially**
Transmitter chip skew	**1,25 ns**	**1,25 ns**	**Without asymmetry Petty 1,065 ns**
Receiver chip skew	**1,25 ns**	**1,25 ns**	**Without asymmetry Petty 1,065 ns**
Cable skew	**2,5 ns**	**2,5 ns**	**12 m case 1,5 ns**
Two x trace skew	**0,4 ns**	**0,4 ns**	
ISI of data	**0,425 ns**	**1,0 ns**	**Worse case pattern Petty +2 -1 ns on 12 m**
ISI of REQ(ACK)	**0,425 ns**	**0,0 ns**	**Post preamble**

Table 32: SCSI Fast-160 Timing Budget Template

Item	Fast-80 (Reference)	Fast-160	Comments
Compensatable total:	6,25 ns	6,4 ns	Petty 7,03 ns
ISI Compensation	0,0 ns	0,4 ns	Modeling/data needed Petty ? ns
Skew compensation	0,0 ns	4,15 ns	Assumes 6,25 ns with 32 taps compensated to 5 tap accuracy & ~ 25% delay tolerance (duplicated tolerances(?)) Petty 4,93 ns (?)
Compensation total:	0,0 ns	4,55 ns	Petty 5,58 ns (?)
Net error:	9,35 ns	4,8 ns	Petty 4,40 ns
Net window (setup -error)	-3,1 ns	-1,675 ns	Note 3
Net window (transfer period - error)	3,15 ns	1,45 ns	Petty 1,85 ns Note 4

Notes:
1) Tolerance adjusted for half cycle (data transfer period)
2) Assumes trimmed to split asymmetry
3) Fast-80 budget in SPI-3 neglects asymmetry and lumps chip noise, clock jitter, crosstalk, noise, ISI and receiver amplitude skew into other terms (e.g., signal distortion skew) and/or ignores the effects.
4) Figure 46 shows this to be not valid but some of the non-compensatable errors may need to be halved to account for their impact only in one direction in reducing setup or hold time.

9.3.1 Cable skew

The maximum difference in propagation time allowed between any two SCSI bus signals measured between any two SCSI devices excluding any signal distortion skew delays.

9.3.2 pCRC Receive hold time

The minimum time required at the receiver between the transition of the REQ signal and the transition of the P_CRCA signal while pCRC protection is enabled.

9.3.3 pCRC Receive setup time

The minimum time required at the receiver between the transition of the P_CRCA signal and the transition of the REQ signal while pCRC protection is enabled.

9.3.4 pCRC Transmit hold time

The minimum time provided by the transmitter between the transition of the REQ signal and the transition of the P_CRCA signal while pCRC protection is enabled.

9.3.5 pCRC Transmit setup time

The minimum time provided by the transmitter between the transition of the P_CRCA signal and the transition of the REQ signal while pCRC protection is enabled.

9.3.6 Receive assertion period

The minimum time required at a SCSI device receiving a REQ signal for the signal to be asserted while using synchronous data transfers, provided P_CRCA is not transitioning with pCRC protection enabled. Also, the minimum time required at a SCSI device receiving an ACK signal for the signal to be asserted while using synchronous data transfers. For SE fast-5 and fast-10 operation, the time period is measured at the 0,8 V level. For SE fast-20 operation the period is measured at the 1,0 V level. For LVD see figure 44 and figure 43 for signal measurement points.

9.3.7 Receive hold time

For ST data transfers the minimum time required at the receiving SCSI device between the assertion of the REQ signal or the ACK signals and the changing of the DATA BUS while using synchronous data transfers, provided P_CRCA is not transitioning with pCRC protection enabled. For DT data transfers the minimum time required at the receiving SCSI device between the transition (i.e. assertion or negation) of the REQ signal or the ACK signals and the changing of the DATA BUS while using synchronous data transfers.

NOTE 19 - For timing budget purposes the value stated in the table is calculated without the benefit of ISI and without the benefit of skew compensation.

9.3.8 Receive negation period

The minimum time required at a SCSI device receiving a REQ signal for the signal to be negated while using synchronous data transfers. Also, the minimum time required at a SCSI device receiving an ACK signal for the signal to be asserted while using synchronous data transfers. For SE fast-5 and fast-10 operation, the time period is measured at the 2,0 V level. For SE fast-20 operation the period is measured at the 1,9 V level. For LVD see figure 44 and figure 43 for signal measurement points.

9.3.9 Receive setup time

For ST data transfers the minimum time required at the receiving SCSI device between the changing of

DATA BUS and the assertion of the REQ signal or the ACK signal while using synchronous data transfers. For DT data transfers the minimum time required at the receiving SCSI device between the changing of DATA BUS and the transition of the REQ signal or the ACK signal while using synchronous data transfers.

NOTE 20 - For timing budget purposes the value stated in the table is calculated without the benefit of ISI and without the benefit of skew compensation.

9.3.10 Receive REQ (ACK) period tolerance

The minimum tolerance that a SCSI device shall allow to be subtracted from the REQ (ACK) period.

9.3.11 Receive REQ assertion period with P_CRCA transitioning

The minimum time required at a SCSI device receiving a REQ signal for the signal to be asserted while using synchronous data transfers with P_CRCA transitioning with pCRC protection enabled.

9.3.12 Receive REQ negation period with P_CRCA transitioning

The minimum time required at a SCSI device receiving an REQ signal for the signal to be negated while using synchronous data transfers with P_CRCA transitioning with pCRC protection enabled.

9.3.13 REQ (ACK) period

The REQ (ACK) period during synchronous data transfers is measured from an assertion edge of the REQ (ACK) signal to the next assertion edge of the signal. In DT DATA phases the nominal transfer period for data is half that of the REQ (ACK) period during synchronous data transfers since data is qualified on both the assertion and negation edges of the REQ (ACK) signal. In ST DATA phases the nominal transfer period for data is equal to the REQ (ACK) period during synchronous data transfers since data is only qualified the assertion edge of the REQ (ACK) signal.

9.3.14 Signal Timing Skew

The maximum signal timing skew occurs when transferring random data and in combination with interruptions of the REQ (ACK) signal transitions (e.g., pauses caused by offsets). The signal timing skew includes cable skew (measured with 0101... patterns) and signal distortion skew caused by random data patterns and transmission line reflections as shown in figure 44, figure 45, figure 46, and figure 43.

The receiver detection range is the part of the signal between the "may detect" level and the "shall detect" level on either edge. (see 9.4)

NOTE 21 - For timing budget purposes the value stated in the table is calculated without the benefit of ISI and without the benefit of skew compensation.

9.3.15 Transmit assertion period

The minimum time that a target shall assert the REQ signal while using synchronous data transfers, provided it is not transitioning P_CRCA with pCRC protection enabled. Also, the minimum time that an initiator shall assert the ACK signal while using synchronous data transfers.

9.3.16 Transmit hold time

For ST data transfers the minimum time provided by the transmitting SCSI device between the assertion of the REQ signal or the ACK signal and the changing of the DATA BUS while using synchronous data transfers. For DT data transfers the minimum time provided by the transmitting SCSI device between the transition of the REQ signal or the ACK signal and the changing of the DATA BUS while using synchronous data transfers.

NOTE 22 - For timing budget purposes the value stated in the table is calculated without the benefit of ISI and without the benefit of skew compensation.

9.3.17 Transmit negation period

The minimum time that a target shall negate the REQ signal while using synchronous data transfers, provided it is not transitioning P_CRCA with pCRC protection enabled. Also, the minimum time that an initiator shall negate the ACK signal while using synchronous data transfers.

9.3.18 Transmit setup time

For ST data transfers the minimum time provided by the transmitting SCSI device between the changing of DATA BUS and the assertion of the REQ signal or the ACK signal while using synchronous data transfers. For DT data transfers the minimum time provided by the transmitting SCSI device between the changing of DATA BUS and the transition of the REQ signal or the ACK signal while using synchronous data transfers.

NOTE 23 - For timing budget purposes the value stated in the table is calculated without the benefit of ISI and without the benefit of skew compensation.

9.3.19 Transmit REQ (ACK) period tolerance

The maximum tolerance that a SCSI device may subtract from the REQ (ACK) period.

9.3.20 Transmit REQ assertion period with P_CRCA transitioning

The minimum time that a target shall assert the REQ signal during a DT DATA phase while transitioning P_CRCA with pCRC protection enabled.

9.3.21 Transmit REQ negation period with P_CRCA transitioning

The minimum time that a target shall negate the REQ signal during a DT DATA phase while transitioning P_CRCA with pCRC protection enabled.

9.3.22 Transmit ISI Compensation

The effective reduction in worse case ISI timing shift provided by the transmitting SCSI device as seen at the receiving SCSI device connector. The value used is the one that provides minimum timing margin.

9.3.23 Receive Skew Compensation

The effective reduction in worse case timing skew of data, parity, and strobe signals provided by the receiving SCSI device but not directly observable at the receiving SCSI device connector. The value used is the one that provides minimum timing margin.

9.3.24 Strobe offset tolerance

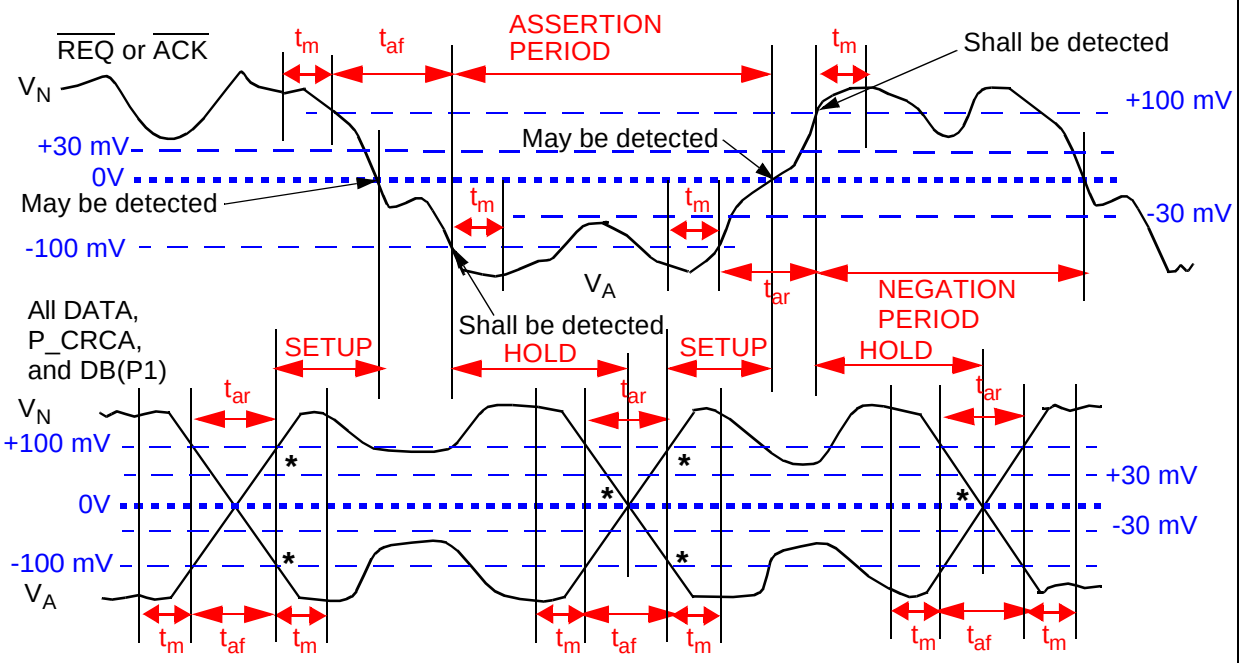
The tolerance on the time used to delay the compensated REQ/ACK to strobe the data and parity signals provided by the receiving SCSI device but not directly observable at the receiving SCSI device connector. The value used is the one that provides minimum timing margin.

9.3.25 Net Receive Internal Setup and Hold times

The net effective setup time measured within the receiving SCSI device from the worse case bit (data or parity) to the compensated offset strobe. This time may not be observable to other than the SCSI device designer. Failure to meet the requirement may be observable in terms of increased error rates.

9.4 Measurement points

The measurements points for SE and differential ACK, REQ, DATA, P_CRCA, and PARITY signals are defined in this clause.



* Use the crossing that yields the shorter SETUP and HOLD time

Notes:

1 V_N - negated signal

2 V_A - asserted signal

3 t_m = 1,25ns minimum

4 V_A or V_N are required to drive the 100 mV at the leading edge of the transition. Those signals shall be at least |100 mV| for at least t_m before and after the transition.

5 Differential voltage signals in all cases.

6 t_{af} and t_{ar} shall be less than 3 ns.

7 Any signal structure may occur at the receiver while in the t_{af} or t_{ar} region including slope reversal.

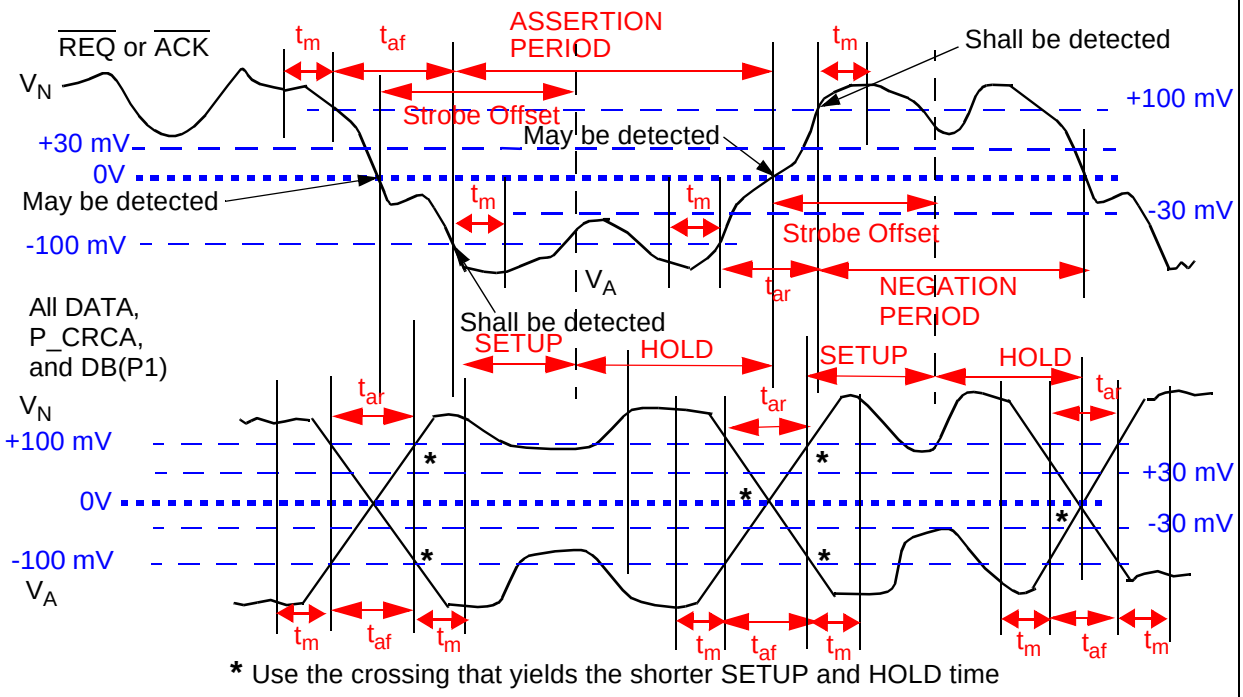
Figure 43 - LVD timing measurement points for DT =< Fast-80 data transfers

The signal shall transition from -100 to +100 mV or +100 to - 100 mV in 0 to 3 ns, the waveform between -100 and +100 mV is not otherwise specified. Signals shall remain above the |100 mV| level for 1,25 ns at each end of the transition. The signals shall not drop below |30 mV| except during the transitions. Conditions exist with longer, loaded SCSI busses and irregular REQ and ACK pulse widths where long assertions or negations produce a much larger signal than short assertions or negations. This sets up an environment where the short REQ or ACK pulses may not have adequate timing margin unless the definitions in figure 44 and figure 43 are used in the measurement of timing parameters.

Measurement of driver timing parameters shall be performed using the circuit and test conditions defined in A.2.5 applied to the SCSI device connector. Receiver timing parameters are defined by the waveforms existing at the connector of the receiving SCSI device. The receiver timing parameters include the effects

of data pattern. The receiver data pattern is therefore not defined.

Figure 45 shows the LVD signal requirements at the receiving SCSI device.



* Use the crossing that yields the shorter SETUP and HOLD time

Notes:

1 V_N - negated signal

2 V_A - asserted signal

3 t_m = 1,25ns minimum

4 V_A or V_N are required to drive the 100 mV at the leading edge of the transition. Those signals shall be at least |100 mV| for at least t_m before and after the transition.

5 Differential voltage signals in all cases.

6 t_{af} and t_{ar} shall be less than 3 ns.

7 Any signal structure may occur at the receiver while in the t_{af} or t_{ar} region including slope reversal.

8 Strobe Offset is from the actual detected time (somewhere between may and shall detect) to the implemented offset time.

Figure 44 - LVD timing measurement points for DT = Fast-160 data transfers

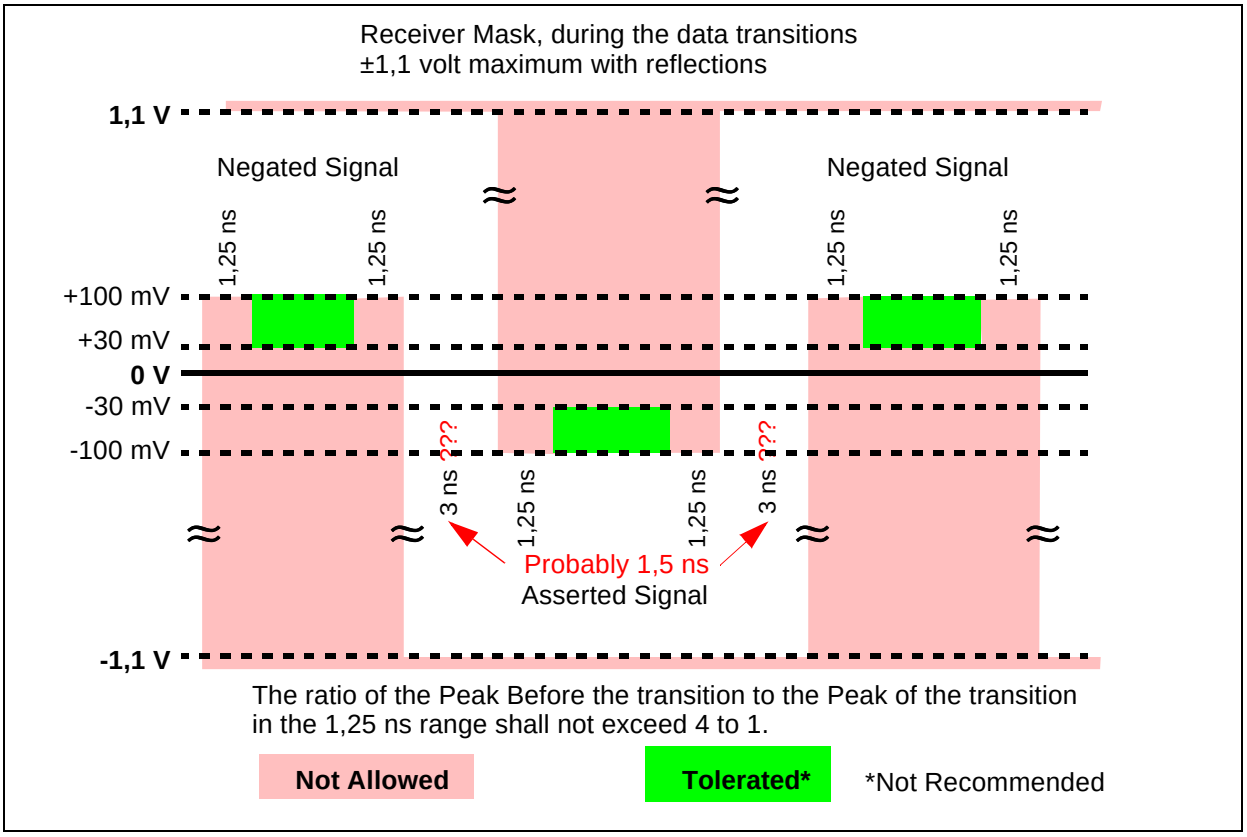


Figure 45 - LVD receiver mask

9.5 Setup and hold timings

9.5.1 DT data transfer calculations

Figure 46 shows how the setup and hold times are calculated for various physical configurations on SCSI devices that support DT data transfers. The minimum set up and hold timings specified in figure 46 shall be used. Note that these values are different for the driver and the receiver but that the receiver sensitivity provides the threshold points for both. This is required because both extreme cases of attenuation need to be covered:

a) receivers connected to drivers with very short interconnect, and
b) receivers connected to drivers through worst case interconnect.

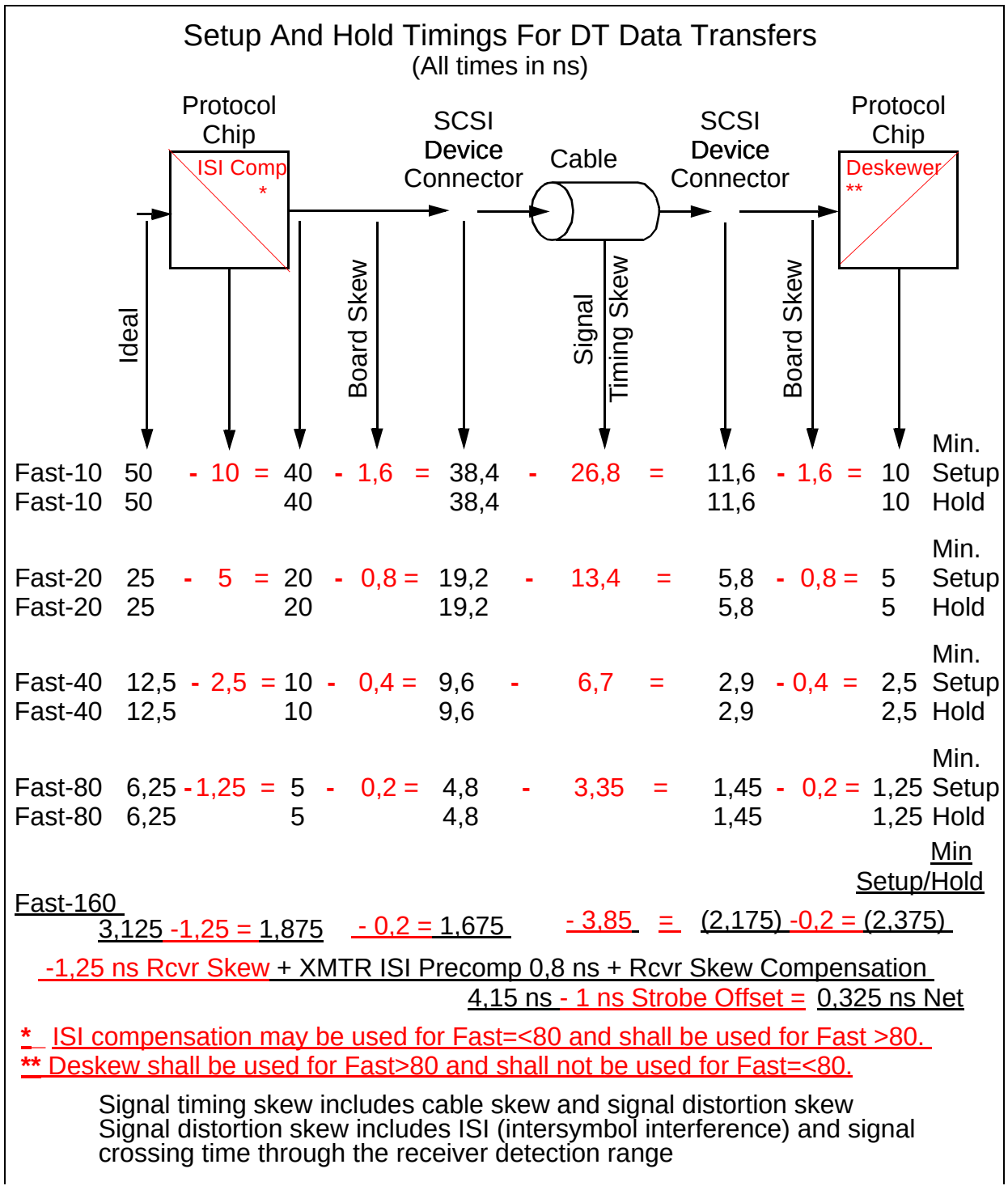


Figure 46 - System setup and hold timings for DT data transfers (all times in ns) (TBD)

9.5.1.1 DT synchronous data transfer

When a DT data transfer agreement has been established the target shall only use the DT DATA IN phase and DT DATA OUT phase for data transfers.

During DT data transfers at up to Fast-80 data shall be clocked by the originating SCSI device with a clock preceding both the assertion and negation of the REQ/ ~~and~~ ACK signal lines by half a bit period. DT data

transfers at up to Fast-80 data shall be clocked by the receiving SCSI device by both the assertion and negation of the REQ and ACK signal lines. References to REQ/ACK transitions in this subclause refer to either an assertion or a negation of the REQ or ACK signal.

During DT data transfers at negotiated rates greater than Fast-80, if P1 is true at strobe time, data shall be clocked by the originating SCSI device by both the assertion and negation of the REQ/ACK signal lines. If P1 is false at strobe time, data shall be ignored. The originating SCSI device shall apply ISI compensation to all the data, parity, and REQ/ACK signals. DT data transfers at rates greater than Fast-80 data shall be clocked by the receiving SCSI device by both the assertion and negation of the REQ and ACK signal lines after having been deskewed by the receiving SCSI device.

The REQ/ACK offset specifies the maximum number of REQ transitions, with P1 true if the transfer is DATA IN transfer at negotiated rates greater than Fast-80, that shall be sent by the target in advance of the number of ACK transitions received from the initiator, establishing a pacing mechanism. If the initiator shall use the pad bytes, if any, in the generation of the transmitted pCRC. The target shall then use those pad bytes, if any, for checking against the computed pCRC for the current data group. Upon receipt of the last byte of the pCRC field, the received pCRC and computed pCRC shall be compared.

If received pCRC and computed pCRC do not match (i.e., a pCRC error is detected), or if an improperly formatted data group is transferred, then the associated data group shall be considered invalid.

If the target does not retry transferring the information transfer or it exhausts its retry limit the target shall go into a STATUS phase and send a CHECK CONDITION status with a sense key set to ABORTED COMMAND and an additional sense code set to SCSI PARITY ERROR for the task associated with the pCRC error.

9.5.1.2 Fast=>80 Training Pattern

The training pattern for Fast-160 shall be transferred at the start of each Fast-160 data phase. Return ACK/REQ signals from the receiving SCSI device shall be ignored by the originating SCSI device during the training pattern. The training pattern for Fast-160 shall conform to Figure TBD. The receiving SCSI device shall use some or all elements of the training pattern to achieve deskewing. The transmitting device shall not make an intentional shift in relative timing between the databus and the ACK/REQ signal subsequent to the training pattern during the DT data phase. The requirement to not intentionally change relative timing does not include the effects of ISI or ISI compensation.

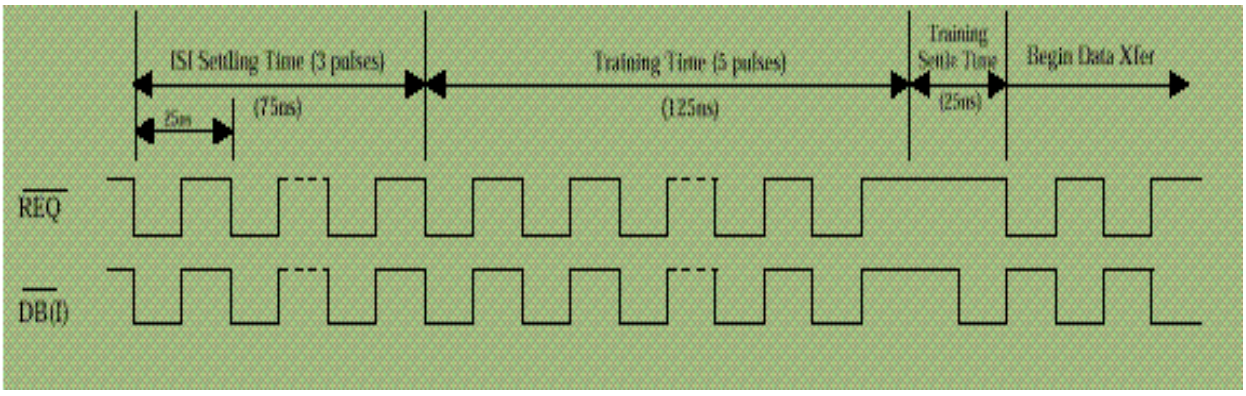


Figure 47 - Fast-160 Training Pattern

9.5.2 PARALLEL PROTOCOL REQUEST

PARALLEL PROTOCOL REQUEST messages (see table 33) are used to negotiate a synchronous data transfer agreement, a wide data transfer agreement, and set the protocol options between two SCSI

devices.

Table 33 - PARALLEL PROTOCOL message format

Bit / Byte	7	6	5	4	3	2	1	0
0	EXTENDED MESSAGE (01h)							
1	EXTENDED MESSAGE LENGTH (06h)							
2	PARALLEL PROTOCOL REQUEST (04h)							
3	TRANSFER PERIOD FACTOR							
4	RESERVED							
5	REQ/ACK OFFSET							
6	TRANSFER WIDTH EXPONENT (m)							
7	RESERVED					QAS_REQ	DT_REQ	IU_REQ

The PERIOD FACTOR field is defined in table 34.

Table 34 - TRANSFER PERIOD FACTOR field

Code	Description
00h-06h	Reserved (note 1)
07h	Transfer period equals 6,25 ns (note 2). This code is only valid if the PROTOCOL OPTIONS field has a value selected that supports double-transition data transfers.
08h	Transfer period equals 8,333 ns (note 3). This code is only valid if the PROTOCOL OPTIONS field has a value selected that supports double-transition data transfers.
09h	Transfer period equals 12.5 ns (note 4). This code is only valid if the PROTOCOL OPTIONS field has a value selected that supports double-transition data transfers.
0Ah	Transfer period equals 25 ns (note 5)
0Bh	Transfer period equals 30,3 ns (note 5)
0Ch	Transfer period equals 50 ns (note 6)
0Dh-18h	Transfer period equals the period factor x 4 (note 6)
19h-31h	Transfer period equals the period factor x 4 (note 7)
32h-FFh	Transfer period equals the period factor x 4 (note 8)

note:
1 - Faster timings may be allowed by future SCSI parallel interface standards.
2 - Fast-160 data is latched every 6,25 ns.
3 - Fast- 120 data is latched every 8,333 ns.
4 - Fast-80 data is latched every 12,5 ns.
5 - Fast-40 data is latched every 25 ns or 30,3 ns.
6 - Fast-20 data is latched using a transfer period of less than or equal 96 ns and greater than or equal to 50 ns.
7 - Fast-10 data is latched using a transfer period of less than or equal 196 ns and greater than or equal 100 ns.
8 - Fast-5 data is latched using a transfer period of less than or equal 1020 ns and greater than or equal to 200 ns

For ST synchronous data transfer the REQ/ACK OFFSET is the maximum number of REQ assertions allowed to be outstanding before a corresponding ACK assertion is received at the target. The size of a data transfer may be 1or 2 bytes depending on the values in the transfer width exponent field.

For DT synchronous data transfer the REQ/ACK OFFSET is the maximum number of REQ transitions allowed to be outstanding before a corresponding ACK transition is received at the target. The size of a data transfer shall be 2 bytes.

See 4.7 for an explanation of the differences between DT and ST data transfers.

The REQ/ACK OFFSET value is chosen to prevent overflow conditions in the SCSI device's reception buffer and offset counter. A REQ/ACK OFFSET value of zero shall indicate asynchronous data transfer mode and

that the PERIOD FACTOR field and the PROTOCOL OPTIONS field shall be ignored; a value of FFh shall indicate unlimited REQ/ACK offset.

The TRANSFER WIDTH EXPONENT field defines the transfer width to be used during DATA IN phases, and DATA OUT phases. The transfer width that is established applies to all logical units on both SCSI devices. Valid transfer widths are 8 bits (m=00h) and 16 bits (m=01h) if all the protocol options bits are zero. The only valid transfer width is 16 bits (m=01h) if any of the protocol options bits are one. TRANSFER WIDTH EXPONENT field values greater than 01h are reserved.

The protocol options bits (IU_REQ, DT_REQ, and QAS_REQ) are used by the originating SCSI device to indicate the protocol options to be enabled. The responding SCSI device uses the protocol options bits to indicate the protocol options requested by the originating SCSI device the responding SCSI device has enabled.

An information units enable request bit (IU_REQ) of zero indicates that information unit transfers shall not be used (i.e., data group transfers shall be enabled) when received from the originating SCSI device and that information unit transfers are not supported when received from the responding SCSI device. An IU_REQ bit of one indicates that information unit transfers shall be used when received from the originating SCSI device and that information unit transfers are supported when received from the responding SCSI device. If the IU_REQ bit is changed from the previous agreement (i.e., zero to one or one to zero) as a result of a negotiation the target shall go to a BUS FREE phase on completion of the negotiation.

A DT enable request bit (DT_REQ) of zero indicates that DT DATA phases are to be disabled when received from the originating SCSI device and that DT DATA phases are not supported when received from the responding SCSI device. An DT_REQ bit of one indicates that DT DATA phases are to be enabled when received from the originating SCSI device and that DT DATA phases are supported when received from the responding SCSI device.

A QAS enable request bit (QAS_REQ) of zero indicates that QAS is to be disabled when received from the originating SCSI device and that QAS is not supported when received from the responding SCSI device. An QAS_REQ bit of one indicates that QAS is to be enabled when received from the originating SCSI device and that QAS is supported when received from the responding SCSI device.

Not all combinations of the protocol options bits are valid. Only the bit combinations defined in table 35 shall be allowed. All other combinations are reserved.

Table 35 - Valid protocol options bit combinations

QAS_REQ	DT_REQ	IU_REQ	**Description**
0	0	0	Use ST DATA IN and ST DATA OUT phases to transfer data
0	1	0	Use DT DATA IN and DT DATA OUT phases with data group transfers
0	1	1	Use DT DATA IN and DT DATA OUT phases with information unit transfers
1	1	1	Use DT DATA IN and DT DATA OUT phases with information unit transfers and use QAS for arbitration

A PARALLEL PROTOCOL REQUEST agreement applies to all logical units of the two SCSI devices that negotiated agreement. That is, if SCSI device A, acting as an initiator negotiates a data transfer agreement with SCSI device B (a target), then the same data transfer agreement applies to SCSI devices A and B

even if SCSI device B changes to an initiator.

A data transfer agreement only applies to the two SCSI devices that negotiate the agreement. Separate data transfer agreements are negotiated for each pair of SCSI devices. The data transfer agreement only applies to DATA phases and information unit transfers.

A PARALLEL PROTOCOL REQUEST message exchange shall be initiated by a SCSI device whenever a previously arranged parallel protocol agreement may have become invalid. The agreement becomes invalid after any condition that may leave the parallel protocol agreement in an indeterminate state such as:

a) after a hard reset;
b) after a TARGET RESET message;
c) after a power cycle;
d) after a change in the transceiver mode (e.g., LVD mode to SE mode).

Any condition that leaves the data transfer agreement in an indeterminate state shall cause the SCSI device to enter an asynchronous, eight-bit wide data transfer mode with all the protocol options bits set to set to zero.

A SCSI device may initiate a PARALLEL PROTOCOL REQUEST message exchange whenever it is appropriate to negotiate a data transfer agreement. SCSI devices that are currently capable of supporting any of the PARALLEL PROTOCOL REQUEST options shall not respond to a PARALLEL PROTOCOL REQUEST message with a MESSAGE REJECT message.

Renegotiation after every selection is not recommended, since a significant performance impact is likely.

The PARALLEL PROTOCOL REQUEST message exchange establishes an agreement between the two SCSI devices;

a) on the permissible periods and the REQ/ACK offsets for all logical units on the two SCSI devices. This agreement only applies to ST DATA IN phases, ST DATA OUT phases, DT DATA IN phases, and DT DATA OUT phases. All other phases shall use asynchronous transfers;
b) on the width of the data path to be used for DATA phase transfers between two SCSI devices. This agreement only applies to ST DATA IN phases, ST DATA OUT phases, DT DATA IN phases, and DT DATA OUT phases. All other information transfer phases shall use an eight-bit data path; and
c) on the protocol option is to be used.

The originating SCSI device (the SCSI device that sends the first of the pair of PARALLEL PROTOCOL REQUEST messages) sets its values according to the rules above to permit it to receive data successfully. If the responding SCSI device is able to receive data successfully with these values (or smaller periods or larger REQ/ACK offsets or both), it returns the same values in its PARALLEL PROTOCOL REQUEST message. If it requires a larger period, a smaller REQ/ACK offset, or a smaller transfer width in order to receive data successfully, it substitutes values in its PARALLEL PROTOCOL REQUEST message as required, returning unchanged any value not required to be changed. Each SCSI device when transmitting data shall respect the negotiated limits set by the other's PARALLEL PROTOCOL REQUEST message, but it is permitted to transfer data with larger periods, smaller synchronous REQ/ACK offsets, or both. The completion of an exchange of PARALLEL PROTOCOL REQUEST messages implies an agreement as shown in table 36.

If the responding SCSI device does not support the selected protocol option it shall clear as many bits as required to set the protocol option field to a legal value that it does support.

Table 36 - PARALLEL PROTOCOL REQUEST messages implied agreements

Responding SCSI device PARALLEL PROTOCOL REQUEST response	Implied agreement
Non-zero REQ/ACK offset	Synchronous transfer (i.e., Each SCSI device transmits data with a period equal to or greater than and a REQ/ACK offset equal to or less than the negotiated values received in the responding SCSI device's PPR message).
REQ/ACK offset equal to zero	Asynchronous transfer
Non-zero TRANSFER WIDTH EXPONENT	Wide transfer (i.e., the initiator and the target transmit data with a transfer width equal to the responding device's transfer width). If the initiating SCSI device does not support the responding SCSI device's TRANSFER WIDTH EXPONENT then the initiating SCSI device shall MESSAGE REJECT the PARALLEL PROTOCOL REQUEST message (see 7.9.9.1 and 7.9.9.2).
TRANSFER WIDTH equal to zero	Eight-bit data
protocol options equal to 0h and transfer period factor equal to 9h	Eight-bit/asynchronous data transfer with PROTOCOL OPTIONS field set to 0h
IU_REQ, DT_REQ, and QAS_REQ equal to zero	ST DATA IN and ST DATA OUT phases to transfer data
DT_REQ equal to one	DT DATA IN and DT DATA OUT phases to transfer data with iuCRC
IU_REQ, and DT_REQ equal to one	DT DATA IN and DT DATA OUT phases with information units
IU_REQ, DT_REQ, and QAS_REQ equal to one	DT DATA IN and DT DATA OUT phases with information units and use QAS for arbitration
MESSAGE REJECT message	Eight-bit/asynchronous data transfer with protocol options field set to 0h
Parity error (on responding message)	Eight-bit/asynchronous data transfer with PROTOCOL OPTIONS field set to 0h
Unexpected bus free (as a result of the responding message)	Eight-bit/asynchronous data transfer with PROTOCOL OPTIONS field set to 0h
No response	Eight-bit/asynchronous data transfer with protocol options field set to 0h

If there is an unrecoverable parity error on the initial PARALLEL PROTOCOL REQUEST message (see 10.9.1 and 10.9.2) the initiating SCSI device shall retain its previous data transfer mode and protocol options. If there is an unexpected bus free on the initial PARALLEL PROTOCOL REQUEST message the initiating SCSI device shall retain its previous data transfer mode and protocol options.

Annex N Example Fast-160 Techniques

(informative)

0.1 ISI Compensation

ISI compensation may be achieved by several techniques including time shifting and transmitter drive strength switching. The technique employed is vendor specific but SPI-4 requires that the technique achieves at least a 0,8 ns reduction in ISI at Fast-160.

Figure N.1 illustrates a transmitter drive strength technique.

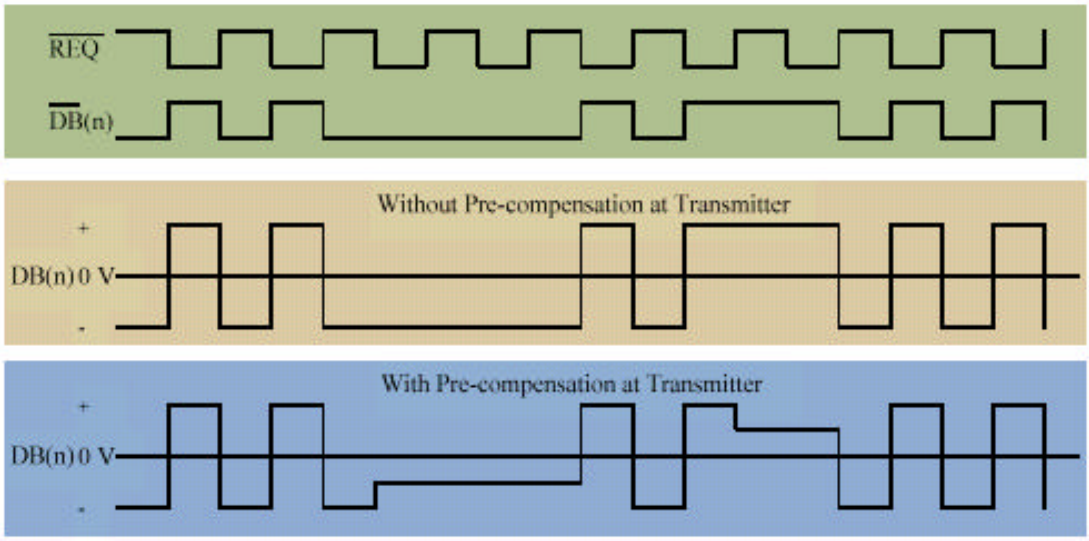


Figure N.1 illustrates a transmitter drive strength technique.

0.2 Deskewing

The deskewing technique used in the receiving SCSI device is vendor unique. Any technique that works with the SPI-4 specified training pattern and complies with the specified Receive Skew Compensation timing requirement is allowed. Figure N.2 illustrates such a technique. The training pattern is not available in Fast=<80 and consequently deskewing is only used for Fast>80.

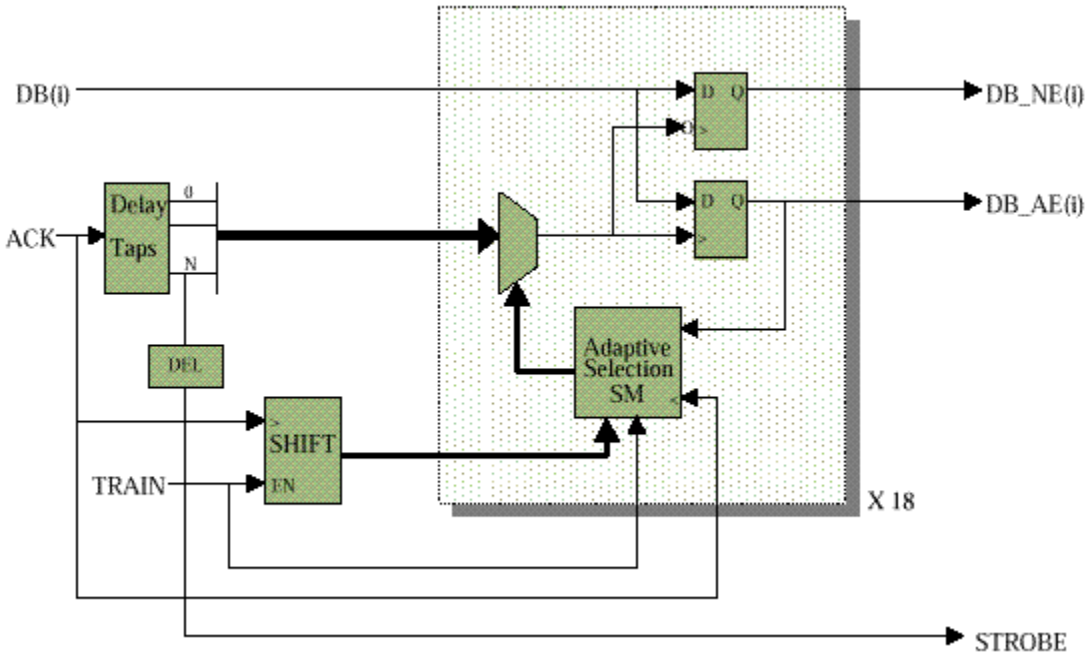


Figure N.2 Example Deskewing Technique

In this example the tap selection is based upon a binary search algorithm.