To: T10 Membership
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Subject: Ultra3 Expander Guidelines
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Expanders need a set of guidelines for implementation that will allow them to be forward compatible. The correct behavior for expanders is not easily deduced from the rules for targets and initiators in SPI-3.

1. Driving P(0) and P(1)

1) drive P(0) and P(1) as data parity signals when bus is running in Fast-5, Fast-10, Fast-20, and Fast 40 speeds [negotiations are done with WDTR/SDTR].

2) drive P(0) from the target to initiator for data group [Ultra160m, DT, P(0)CRCA] mode [negotiations are done with PPR]. [note that this is contrary what SPI-3 currently states] P(1) is negated.

3) drive P(0) in direction opposite of data flow for information unit transfers [Packetized mode] to support flow control; [negotiations are done with PPR]. P(1) is driven in the direction of the data flow [note that this is contrary what SPI-3 currently states].

2. STT Support

All targets and expanders should support the Synchronous Transfer Timeout feature. If an expander detects an unexpected BUS FREE phase on the driving side it should release all signals on the propagating side.

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4. Bus Segment Topology Mapping (BSTM)

Bus segment topology mapping uses a feature of the expander that lets the initiator enable/disable the farside transceivers of an expander. By disabling the farside transceivers the initiator can walk the bus segments and gain valuable information about the topology.

In addition the expander does not pass the expander selection through until it is enable. All normal and extended selections pass. This lets an initiator detect the presence of expanders in various topologies.

5. Selective Segment Reset

Selective segment reset is a feature of the expander that lets it assert the RST signal on the farside when it receives a BUS DEVICE RESET message. Expanders supporting this feature would not propagate the RST signal. This lets an initiator manage the bus on a segment by segment basis.

6. Expander Addressing

Addressing expanders can be done with a simple extension of the extended addressing concept. A five-bit value is asserted on the lower-byte DB(7-0) as a signature and the expander address is on the upper byte DB(15-8). Devices addressed in this manner cannot participate in arbitration and thus are prevented from performing a re-selection.

Valid bit combinations for the upper and lower nibble of the lower byte. This gives a total combination of 24 signatures, with eight of each type of device selectable with the upper byte. Signature A7h and ABh are assigned to expanders; signature 37h is assigned to terminators; signature 3Eh is assigned to enclosure chips.

DB(7-4)	DB(3-0)
0011 (3h)	0111 (7h)
0101 (5h)	1011 (Bh)
0110 (6h)	1111 (Dh)
1001 (9h)	1110 (Eh)
1010 (Ah)	
1100 (Ch)	

The following illustrations will be used to discuss BSTM.